TONO

Θ-5000E

SERVICE MANUAL

TABLE OF CONTENTS

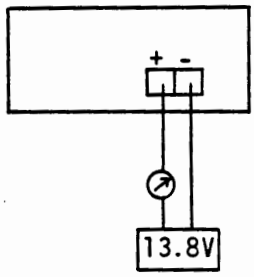
TONO CORPORATION
98 Motosoja-Machi, Maebashi-shi, 371, Japan
Phone : 0272-53-6955 Telex : (0)3422-732 tono j

1. POWER SUPPLY CIRCUIT

Fuse: for DC ..... installed at a fuse clip on the power supply board (midget type).
for AC 100-120V ..... inserted in a fuse holder on the rear panel.
for AC 200-240V ..... inserted in a fuse holder on the rear panel.

1.1 DC

Pull out the AC cord.
Connect the DC power supply (13.8V-14V) to the Theta-5000E through an ampare meter (2A-3A).
Turn on the DC power supply and then the power switch of the Theta-5000E.
The value of current should be approx. 1.4A.
Check if there is no abnormal oscillation at +5VDC and +12VDC outputs.



[PROBLEMS]

1. Over-current (including fuse cut)

   1) Is there any short circuit at D30 (DBA30), D32 (RD30E or the equivalent 30V zener diode)?

   2) Does the over-current run even when CN8 is removed?
      YES ↓
      Check the parts on the power supply board.
      NO ↓
      Remove the other connectors CN2, CN5, CN9, CN6 and CN3 to check if there is any defect on the CPU board or the other boards.

2. No current runs

   1) Check the fuse.
   2) S1 switch may be defective.
   3) AC socket may be defective.
   4) CN8 may be defective of contact.
   5) IC53 (7805) and IC54 (7812) may be defective.
   6) D30 (DBA30) may be defective.

3. Abnormal oscillation

   1) Do both of IC53 and IC54 oscillate abnormally?
      YES ↓
      The capacity of C150 (47μ) may be deficient.

2) IC53 oscillates abnormally. ⟶ The capacity of C119 (0.33μ) may be deficient or IC53 may be defective.

3) IC54 oscillates abnormally. ⟶ The capacity of C118 (0.33μ) may be deficient or IC54 may be defective.

4. Increase/decrease of current

1) When the +5VDC output is greatly changed, the thermal protector of IC53 is working. ⟶ Check if R157 (39 ohms) is broken down.

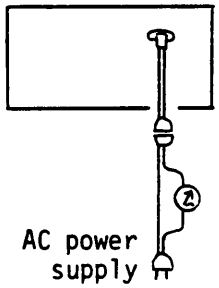
2) When the +12VDC output is greatly changed, the thermal protector of IC54 is working. ⟶ Check if R155 (33 ohms) is broken down.

3) Both the +5VDC and +12VDC outputs are greatly changed. ⟶ Check the AC power supply voltage. It should not exceed 125V or 250V.

NOTE: Even though a great voltage is measured at the +5VDC and +12VDC outputs when the power supply board is in no-load state with CN8 removed, the unit is considered to be in normal state in case the rated voltage is obtained with the rated load.

1.2 AC

Attach the AC cord to the unit.
Connect the unit to the AC power supply through an ampare meter (1A).
Turn on the power switch of the Theta-5000E.
See if the input/output voltage of IC53 (7805) and IC54 (7812) are as shown below.
Also see if there is no abnormal oscillation at the +5VDC and +12VDC outputs.

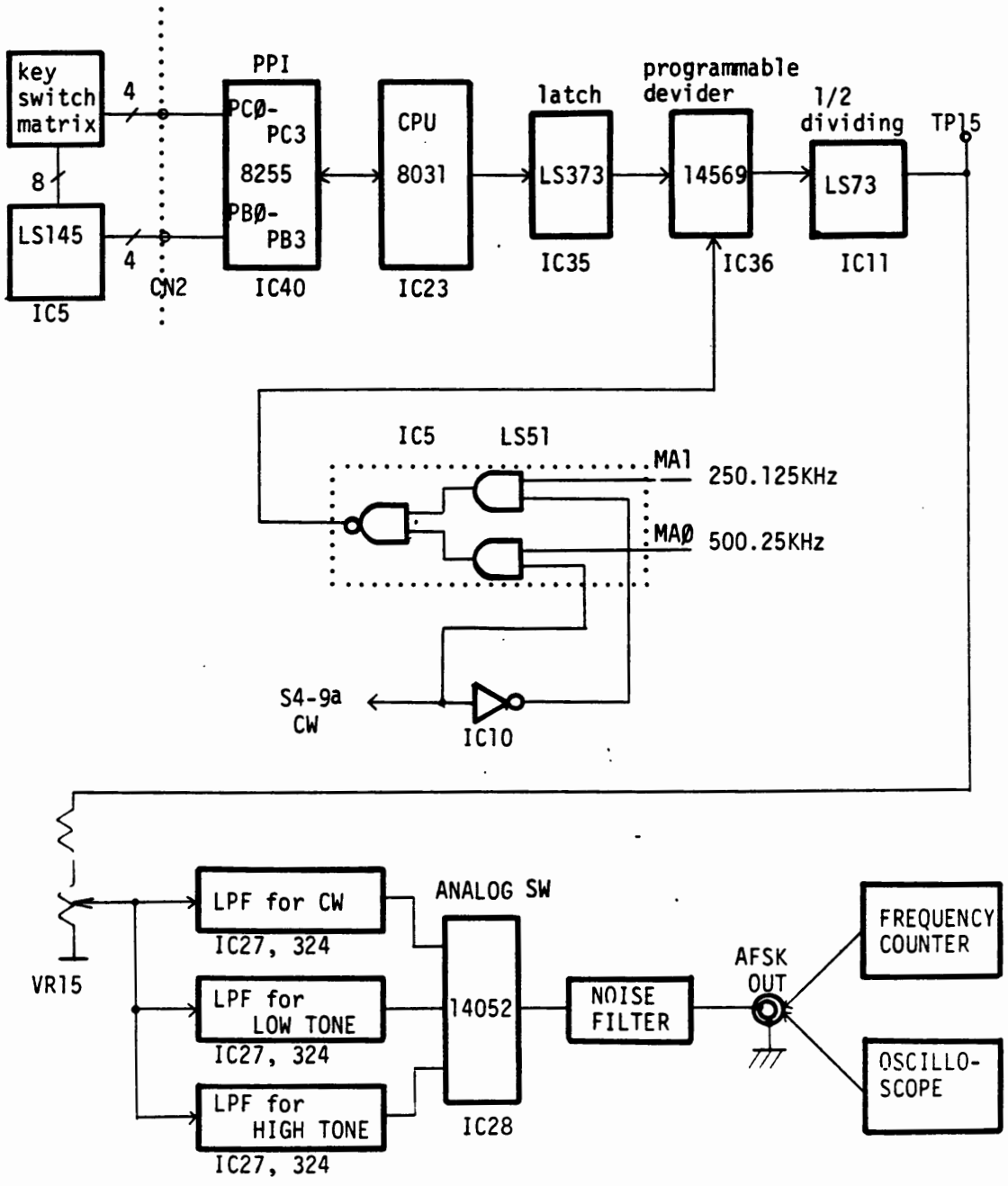


AC Voltage	AC Current	IC53, IC54 Input Voltage	IC53 Output	IC54 Output
115V	approx. 0.5A	approx. 22V (ripple under 2Vp-p)	4.8V - 5.2V	11.5V - 12.5V
220V	approx. 0.25A	approx. 21V (ripple under 2Vp-p)	4.8V - 5.2V	11.5V - 12.5V

[PROBLEMS]

Refer to the [PROBLEMS] in the "1.1 DC" section.

AFSK OUTPUT DIAGRAM



2. AFSK OUTPUT

Connect a frequency counter and an oscilloscope, or voltage meter (100mV) to the AFSK output terminal of the unit.
Set AFSK GAIN to maximum.
The output frequency should stay within +/- 1Hz of the frequencies as shown in the table below. The output level should be approx. 80mVpp.

MODE	TONE	SHIFT	SENSE	OUTPUT FREQUENCY
MORSE.E	--	---	OUT-R	828.2 Hz
TOR.B	--	---	OUT-N	1613.7 Hz
			OUT-R	1786.6 Hz
BAUDOT	L.T.	---	OUT-N	1276.1 Hz
		170	OUT-R	1445.8 Hz
		425	OUT-R	1701.5 Hz
		850	OUT-R	2119.7 Hz
	H.T.	---	OUT-N	2119.7 Hz
		170	OUT-R	2294.7 Hz
		425	OUT-R	2552.3 Hz
		850	OUT-R	2979.2 Hz

---: don't care

[PROBLEMS]

1. Accurate frequency is not obtained.

   1) System clock may not be set to 8.004MHz. ⟶ Check TP13.

   2) Either of IC35 (LS373), IC36 (14569) or IC5 (LS51) may be defective.

   3) The frequencies shown in above table are obtained, but the combination of MODE, TONE, SHIFT and SENSE is not corresponding to the table.

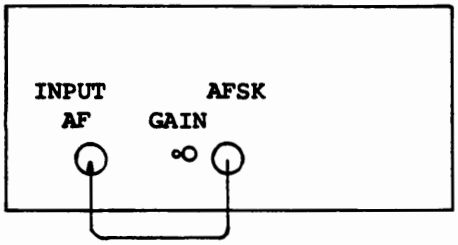
      Check PBØ-PB3 and PCØ-PC3 of IC40 (8255) to the keyboard switches on the front panel, and IC5 (LS145), D52, D53, D54, R213, R214 and the arounds.

2. No output

   1) Check IC5 (LS51), IC36 (14569), IC11 (LS73), IC27 (324), IC28 (14052) and the arounds.

   2) Check if there is any damage on VR15 (AFSK GAIN VOL).

3. DEMODULATOR



If no faults were found in AFSK output, connect AFSK output to the INPUT AF jack and get maximum gain.

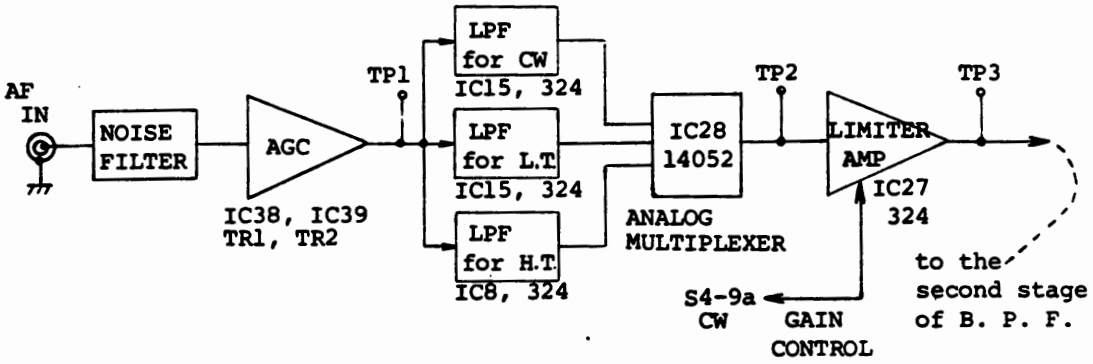
Table 3-1

MODE	TONE	SHIFT	SENSE	AFSK OUT Freq.	TP1	TP3	Test Point	VR to be adjusted
MORSE.E	——	——	OUT-R	828.2 Hz	2.2-2.5 Vpp	0.8-1.0Vpp	TP5 2.1-2.4Vpp	VR9
TOR.B	——	——	OUT-N	1613.7 Hz		1.3-1.4 Vpp	TP5 1.6-1.8Vpp	VR11
			OUT-R	1786.6 Hz			TP4 1.6-1.8Vpp	VR4
BAUDOT	L.T.	——	OUT-N	1276.1 Hz			TP5 1.6-1.8Vpp	VR10
		170	OUT-R	1445.8 Hz			TP4 1.6-1.8Vpp	VR1
		425	OUT-R	1701.5 Hz			TP4 1.6-1.8Vpp	VR2
		850	OUT-R	2119.7 Hz			TP4 1.6-1.8Vpp	VR3
	H.T.	——	OUT-N	2119.7 Hz			TP5 1.6-1.8Vpp	VR12
		170	OUT-R	2294.7 Hz			TP4 1.6-1.8Vpp	VR5
		425	OUT-R	2552.3 Hz			TP4 1.6-1.8Vpp	VR6
		850	OUT-R	2979.2 Hz			TP4 1.6-1.8Vpp	VR7

Setting of other switches: AF-IN, IN-N, SPEED=L.S., AFSK GAIN=MAX., FINE tuning vol.=center

NOTE) —— : DON'T CARE

3.1 AGC Circuit · The First Stage of Band Pass Filter



Change MODE, TONE, SHIFT and SENSE as shown in Table 3-1.
Amplitude of TP1 and TP3 should be as shown in Table 3-1.

[PROBLEMS]

1. No signal or too little signal is output from TP1.
   ⟶ Check IC38 (3301), IC39 (3301), TR1 (2SC536) and TR2 (2SC536), and check if the circuit is disconnected or short-circuit between the AF IN jack and TP1.

2. Excessive signal is output from TP1.
   ⟶ Check the feed back circuit between R6 and C8.

3. No signal or too little signal is output from TP3 regardless of MODE, TONE, SHIFT and SENSE.
   ⟶ Check IC28 (14052) if no signal is output into TP2.
   Check IC27 (324) if any signal is output into TP2.

4. No signal or too little signal is output from TP3 in a certain state of MODE, TONE, SHIFT and SENSE.
   ⟶ Check IC15 (324), IC8 (324) and IC28 (14052).

3.2 Adjustment of the second stage of Band Pass Filter

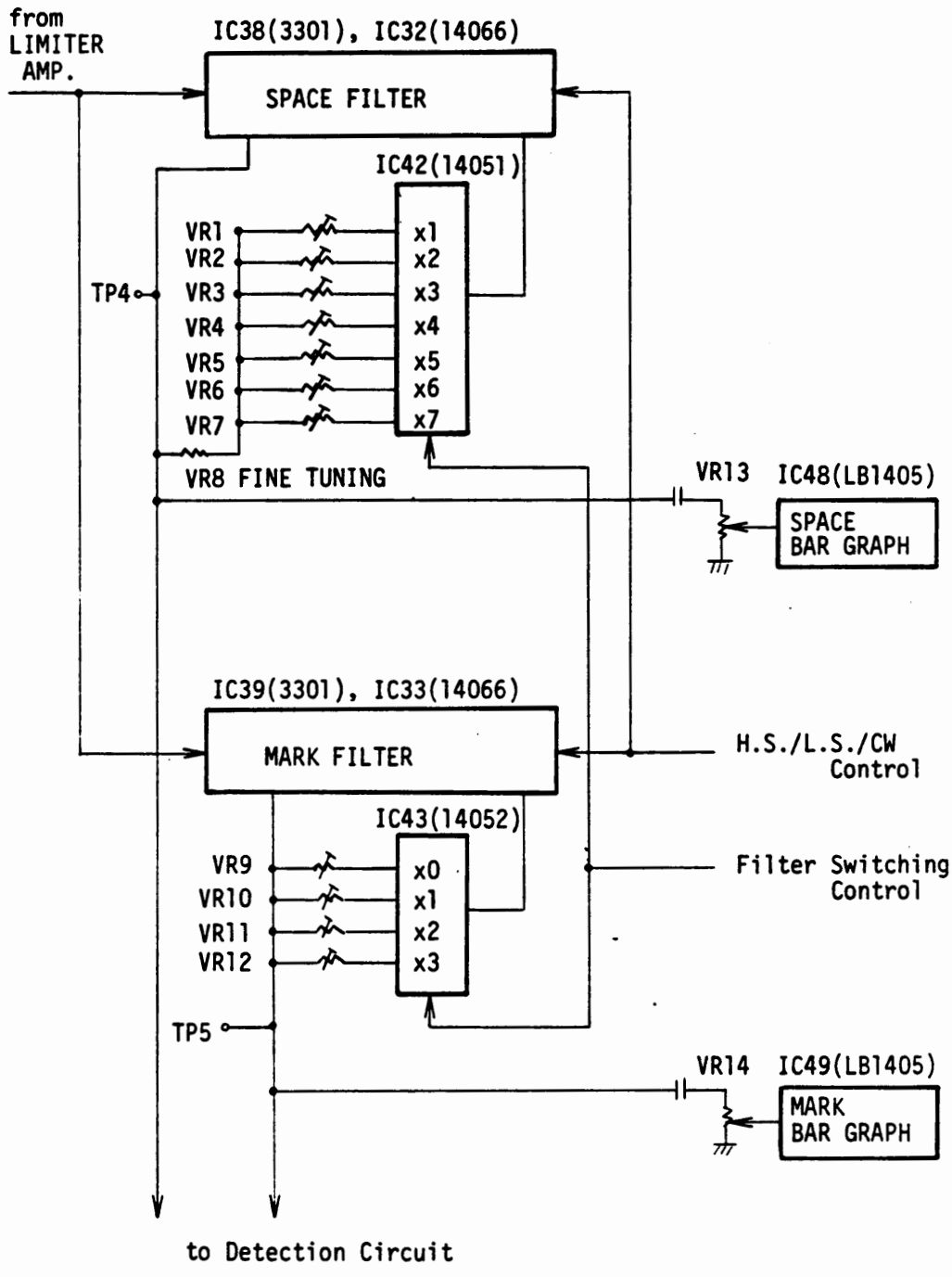


Table 3-2 Truth Value Table of Filter Switching Circuit

MODE	TONE	SHIFT	A(IC21, pin3)	B(IC21, pin11)	C(IC6, pin11)	a(IC13, pin11)	b(IC6, pin11)
MORSE.E MORSE.J	—	—	0	0	0	0	0
BAUDOT/TOR.C ASCII/JIS	L.T.	170	1	0	0	1	0
"	L.T.	425	0	1	0	1	0
"	L.T.	850	1	1	0	1	0
TOR.A TOR.B	—	—	0	0	1	0	1
BAUDOT/TOR.C ASCII/JIS	L.T.	170	1	0	1	1	1
"	L.T.	425	0	1	1	1	1
"	L.T.	850	1	1	1	1	1

NOTE: 0: Low Level 1: High Level

Change MODE, TONE, SHIFT and SENSE as shown in Table 3-1 and adjust corresponding trimmer potentiometer to get maximum output from TP4 and TP5. Maximum amplitude should be 1.6Vpp through 1.8Vpp.

[PROBLEMS]

1. No normal signal is output in spite normal signal is sent to SPACE filter, or the situation is incapable of adjustment.

   → 1) Check IC38 (3301), IC42 (14051), IC32 (14066), VR8 (FINE), the trimmer potentiometer corresponding to MODE, TONE and SHIFT which outputs no signal, and poor connection of CN2.

   2) Check if the output of "A", "B" and "C" in the filter switching circuit is corresponding to the Truth Value Table.

      NO Check IC21 (LS08), IC6 (LS00), IC19 (LS04), IC13 (LS32), MODE switch, TONE switch, SHIFT switch and CN2.

2. No normal signal is output in spite normal signal is sent to MARK filter, or the situation is incapable of adjustment.

→ 1) Check IC39 (3301), IC43 (14052), IC33 (14066) and the trimmer potentiometer corresponding to MODE and TONE which output no signal.

2) Check if the output of "a" and "b" in the filter switching circuit is corresponding to the Truth Value Table.

NO Check IC21 (LS08), IC6 (LS00), IC19 (LS04), IC13 (LS32), MODE switch, TONE switch, SHIFT switch and CN2.

3.3 Adjustment of BAR GRAPH

SPACE indicating BAR GRAPH

Set the unit in the following state: MODE=BAUDOT, TONE=L.T., SHIFT SHIFT=170, OUT-R, SPEED=L.S., AF-IN, IN-N, AFSK GAIN=MAX., FINE TUNING VOLUME=center.
Turn VR13 to minimum, then turn it clockwise gradually till the fifth LED lights.

MARK indicating BAR GRAPH

Set the unit in the following state: MODE=BAUDOT, TONE=L.T., OUT-N, SPEED=L.S., AF-IN, IN-N, AFSK GAIN=MAX.
Turn VR14 to minimum, then turn it clockwise gradually till the fifth LED lights.

[PROBLEM]

1. LED does not light to maximum for all proper signal is output to TP4 and TP5.

Check VR13, VR14, IC48 (LB1405), IC49 (LB1405) and CN2.

3.4 Detection Circuit

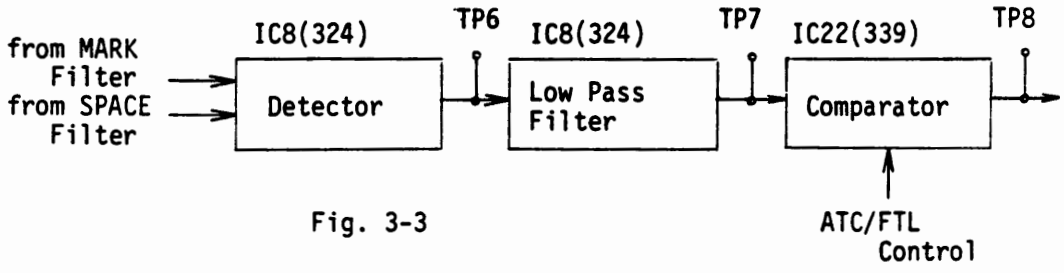


Fig. 3-3

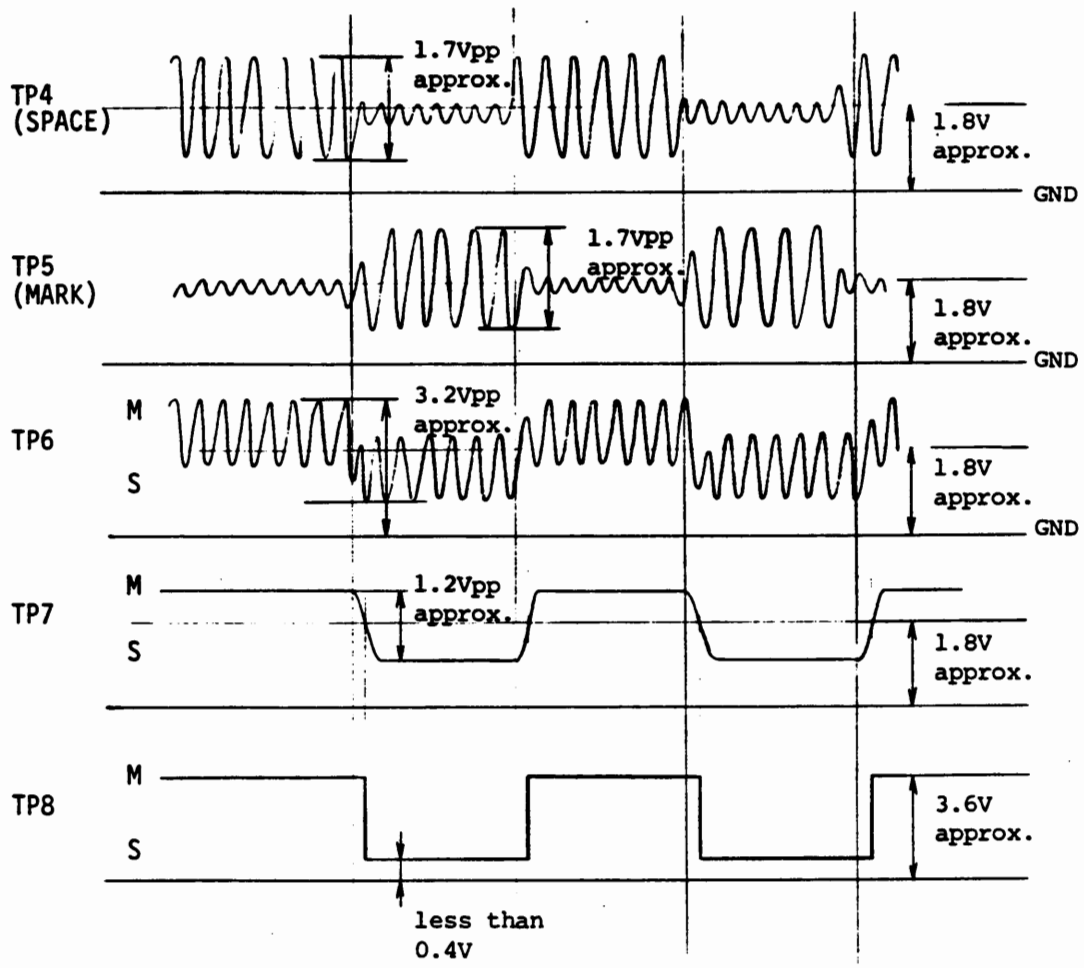


Fig. 3-4.

Set the unit in the following state: MODE=BAUDOT, TONE=L.T., SHIFT=170, SPEED=L.S., THRESHOLD=ATC.
Transmit "RY" test message repeatedly at 50 BPS by pressing "REPT" "Y".
Make sure that amplitude of TP6 through TP8 is as shown in Fig. 3-4.
Make sure that the waveform of TP6 through YP8 does not change even when the THRESHOLD control is changed to FTL.
Make sure that the waveform remains in normal when the state is changed to: SPEED=H.S., THRESHOLD=ATC, Baud Rate=200 BPS.

[PROBLEMS]

1. The waveform of TP6 is not normal. ⟶ Check D17 through D22 and IC8 (324).
2. The waveform of TP7 is not normal. ⟶ Check IC7 (14066) and IC8 (324).
3. The waveform of TP8 is not normal. ⟶ Check D23, D24, D25, IC7 (14066) and IC22 (324).

4. The waveform does not remain in normal when the speed setting is changed to 200 BPS. ⟶ Check IC7 (14066), IC14 (LS02), CN2, S5-6a, IC32 (14066) and IC33 (14066).

NOTE: It is recommended to compare the waveform with normal one by using two-channel oscilloscope, for it is very difficult to judge singly whether the waveform is normal or not.

3.5 ANTI-NOISE Switching, AF-TTL Switching, Input Polarity Switching Circuit

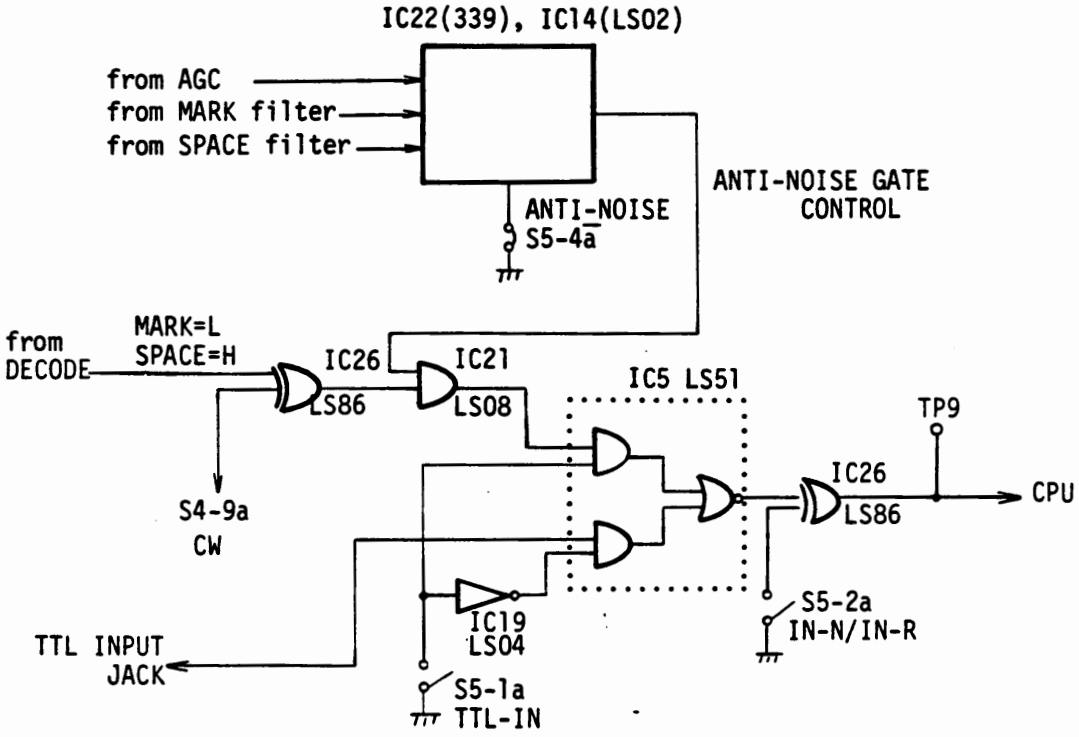


Fig. 3-5

Level of TP9

Polarity / Code	IN-N	IN-R
CW	MARK =L SPACE=H	H L
Otner Codes	MARK =H SPACE=L	L H

The ANTI-NOISE circuit works in the state of A.N.=ON to open the GATE when the input signal from MARK FILTER or SPACE FILTER is larger than the one from AGC. Set the unit as follows: MODE=BAUDOT, SPEED =L.S., TONE=L.T., SHIFT=850, A.N.=ON, AF-IN. Make connection between INPUT AF and the variable audio generator.
Increase the frequency of the audio generator from around 800 Hz to make sure that the 1 pin level of IC22 (339) decreases from approx. 5V to 0V when the output level of TP5 becomes 1.1 - 1.2V.
Increase the frequency furthermore to make sure that the output level of TP5 becomes 1.0 - 1.1V when the frequency becomes higher than 1275 Hz and that the 1 pin level of IC22 increases from 0V to approx. 5V.
Make sure that if the state is changed to A.N.=OFF when the 1 pin level of IC22 is approx. 5V, the level decreases to 0V.
The TP9 level corresponding to MARK and SPACE is as shown in Fig. 3-5.

[PROBLEMS]

1. ANTI NOISE circuit does not open.

   Check IC22 (339), IC14 (LS02) and IC21 (LS08).

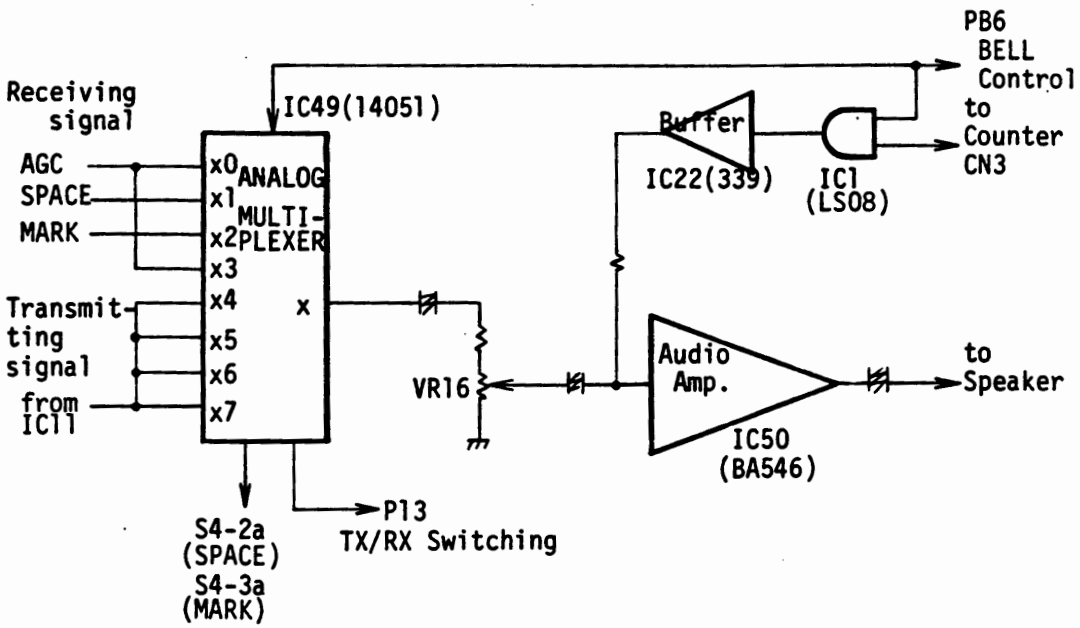
2. ANTI NOISE circuit is left opened.

   Check IC22 (339), IC14 (LS02) and S5-4a.

3. The polarity of the input signal does not reverse.

   Check IC26 (LS86), S5-2a and CN2.

4. AUDIO MONITOR CIRCUIT



The input signal sound being monitored is switched by S4-2a and S4-3a.
The input/output signal sound is switched by P13.
It is controlled by PB6 to inject the bell sound into the audio monitor circuit.

[PROBLEMS]

1. No sound or too small sound is heard.
   ⟶ Check IC50 (BA546), VR16, the speaker, J8, CN9 and S1d.

2. Only a certain sound is heard.
   ⟶ Check IC49 (14051), CN2, S4-2a and S4-3a.

3. No bell sound is heard.
   ⟶ Check IC22 (339) and IC1 (LS08).

5. RESET, BATTERY-BACK-UP CIRCUIT

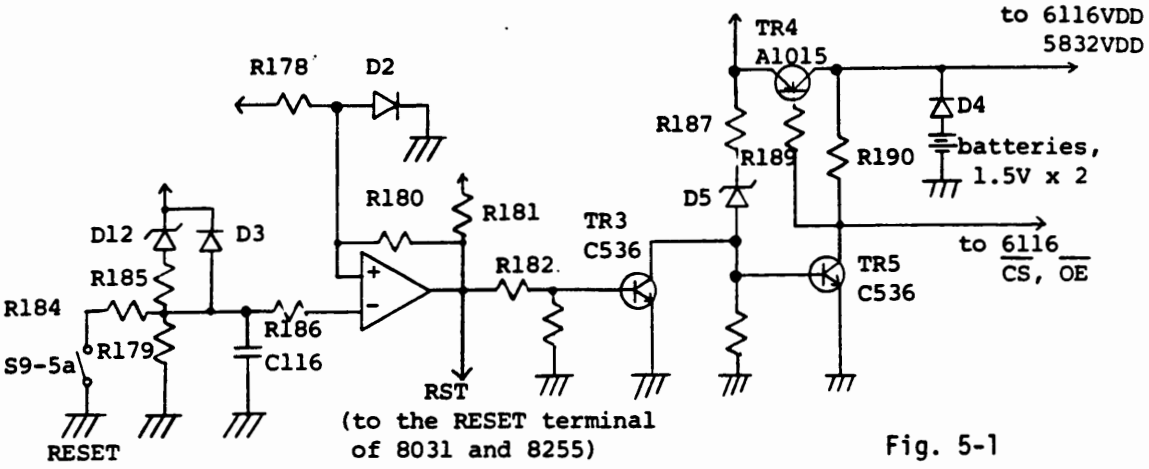


Fig. 5-1

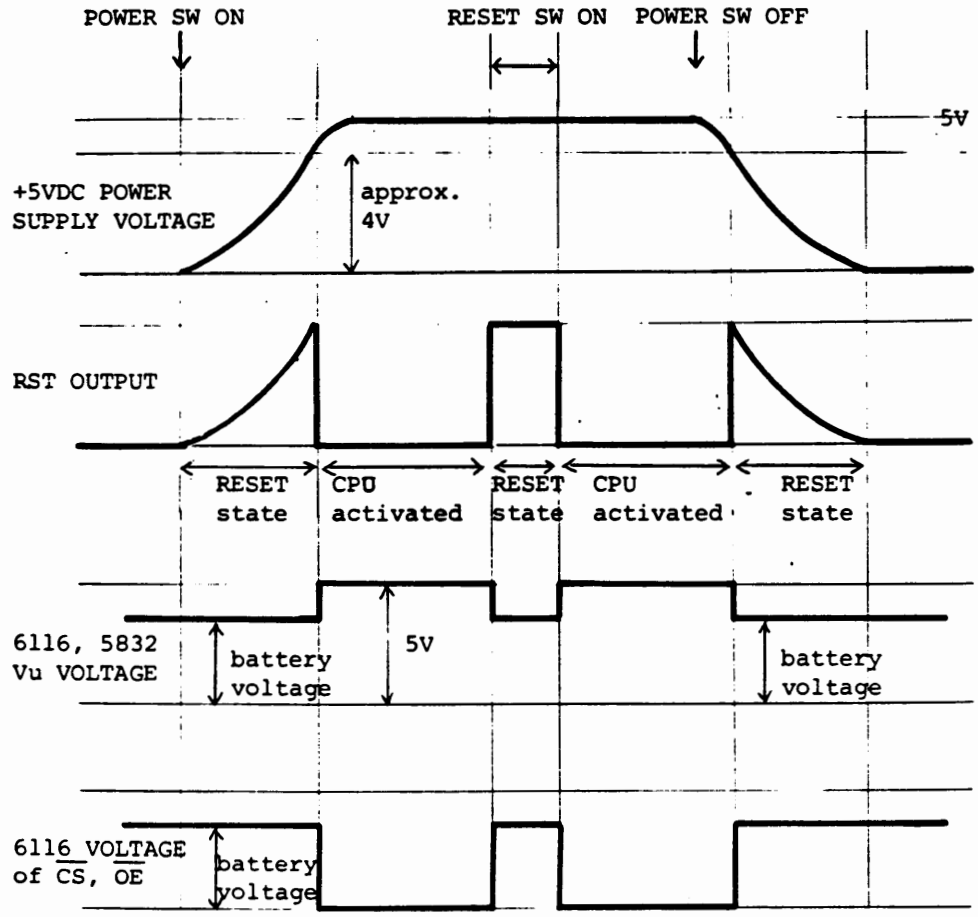


Fig. 5-2

As shown in Fig. 5-2, when the RESET switch is pressed or when POWER ON/OFF, the reset circuit generates a reset pulse and the battery-back-up circuit switches the Vdd of IC31 (6116) and IC46 (5832) between the +5VDC main power supply and batteries, and at the same time generates high level voltage against $\overline{CS}$ and $\overline{OE}$ of IC31 (6116) in order not to be chip-selected.

[PROBLEMS]

1. When power is turned on, no reset function is activated and CPU runs away.

   ↓

   The capacity of C116 may be deficient, IC22 (339) may be defective, check D2, D3 and D12.

2. When power is turned on, the reset function is activated properly, but no reset function is activated when the RESET button is pressed.

   ↓

   Check from S9-5a (RESET button) to R184 through CN2.

3. Memorized date is cleared. Check the battery voltage, check TR3, TR4, TR5, D4 and D5.

6. FULL KEYBOARD

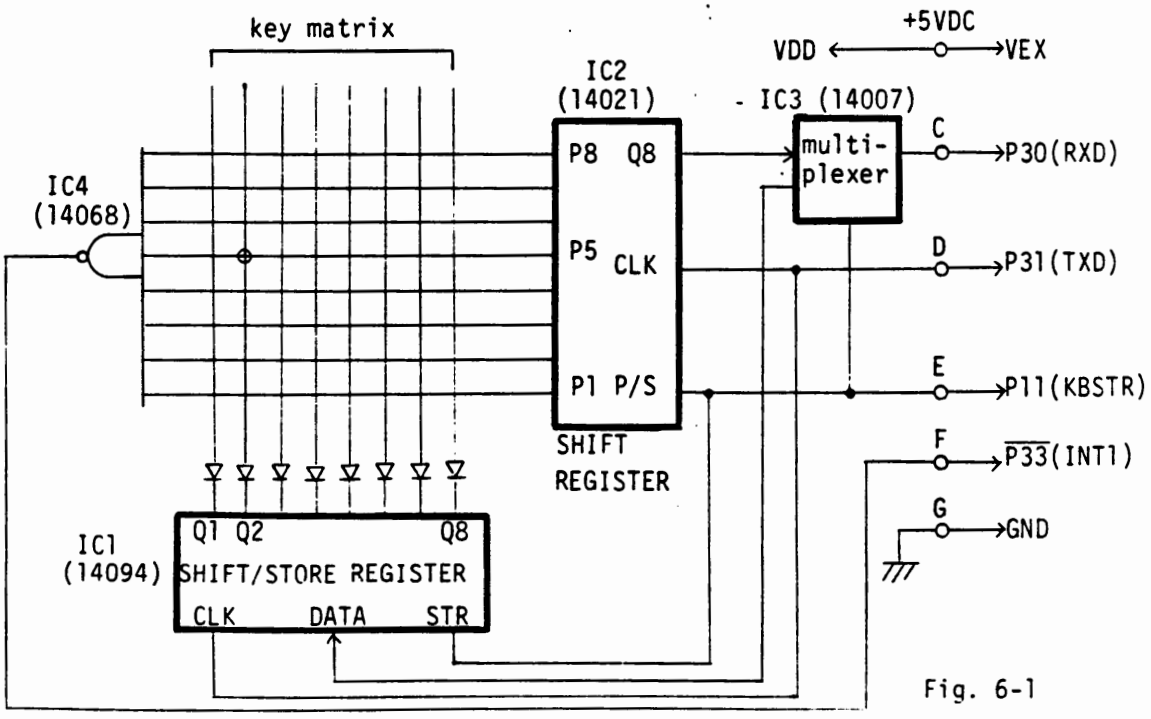
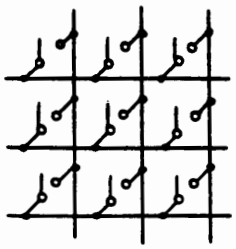


Fig. 6-1



key matrix

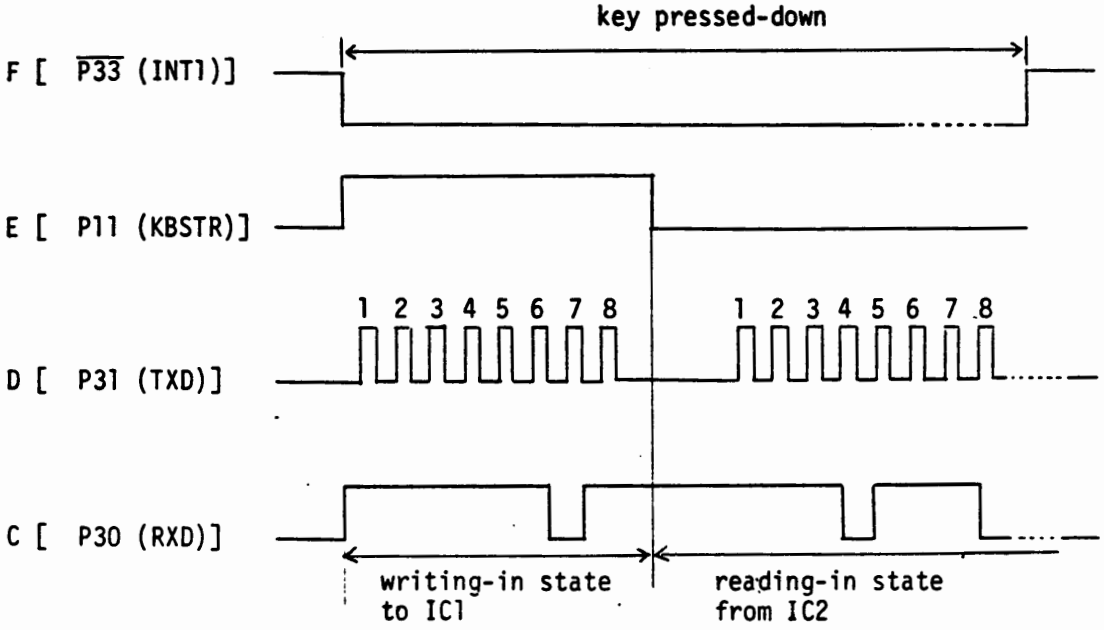


Fig. 6-2 Full Keyboard Timing
(The detecting timing when the °marked key in Fig. 6-1 is pressed down.)

When the keys are not pressed down, every output from IC1 is set to L level and the full keyboard is stopping its keyboard scan. Any keystroke is detected by IC4 (14068) and starts the keyboard scan.

- P11 (KBSTR) is set to H level to enable programming in IC1 (14094).
- The data which is to be programmed in Q8 is set to P30.
- One clock pulse is generated from P31 and IC2 is shifted.
- The same procedure is repeated eight times as shown in the figure to set date to Q1-Q8.

- P11 is set to L level to enable reading-out from IC2 (14021).
- The data sent to Q8 with CPU.
- One clock pulse is generated from P31 and IC2 is shifted.
- The next data is output to Q8.
- The same procedure is repeated eight times to read every data from P1-P8 with CPU.

[PROBLEMS]

1. No keying accepted

   1) The keyboard cable may be disconnected or check if CN6 is defective of contact.

   2) Check IC1 (14094), IC2 (14021), IC3 (14007) and IC4 (14068) on the keyboard PCB.

   3) Check P30, P31, P33 and P11 of the CPU (8031), and also IC19 (LS04).

2. The keying of a specified group of keys is not accepted.

   ↓

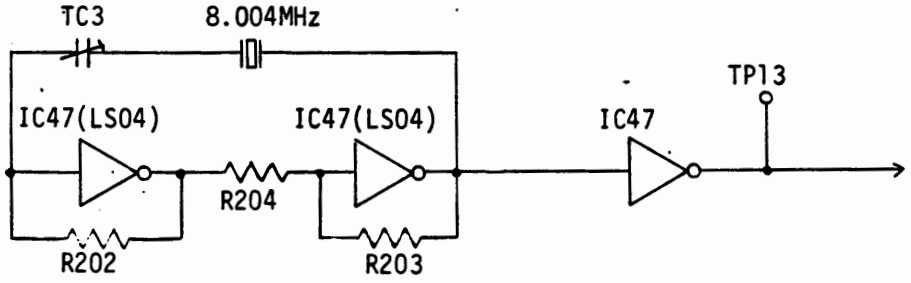
   Check IC1 (14094), IC2 (14021), D1-D8, IC4 (14068) and R9.

3. The keying of a specified key is not accepted.

   ↓

   The key-switch may be defective.

7. SYSTEM CLOCK OSCILLATION CIRCUIT



After warming up the unit, the output frequency of TP13 should stay within 8004.000KHz +/- 0.050KHz. If not, adjust TC3 to make it stay within the range.

[PROBLEMS]

1. Frequency error ——→ Re-adjust with TC3.

2. No oscillation. ——→ Check IC47 (LS04), crystal oscillator and trimmer capacitor TC3.

8. CPU AND THE AROUNDS

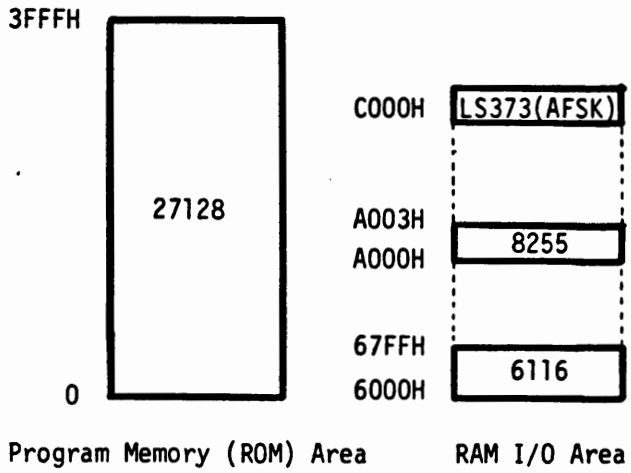


Fig. 8-1 Memory Map

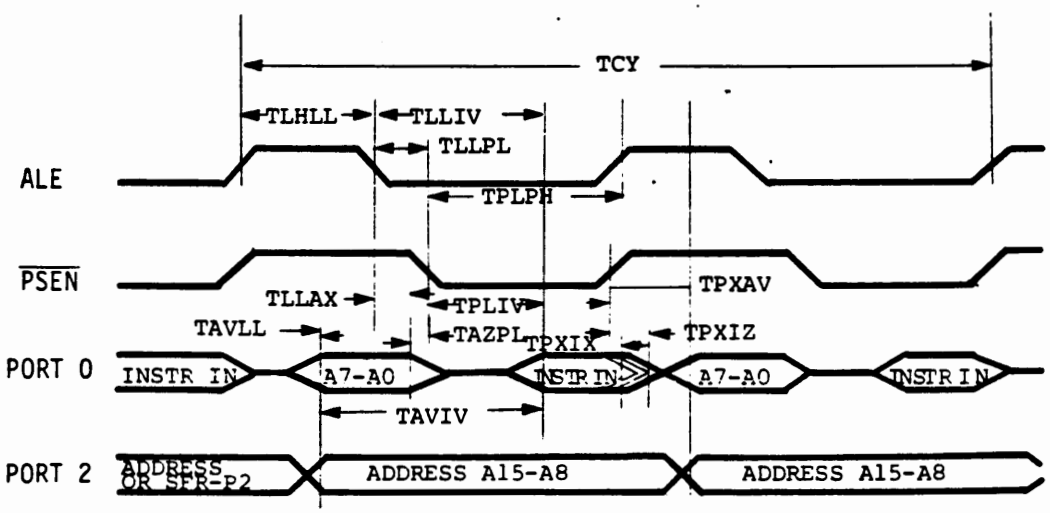


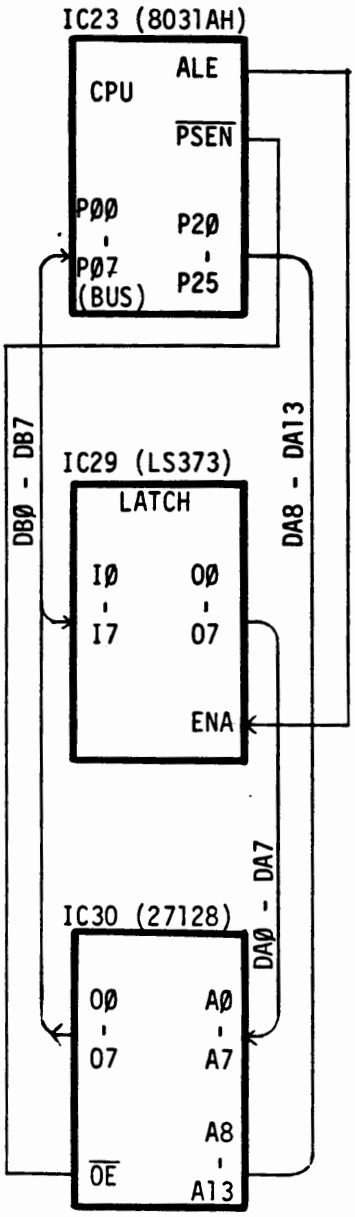
Fig. 8-2 Program Memory Read Cycle Wave Forms

PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TLHLL	ALE pulse Width	127		ns	2TCLCL-40		ns
TAVLL	Address Setup to ALE	53		ns	TCLCL-30		ns
TLLAX1	Address Hold After ALE	48		ns	TCLCL-35		ns
TLLIV	ALE To Valid Instr In		233	ns		4TCLCL-100	
TLLPL	ALE To $\overline{PSEN}$	58		ns	TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		ns	3TCLCL-35		ns
TPLIV	$\overline{PSEN}$ To Valid Instr In		125	ns		3TCLCL-125	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns	0		ns
TPXIZ[1]	Input Instr Float After $\overline{PSEN}$		63	ns		TCLCL-20	ns
TPXAV[1]	Address Valid After $\overline{PSEN}$	75		ns	TCLCL-8		ns
TAVIV	Address To Valid Instr In		302	ns		5TCLCL-115	ns
TAZPL	Address Float To $\overline{PSEN}$	0		ns	0		ns

NOTE:

1. Interfacing the 8051AH to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.
2. TCLCL=Ocsillator Period.



Port Ø of CPU 8031AH is an 8-bit open drain bidirectional I/O port, and also is a multiplexed low-order address and a data bus as shown in the waveform of Fig. 8-4.

Port 2 is an 8-bit quasi-bidirectional I/O port which emits a high-order address.

ALE provides the Address Latch Enable output which is to be used to latch a low-order address to external memory.

$\overline{\text{PSEN}}$ (Program Store Enable Output) is a control signal which enables external memory to bus during the external fetch operations.

IC29 (LS373) is used as a low-order latch, which provides the low-order address to IC30 (27128), IC40 (8255) and IC31 (6116) through multiplexer during normal operation.

[PROBLEMS]

1. CPU doesn't work at all.
   1) Check the system clock circuit.
   2) Check IC29 (LS373) and IC23 (8031AH).
2. CPU runs away.
   1) Check the system clock circuit and the reset circuit.
   2) Check IC23 (8031AH), IC29 (LS373) and IC30 (27128).

8-2 RAM

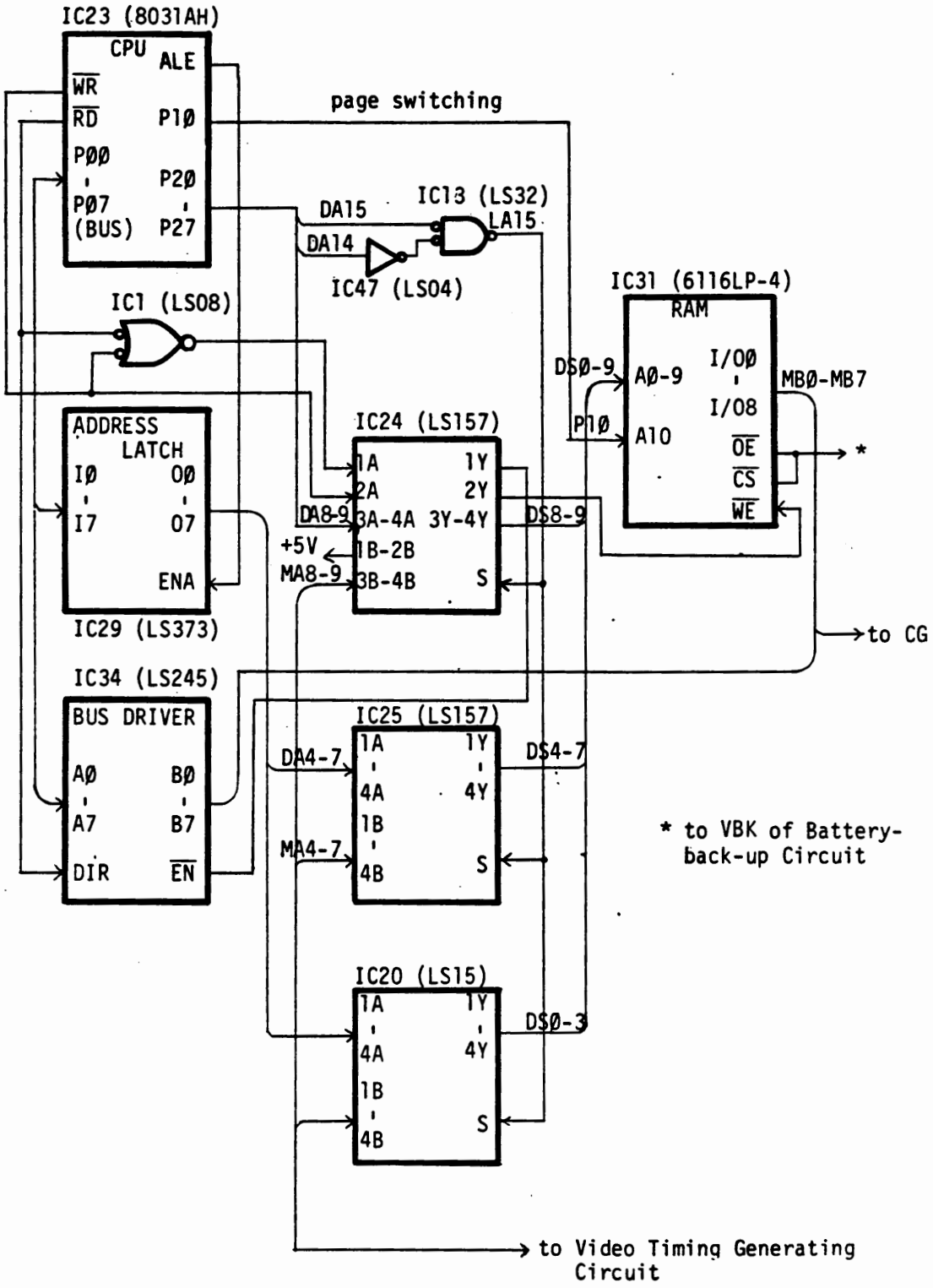

IC23 (8031AH)
CPU
ALE
WR
RD
P10
P00
P20
P07
(BUS)
P27
page switching
DA15
IC13 (LS32)
LA15
DA14
IC47 (LS04)
IC1 (LS08)
IC31 (6116LP-4)
RAM
DS0-9
A0-9
I/O0
I/O8
MB0-MB7
P10
A10
OE
CS
WE
*
ADDRESS
LATCH
I0
O0
I7
O7
ENA
IC24 (LS157)
1A
1Y
2A
2Y
DA8-9
3A-4A
3Y-4Y
DS8-9
+5V
1B-2B
MA8-9
3B-4B
S
IC29 (LS373)
to CG
IC34 (LS245)
BUS DRIVER
A0
B0
A7
B7
DIR
EN
IC25 (LS157)
DA4-7
DS4-7
4A
4Y
1B
MA4-7
4B
S
* to VBK of Battery-back-up Circuit
IC20 (LS15)
DS0-3
to Video Timing Generating Circuit

Fig. 8-3

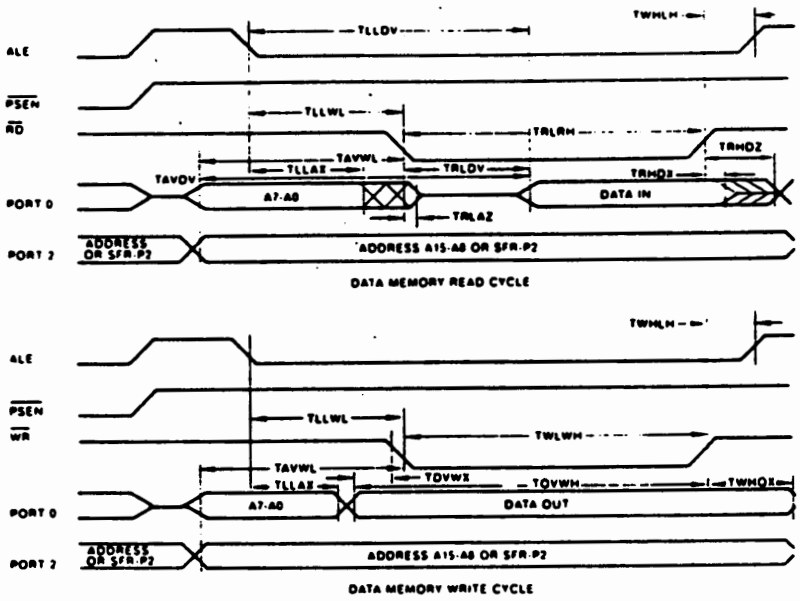


Fig. 8-4

EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TRLRH	$\overline{RD}$ Pulse Width	400		ns	6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		ns	6TCLCL-100		ns
TLLAX2	Address Hold After ALE	132		ns	2TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In		250	ns		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		ns	0		ns
TRHDZ	Data Float After $\overline{RD}$		97	ns		2TCLCL-70	ns
TLLDV	ALE To Valid Data In		517	ns		8TCLCL-150	ns
TAVDV	Address To Valid Data In		585	ns		9TCLCL-165	ns
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	200	300	ns	3TCLCL-50	3TCLCL+50	ns
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	203		ns	4TCLCL-130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	43	123	ns	TCLCL-40	TCLCL+40	ns
TDVWX	Data Valid To $\overline{WR}$ Transition	0		ns	0		ns
TQVWH	Data Setup Before $\overline{WR}$	433		ns	7TCLCL-150		ns
TWHQX	Data Hold After $\overline{WR}$	33		ns	TCLCL-50		ns
TRLAZ	Address Float After $\overline{RD}$		0	ns		0	ns

The external RAM IC31, 6116LP-4 is a battery-back-up video RAM. When nothing is wrote-in/read-in from CPU, it is separated from CPU by bus driver IC34 (LS245) and multiplexer IC's 20, 24, 25 (LS157) to be directly accessed by the video timing generating circuit.
When addresses 6000H-67FFH are sent from CPU, each LS157 selects addresses on the CPU side. While $\overline{WR}$ pulse or $\overline{RD}$ pulse is sent, $\overline{EN}$ of LS245 is set to L level and PØ (BUS) of CPU is connected to the I/O port of 6116LP-4 so that 6116LP-4 can be accessed from CPU. The output of P1Ø from CPU switches page-1/page-2 of the screen.

[PROBLEMS]

1. Random characters are displayed on the screen but the function parameter or the characters typed in from the keyboard are not displayed properly.

   1) Check IC20 (LS157), IC24 (LS157), IC25 (LS157), IC1 (LS08), IC13 (LS32) and IC47 (LS04).

   2) Check IC34 (LS245).

   3) Check IC31 (6116LP-4).

2. Text in the battery-back-up memory is damaged.

   1) Check the batteries.

   2) Check the battery-back-up circuit and the reset circuit.

8-3 Interface

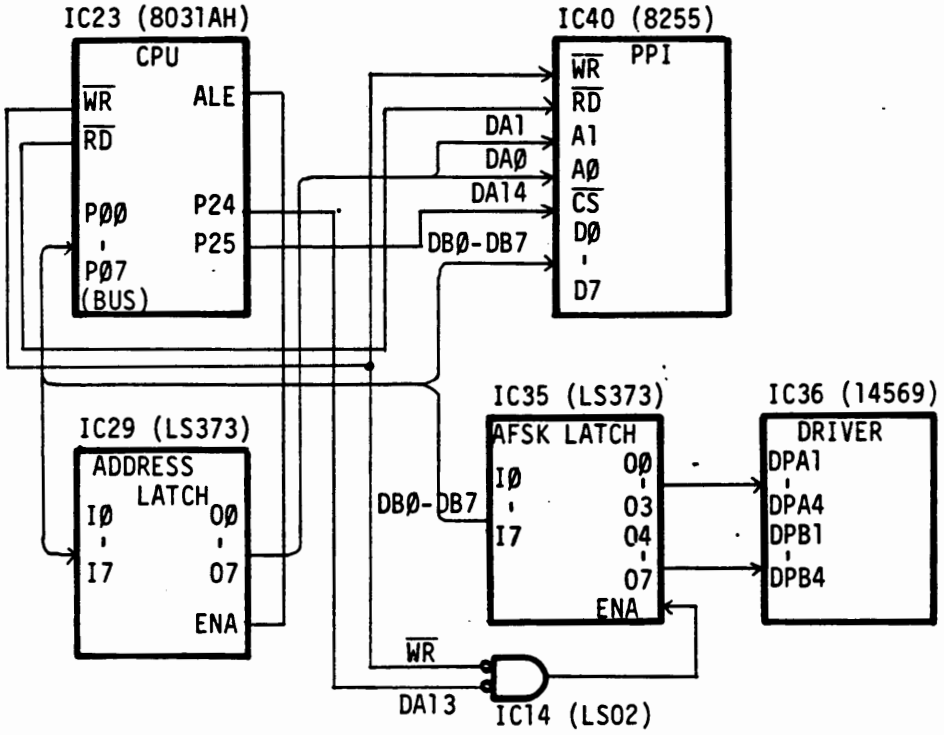
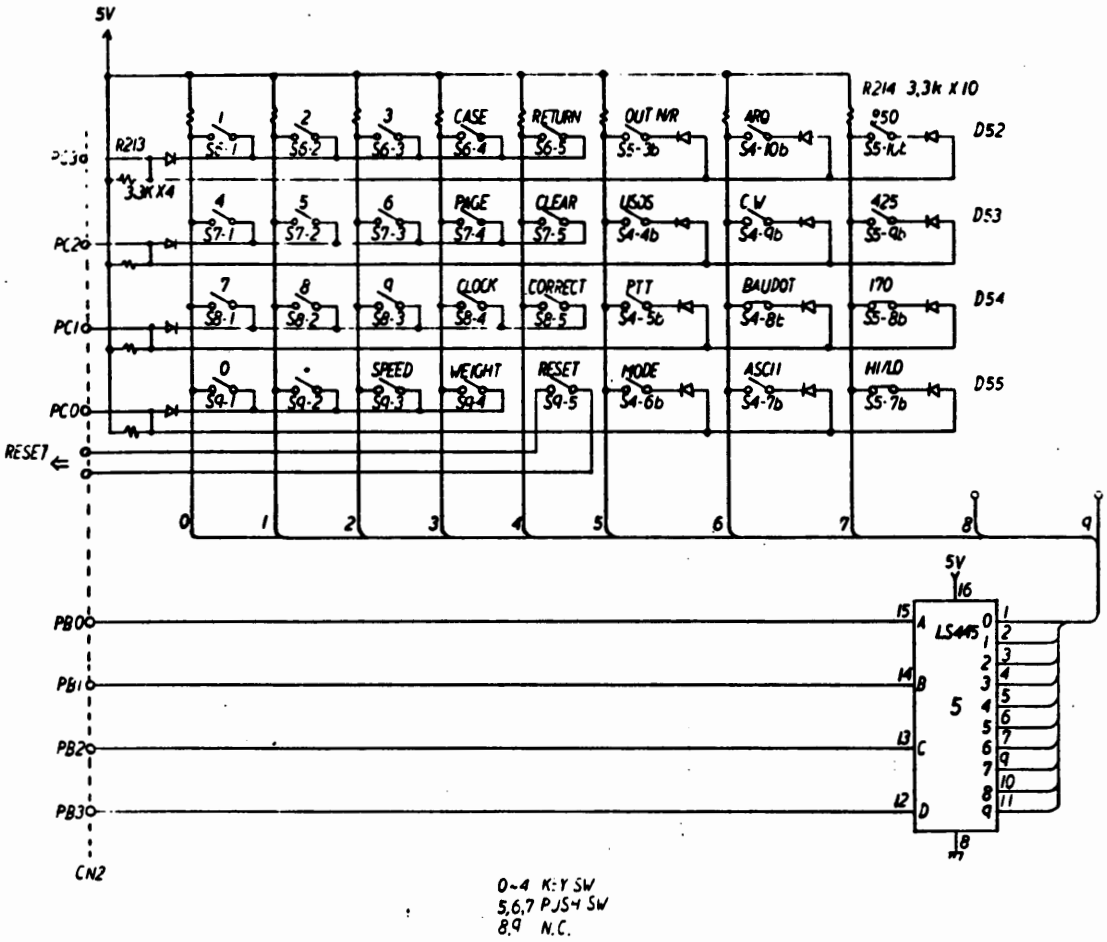


Fig. 8-5

IC40 (8255) is a programmable peripheral interface. When CPU outputs address 0A000H-0A003H, 8255 becomes to be accessed, and the writing data in 8255 from CPU or reading data in CPU from 8255 is enabled. The waveform is the same as shown in Fig. 8-4.
IC35 (LS373) is a latch to memorize the dividing ratio for the AFSK generator. When CPU outputs 0C000H address to enable the writing-in ($\overline{WR}$ pulse is sent), IC14 (LS02) becomes select status and the data from CPU is latched to IC35 (LS373).

9. FRONT PANEL KEYBOARD, SWITCH BOARD



The pressing of the key switches and push buttons on the front panel is read in CPU through the same circuit by scanning. PBØ-PB3 of 8255 outputs the number of a line which has a key desired to be read-in by BCD, which is decoded by IC5 (LS145 or LS445). The level of the line is set to L level and the rest to H level. In this case, the reading-in of PCØ-PC3 enables CPU to see the state of the line. If any one key is pressed then, either of PCØ-PC3 which is on the same line with the pressed key set to L level and the others to H level.

[PROBLEMS]

1. The keystroke of a specific key or switch is not read-in. → Check the key or switch. and Check D52-D55.

2. The keystroke of a specific group of keys or switches is not read-in. → Check IC5 (LS145), D52-D55, PBØ-PB3 and PCØ-PC3 of IC40 (8255).

3. No keystroke of any keys or switches is read-in. → Check IC5 (LS145) and IC40 (8255).

   Check if CN2 is defective of contact.

10. CLOCK

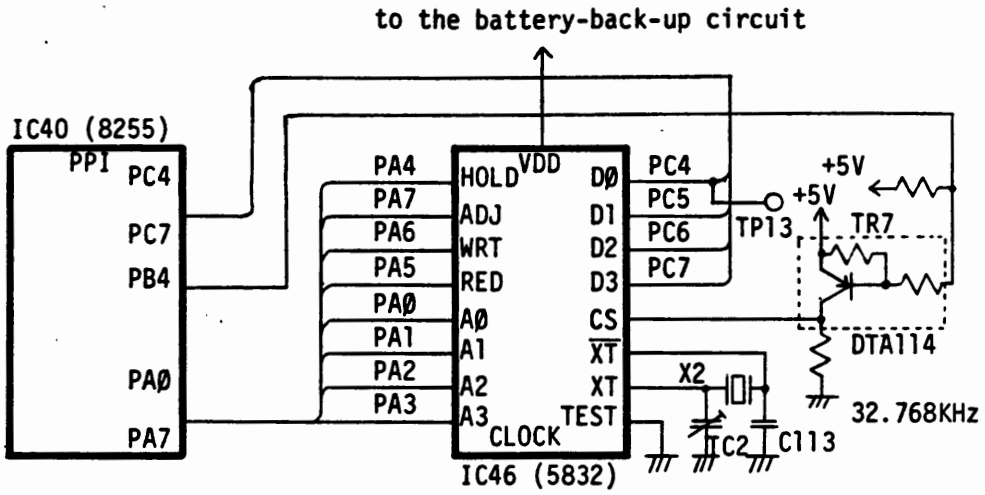


Fig. 10-1 Real Time Clock

The real time clock IC46 (5832) is backed up by batteries so that works even when the main power source is turned off. IC46 is controlled by IC40 (8255). The function table of IC46 (5832) is as shown in Fig. 10-1. When the RESET button is pressed, each port of IC40 (8255) becomes in high impedance state and TR7 (DTA114) becomes OFF state. Thus CS of IC46 becomes Low level and in disselect state, so the data in IC46 is protected.
The gaining or losing time of the clock can be adjusted with TC2. For the adjustment, follow the procedure below;

1) Input **CLOCK** + . + **FUNC** from the front panel to give the 1024Hz output to TP18.
2) Connect a frequency counter of high accuracy to adjust TC2 to get TP18 precisely at 1024Hz.

Address Input				Internal Counter	Data I/O				Count Value	
A0	A1	A2	A3		D0	D1	D2	D3		
0	0	0	0	S1	*	*	*	*	0 - 9	S1 and S10 enable WRITE to zero regardless to input data of D0-D3 when WRITE is enabled by selecting the address. READ is enabled by the or inary operation.
1	0	0	0	S10	*	*	*	*	0 - 5	
0	1	0	0	MI1	*	*	*	*	0 - 9	
1	1	0	0	MI10	*	*	*		0 - 5	
0	0	1	0	H1	*	*	*	*	0 - 9	
1	0	1	0	H10	*	*	°	°	0 - 1 / 0 - 2	D2=P.M. by "H", D2=A.M. by "L" D3=total 24 hours by "H" D3=total 12 hours by "L"
0	1	1	0	W	*	*	*		0 - 6	
1	1	1	0	D1	*	*	*	*	0 - 9	
0	0	0	1	D10	*	*	°		0 - 3	D2=leap year by "H", 29 days for February D2=28 days for February by "L"
1	0	0	1	MO1	*	*	*	*	0 - 9	
0	1	0	1	MO10	*				0 - 1	
1	1	0	1	Y1	*	*	*	*	0 - 9	
0	0	1	1	Y10	*	*	*	*	0 - 9	

NOTES: 1 When a leap year is set, the setting is canceled after the 29th of February is over.

2 Regarding D0-D3,

1) * = 0 or 1

2) ° = AM/PM, 12-hours/24-hours, a bit (0 or 1) for a leap year

3) blank column = no bit

[PROBLEMS]

1. Not set as instructed from the keyboard, or no display of correct numerical value.

↓

Check PAØ-PA7, PB4 and PC4-PC7 of IC40 (8255).
Check IC46 (5832) and TR7 (DTA114).

2. The display of time doesn't go forward.

↓

Check IC46, TC2 and X2.

↑

3. No adjustment of gaining/losing time available.

11. PRINTER PORT

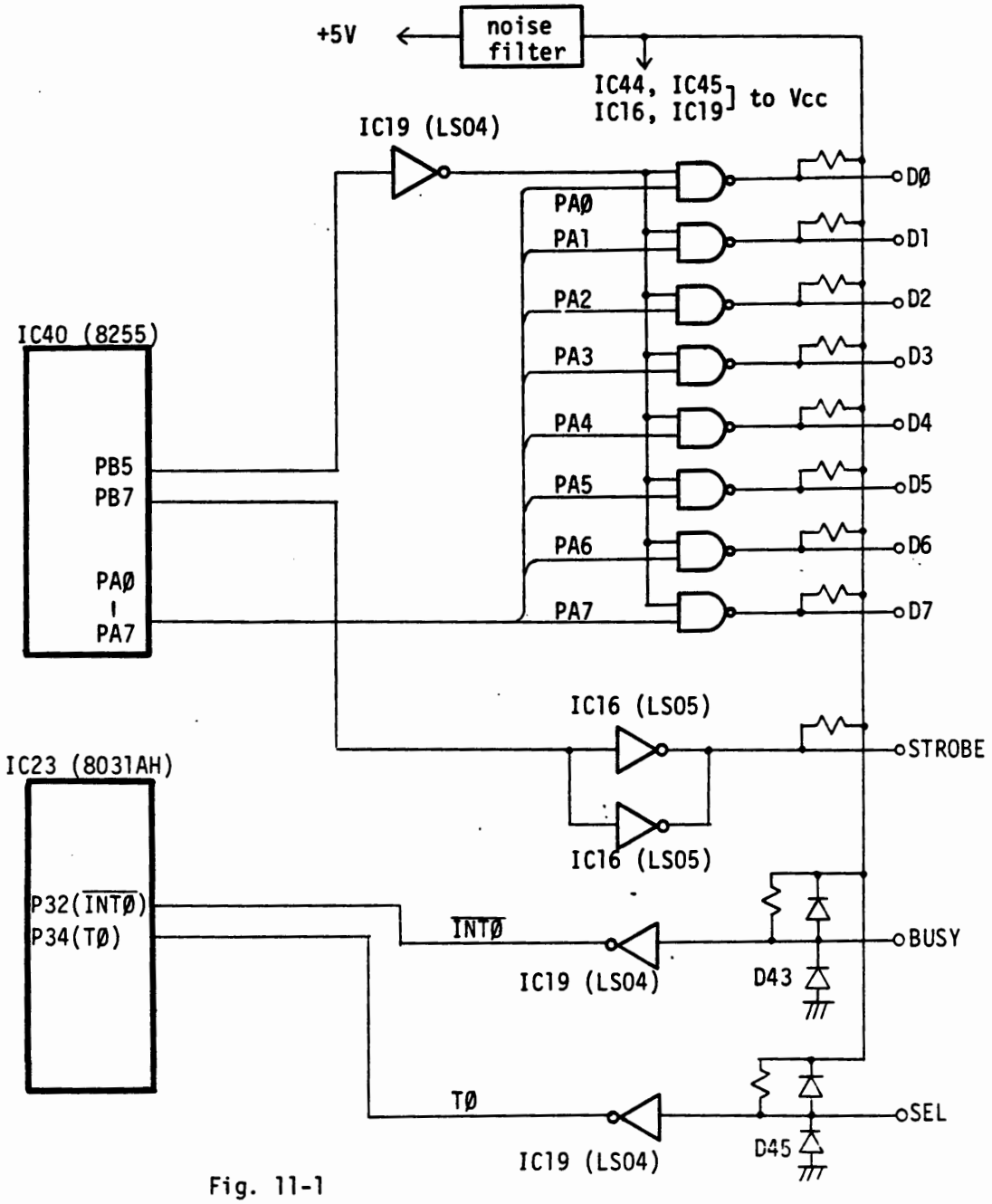


Fig. 11-1

The power source for IC44 (LS03), IC45 (LS03), IC16 (LS05) and IC19 (LS04) used as the input/output buffer of the printer port is provided with power through a noise filter to keep the spurious radiation at low rate. As PAØ-PA7 of IC40 (8255) are used to control the real time clock IC46 (5832), PB5 of IC40 controls the gate of IC44 and IC45 not to output unnecessary data to DØ-D7. Only the STROBE output is designed to be the parallel output of LS05 to increase the fan out, since usually the pull-up resistor of STROBE input of a printer is small.

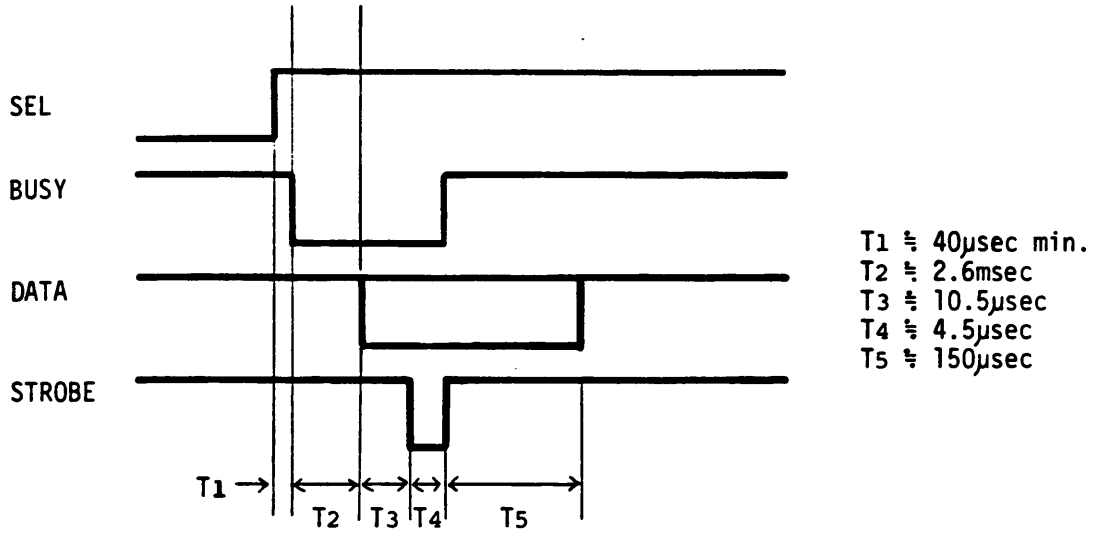


Fig. 11-2 Printer Port Timing

[PROBLEMS]

1. Misprints characters though the electric characteristic and the timing of the printer interface is compatible.

   ↓

   Check IC40 (8255), IC44 (LS03) and IC45 (LS03).
   Check if CN4 is defective of contact.

2. No printing of characters though the electric characteristic and the timing of the printer interface is compatible.

   ↓

   Check if the BUSY signal and the SELECT signal are correctly conveyed
   from BUSY (no. 21 pin of CN4) to P32 of CPU (no. 12 pin, $\overline{INT\emptyset}$),
   from SEL (no. 25 pin of CN4) to P34 of CPU (no. 14 pin, $\overline{T\emptyset}$)
   respectively.

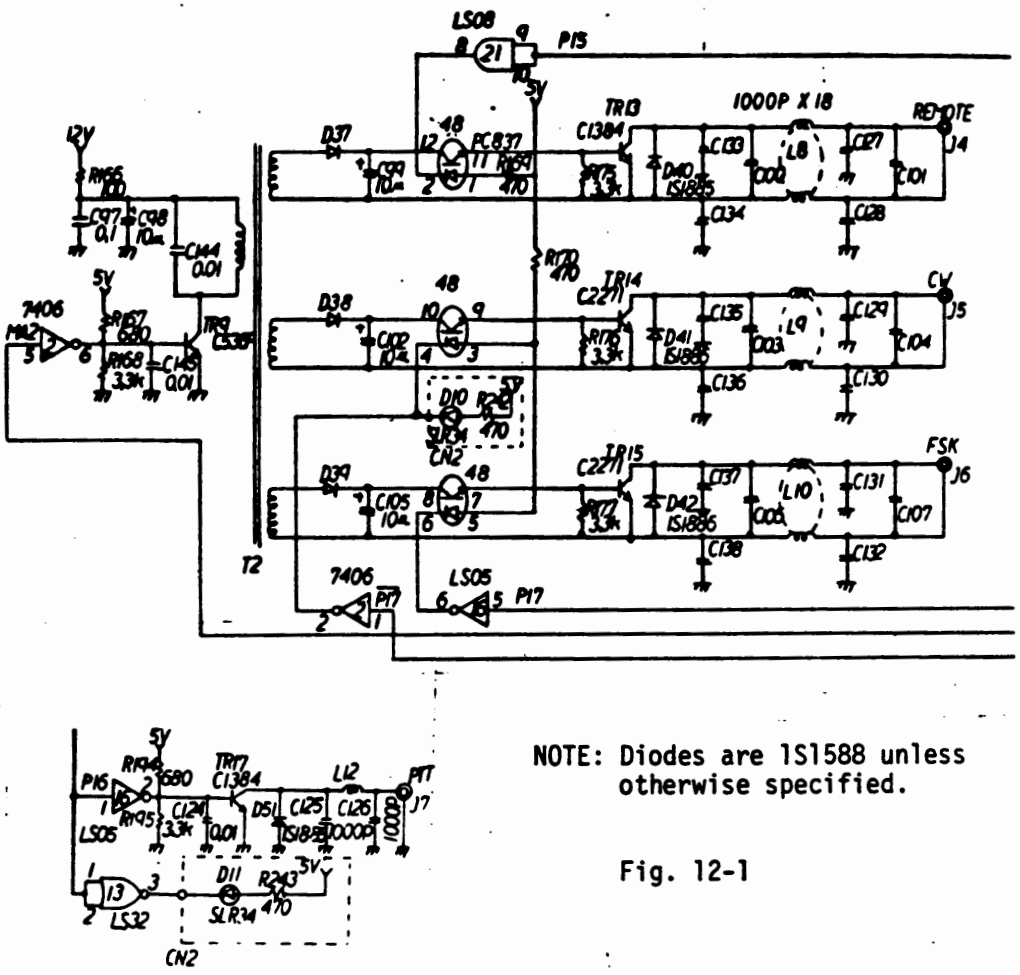
   -Check IC19 (LS05)-

   Check if the STROBE pulse is emitted .

   -Check IC16 (LS05) and IC40 (8255)-

   Check if the data is sent. ——— -Check IC44 (LS03), IC45 (LS03), IC19 (LS04) and IC40 (8255)-

12. KEYING CIRCUIT



NOTE: Diodes are 1S1588 unless otherwise specified.

Fig. 12-1

The keying circuits of REMOTE, CW and FSK are floated by the optoisolator over the ground. The power is supplied to each photo transistor through the secondary winding of T2. T2 is driven by TR9 (2SC536) at 125 KHz. The PTT keying circuit works only when plus voltage is added, for the circuit uses emitter grounded NPN transistor: 2SC1384 of TR17.

[PROBLEMS]

1. A certain cercuit among REMOTE, CW and FSK circuits does not work.

   Check the following components of the circuit not working: Keying Transistor, Protective Diode, Optoisolator, Secondary Supply Voltage*, ICs which drive optoisolator.

   * It is not defective if the voltage is over 2V when the keying circuit is ON.

2. None of REMOTE, CW and FSK circuits works.

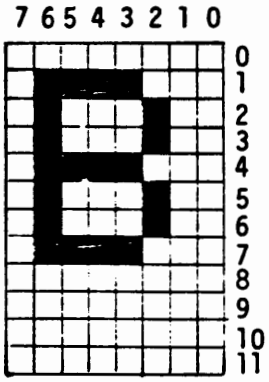
Check IC2 (7406), TR9 (2SC536) and check if the primary winding has disconnection or short circuits.

3. PTT circuit may be defective.

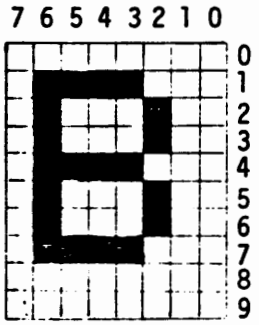
Check TR17 (2SC1384), D51 and IC16 (LS05).

13. VIDEO CIRCUIT

13.1 Character Font



Vertical Synchronizing Frequency: 50 Hz



Vertical Synchronizing Frequency: 60 Hz

Fig. 13-1

In case the vertical synchronizing frequency is 50 Hz, a character font occupies a 5 x 7 dot element in the 8 x 12 dot character matrix box. In case of 60 Hz, a character font occupies a 5 x 7 dot element in the 8 x 10 dot character matrix box.

13.2 Screen Format

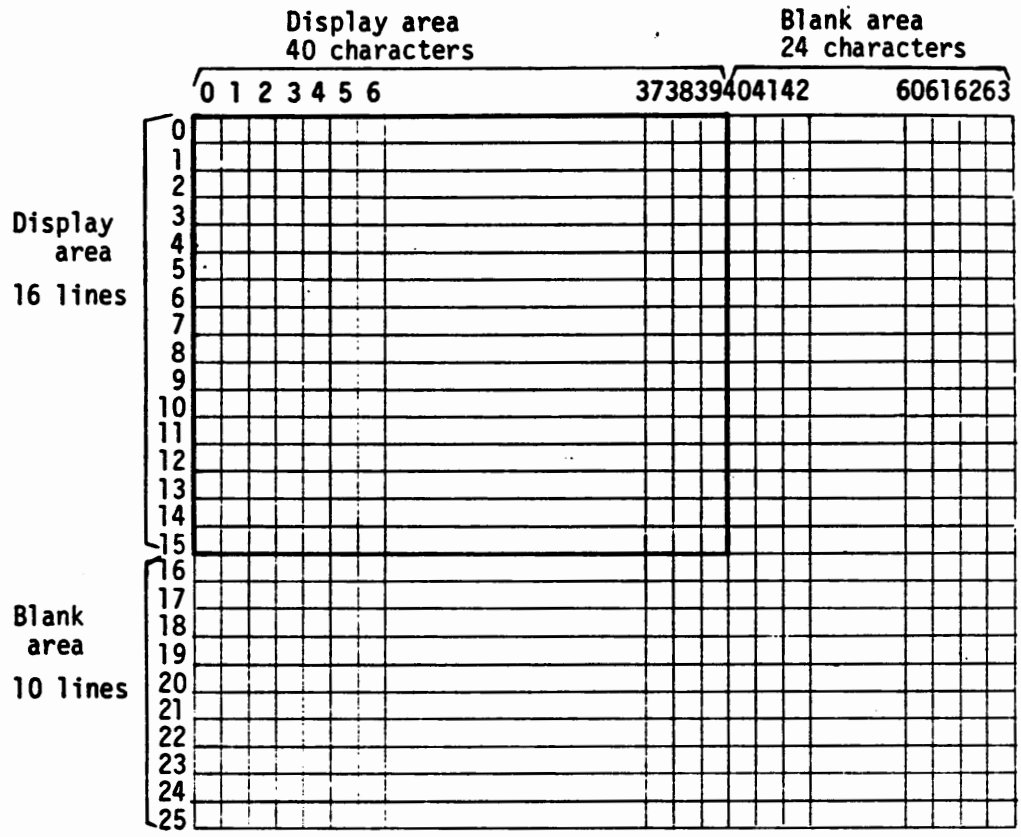
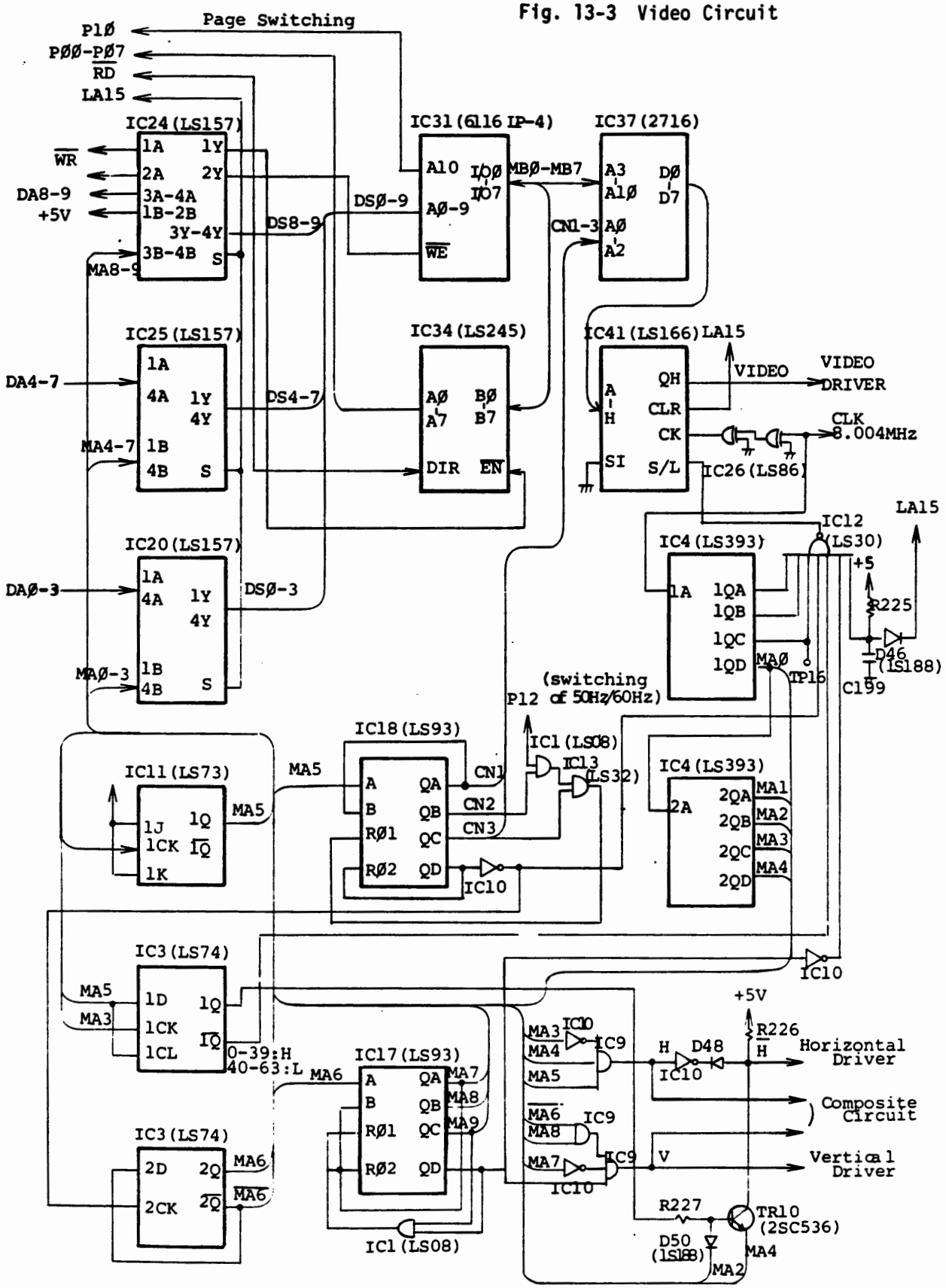


Fig. 13-2 Screen

A page of the screen consists of 40 characters x 16 lines.
The Theta-5000E provides 2 pages.

13-3 Video Signal Generating Circuit

Fig. 13-3 Video Circuit



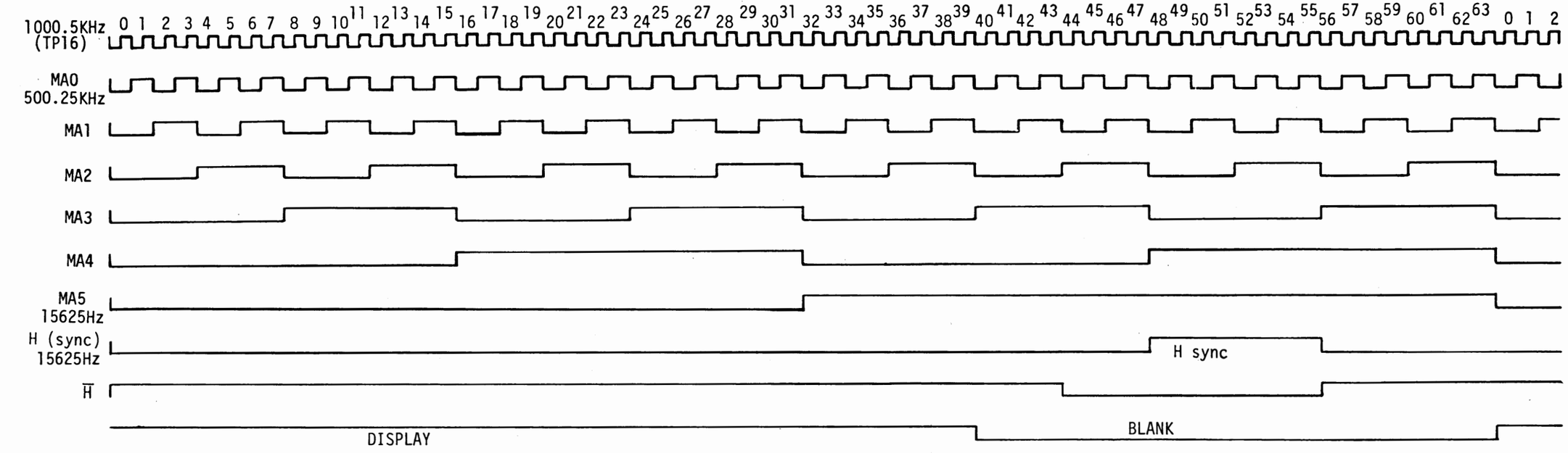


Fig. 13-4 Synchronizing Signal Timing Chart

(INTENTIONALLY LEFT BLANK)

The address signals DSØ-DS9 are provided to the address lines of IC31 (6116 LP-4). When IC31 is not accessed by CPU, DSØ-DS9 are connected to the address lines MAØ-MA9 which are produced in the video timing generation circuit through the multiplexer IC's 20, 24, 25.
The I/O terminal of IC31 (6116LP-4) outputs ASCII, JIS or graphic pattern code which is in the memory for the address specified by DSØ-DS9 connected to the address lines A3-A10 of IC37 (2716). The address lines AØ-A2 of IC37 are connected to the output CN1-CN3 of the row scan counter IC18 (LS93). The output port DØ-D7 of IC37 are connected to the shift resistor for the video signal generation and made parallel/series conversion.
To IC12 (LS03), the octal data of IC4 (LS393) and the display duration signal are provided, and the load signal is sent to the shift resistor IC41 (LS166) every eight clock in the display duration.
A divide-by-64 counter is contructed by 1QD (MAØ) - 2QD (MA4) of IC4 (LS393) and 1Q (MA5) of IC11 (LS73), whose output is synthesized at IC9 (LS11) and IC10 (LS04) to produce the horizontal synchronous signal $\overline{H}$ for the composite signal. IC3 (LS74) is a flip flop for generating the horizontal display duration signal and the display is activated between the counter value 0-39 of the divide-by-64 counter, and between 40-63 is left blank.
The horizontal synchronous signal $\overline{H}$ for the built-in monitor is synthesized by R226, R227, D48, D50, TR10 and IC10 (LS04). IC18 (LS93) is a counter for the row scan which becomes a decade counter by IC1 and IC13 when P12 of CPU is High level, in which case the number of vertical elements for one character will be 10 and the vertical synchronous signal will be 60Hz. In case P12 of CPU is Low level, it becomes a divide-by-12 counter in which case the number of vertical elements for one character will be 12 and the vertical synchronous signal will be 50Hz.
A divide-by-26 counter is consist of 2Q (MA6) of IC3 (LS74), IC17 (LS93) and IC1 (LS08), whose output is synthesized at IC9 (LS11) and IC10 (LS04) to obtain the vertical synchronous signal V. The vertical display duration signal is obtained from QD of IC17 (LS93). The display is activated between the counter value Ø-15 of the divide-by-26 counter and 16-25 is left blank.

13.4 Video Driver Circuit · Composite Video Circuit

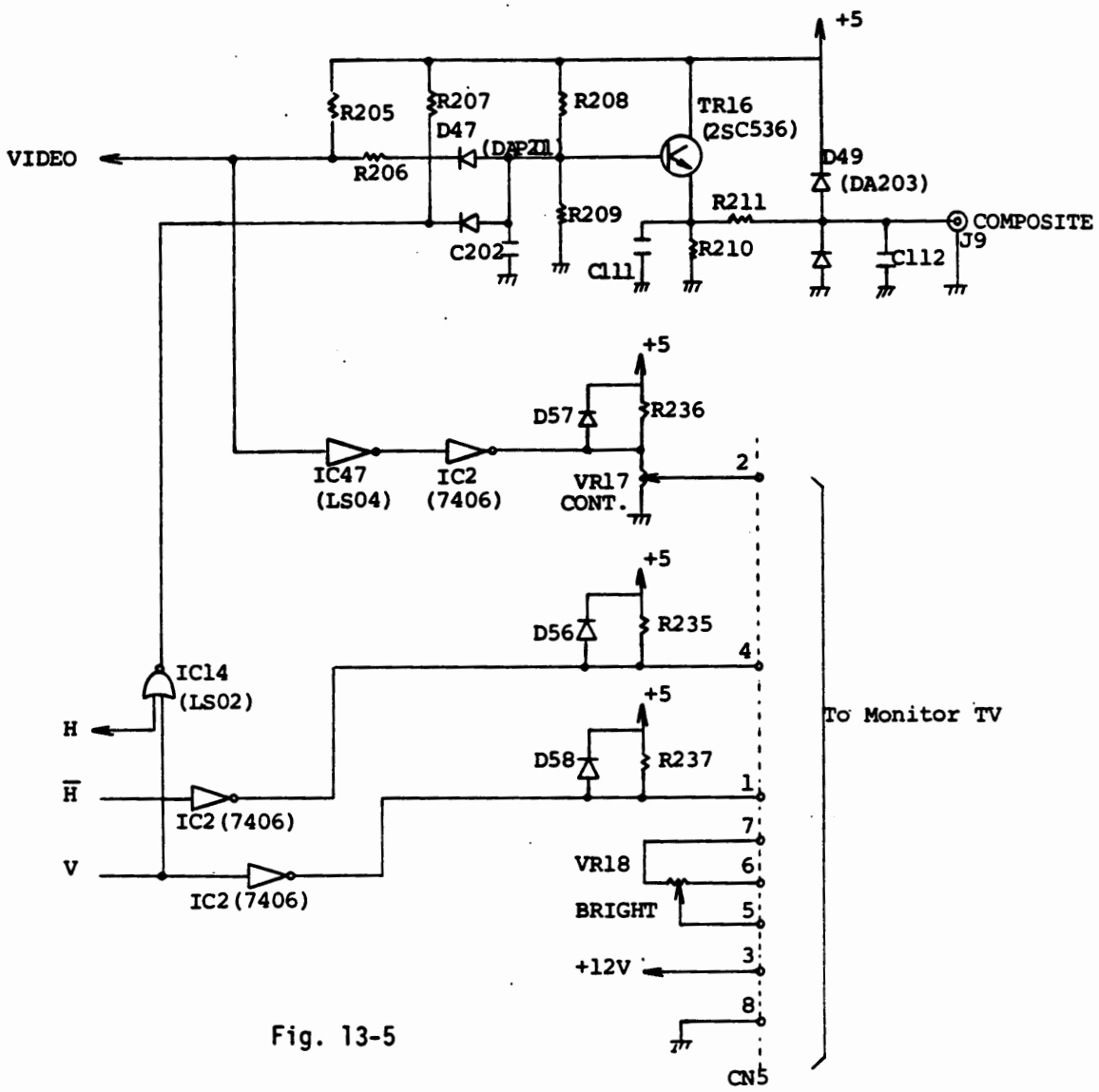


Fig. 13-5

Each of the VIDEO, $\overline{H}$ and V signals obtained from the video signal generating circuit is sent to the built-in monitor TV through the driver IC2 (7406). VR17 is a variable resistor for contrast adjustment, VR18 is a variable resistor for brightness adjustment. An +12VDC power is supplied from CN5 to drive the built-in monitor.
H and V signals are synthesized at IC14 (LS02) and are sent together with the VIDEO signal to the composite signal synthesizing circuit which consists of D47 (DAP201) and TR16 (2SC536).

[PROBLEMS]

1. Proper display on the built-in monitor screen but no COMPOSITE signal output.
   Check IC14 (LS02), D47 (DAP201), TR16 (2SC536) and the arounds.

2. No display on the built-in monitor screen but proper COMPOSITE signal output.

   1) Check IC2 (7406), VR17 and VR18. Check if CN5 is defective of contact or down.

   2) Check the built-in monitor.

3. No display on the built-in monitor screen, nor the COMPOSITE signal output.

   Check if the horizontal and vertical synchronizing signal are sent properly.

↓OK	↓NO
Check the VIDEO signal circuit - IC20 (LS157), IC24 (LS157), IC25 (LS157), IC31 (6116LP-4), IC32 (2716) and IC41 (LS166).	Check the synchronizing signal generating circuit.

4. Two data or more are displayed horizontally when one data is to be displayed on the screen.

   Check IC4 (LS393), IC11 (LS73), IC9 (LS11) and IC10 (LS04).

5. Two data or more are displayed vertically when one data is to be displayed on the screen.

   Check IC18 (LS93), IC3 (LS74), IC17 (LS93), IC9 (LS11) and IC10 (LS04).

6. Horizontal synchronization or vertical synchronization can not be obtained.

   Check the circuit for synthesizing the synchronizing signal which consists of IC9 (LS11) and IC10 (LS04), and the arounds.

SPARE PARTS LIST

I C

CODE NO.	NAME	DESCRIPTION
IC 1	8031	CPU
IC 2, 12	LS373	TTL
IC 3	LS245	"
IC 4	27128	EPROM (PROGRAM MEMORY)
IC 5	LS145	TTL
IC 6, 7, 8	LS157	"
IC 9	LS73	"
IC 10	LS74	"
IC 11	8255	PPI
IC 13	6116LP-4	CMOS RAM
IC 14, 15	LS93	TTL
IC 16	5832	REAL TIME CLOCK
IC 17	14569	CMOS LOGIC
IC 18	LS166	TTL
IC 19	2716	EPROM (CHARACTER GENERATOR)
IC 20	LS393	TTL
IC 21, 22	LS03	"
IC 23, 33, 35	LS04	"
IC 24	LS11	"
IC 25	LS30	"
IC 26	LS00	"
IC 27	LS08	"
IC 28	LS02	"
IC 29	LS32	"
IC 30	LS51	"
IC 31	LS86	"

CODE NO.	NAME	DESCRIPTION
IC 36	LS05	TTL
IC 37	7406	"
IC 38, 50	14051	CMOS LOGIC
IC 39, 40, 41	14066	"
IC 42, 43	3900	OP. AMP.
IC 44, 45, 46	324	"
IC 47	339	COMPARATOR
IC 48, 49	LB1405	LEVEL METER
IC 51, 52	14052	CMOS LOGIC
IC 53	7805	5V VOLTAGE REGULATOR
IC 54	7812	12V VOLTAGE REGULATOR
IC 55	14021	CMOS LOGIC
IC 56	14094	"
IC 57	14068	"
IC 58	14007	"
IC 59	PC837	OPTOISOLATOR
IC 60	BA546	AUDIO AMP.

D I O D E

CODE NO.	NAME	DESCRIPTION
D 1, 13-16, 28, 43 45, 49	DA203	DIODE ALLEY
D 2-4, 23, 26-29 33-39, 56-58	1S1588, DS448	"
D 5, 12	RD3.3EB	ZENOR DIODE
D 6, 7	SLP-169B	LIGHT EMISSION DIODE
D 8, 9	SLP-139B	"
D 10, 11	SLR-34UR	"

CODE NO.	NAME	DESCRIPTION
D 17-22, 24, 25	1S188FM	DIODE
46, 48, 50		
D 30	DBA30	BRIDGE
D 32	RD30EC	ZENOR DIODE
D 40-42, 51	1SR35-200VL	DIODE
D 47	DAP201	DIODE ALLEY
D 52-55	DAP601	"

TRANSISTOR

CODE NO.	NAME	DESCRIPTION
TR 1-3, 5, 9, 10, 16	2SC536F	TRANSISTOR
TR 4	2SA1015Y	"
TR 7	DTA114	"
TR 13, 17	2SC1384	"
TR 14, 15	2SC2271E	"

COIL

CODE NO.	NAME	DESCRIPTION
L 1, 6, 7, 12, 13, 19	C4433	INDUCTOR
L 8, 9, 10	C4519	TROIDAL COIL
L 11, 14, 15	42724 P821K	FIXED INDUCTOR 820 μH
L 16, 17	C3637A	TROIDAL COIL
L 18	C4447	CHOKING COIL

VARIABLE RESISTOR

CODE NO.	NAME	DESCRIPTION
VR 1, 4	1021A 22K	TRIMMER POTENTIOMETER 22K
VR 2	" 10K	" 10K
VR 3, 5-7	" 4.7K	" 4.7K
VR 8	179-5KB	VARIABLE RESISTOR 5KB
VR 9, 13, 14	1021A 47K	HALF-FIXED VR 47K
VR 10	" 22K	" 22K
VR 11	" 10K	" 10K
VR 12	" 4.7K	" 4.7K
VR 15	123P-N-10KB	VARIABLE RESISTOR 10KB
VR 16	179N-10KA	" 10KA
VR 17	123P-N-500B	" 500 B
VR 18	123P-N-100KB	" 100KB

CONNECTOR

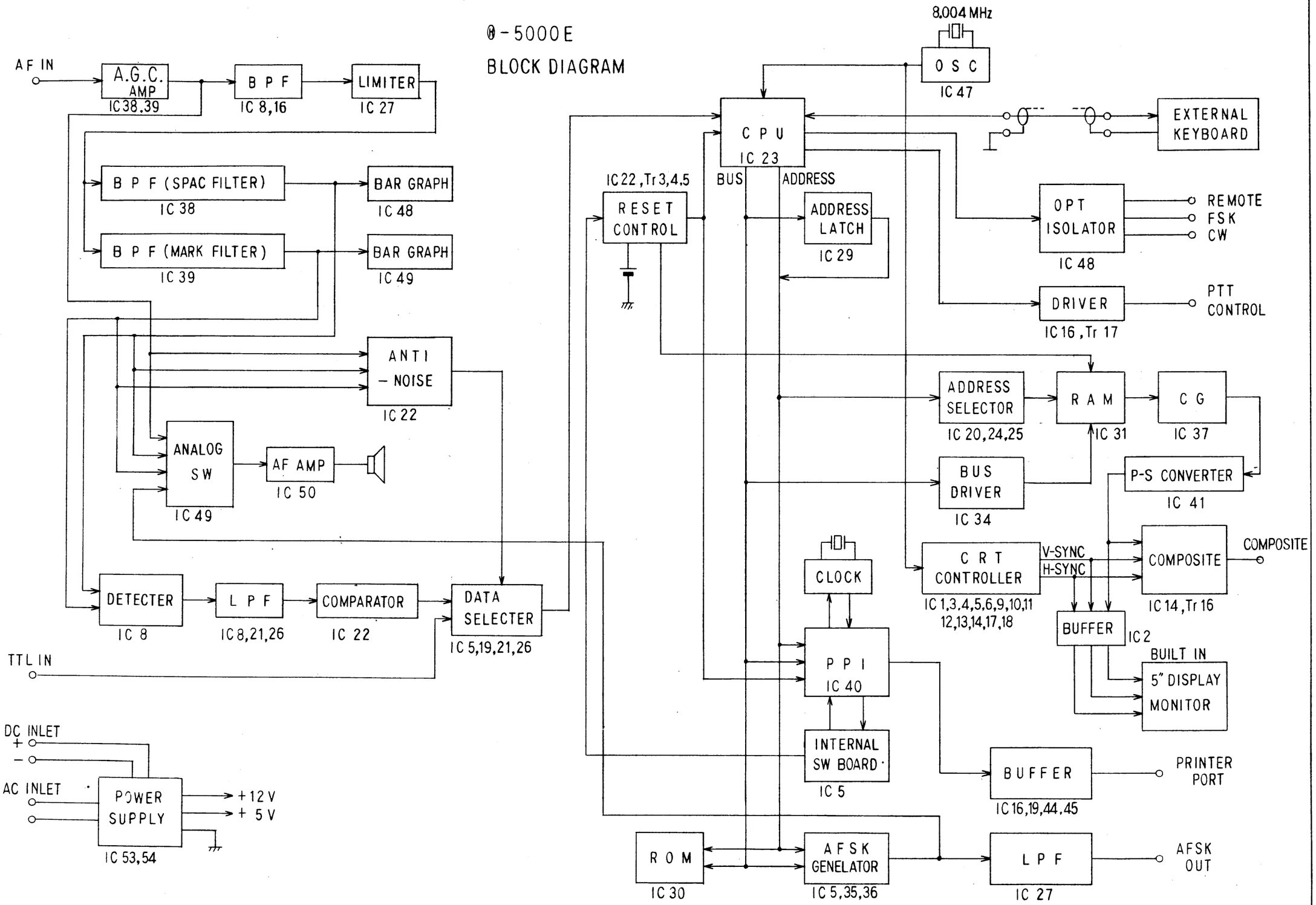
CODE NO.	NAME	DESCRIPTION
CN 1	5281-4A	WAFER 4P
CN 2	1LG-10P	HEADER 10P
CN 3	1LG-2G	" 2P
CN 4	JAE-34PE-D4T1-LT	BLOCK HEADER
CN 5	5281-8A	WAFER 8P
CN 6	D6-729A-200	DIN CONNECTOR
CN 7	5281-2A	WAFER 2P
CN 8	5281-3A	WAFER 3P
CN 9	1LG-3P	HEADER 3P

OTHER PARTS

CODE NO.	NAME	DESCRIPTION
T 2	C-4432	OSCILLATION TRANSFORMER
T 3	T40VA	POWER SOURCE TRANSFORMER
X 1	8MHZ	CRYSTAL
X 2	32.768KHZ	"
J 1-9	SQ-3099	PIN JACK
J 10, 11	SQ-3063	"
S 1	SDU	POWER SWITCH
S 3	JS5040	VOLTAGE SWITCH
S 4	SUZA1-U	10-GEAR PUSH SWITCH
S 5	SUZA1-L	"
S 6-9	SPQ051D	5-GEAR PUSH SWITCH

NOTE: THE EQUIVALENT MAY BE MOUNTED IN THE UNIT IN PLACE OF ABOVE-MENTIONED PARTS.

ⓐ-5000E
BLOCK DIAGRAM



DDC5NDG

DATA DISPLAY MONITOR CHASSIS

TECHNICAL MANUAL

DO NOT SCALE THIS DRAWING

	SCALE	TITLE TECHNICAL MANUAL	SIZE
	DRAWN	MODEL DDC5NDG	PAGE OF PAGES
REVISION	CHECKED		

CONTENTS

DO NOT SCALE THIS DRAWING

	SCALE	TITLE CONTENTS	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE OF PAGES 1/32
REVISION	CHECKED		

SAFETY PRECAUTION

WARNING : Service should not be attempted by anyone unfamiliar with the necessary precautions on this unit.
The following precautions are necessary during servicing.

1. Some parts such as a picture tube in this monitor have special safety-related characteristics for X-RAY RADIATION protection. For continued safety, the parts replacement should be undertaken referring to item 2 below.

2. Many electrical and mechanical parts in this unit have special safety-related characteristics for protection against shock hazard, fire hazard and others. These characteristics are often passed unnoticed by a visual inspection and the protection afforded by them cannot necessarily be obtained by using replacement components rated for higher voltage wattage, etc. Replacement parts which have these special safety characteristics are identified in this manual and its supplements marked with a ⚠ on the schematic diagram and the parts list. Before replacing any of these components, read the parts list in this manual carefully.

3. When replacing a chassis in the cabinet, always be certain that all the protective devices are installed properly, such as; insulating cover, barries, strain relief, etc.

GENERAL DESCRIPTION

Model DDC5NDG is a 5.5-inch raster scan display monitor designed specifically for data terminals. This model designed for high quality display of the alphanumeric dot characters.
DDC5NDG accepts video, horizontal drive and vertical drive as separate TTL level signals.
The 100% solid state sillicon circuitry provides cool operation and high reliability.

Features

- 5.5 inch CRT
- Direct etched non glare faceplate (option)
- 650 lines horizontal resolution
- Horizontal Video Center Control
- Compact chassis type for easy mounting

DO NOT SCALE THIS DRAWING.

		GENERAL DESCRIPTION	
		DDC5NDG	3/32

SPECIFICATIONS

Mechanical (approx.)

Chassis Dimension	130 mm (W) x 113 mm (H) x 219 mm (D)
Weight	
Net Weight	1.2 Kg.

Picture tube

Size & deflection	5.5 inch, 20.0 mm dia. neck, 70° deflection.
Faceplate	360 mm radius, direct etched non-glare faceplate.
Phosphor	P39 (GREEN)
Type	C5M113P39

Controls

Width	Coiled type mounted on PCB
Horiz. Video-center	Rotary VR type mounted on PCB
Height	Rotary VR type mounted on PCB
Vert. Linearity	Rotary VR type mounted on PCB
Vert. Hold	Rotary VR type mounted on PCB
Horiz. Linearity	Coiled type mounted on PCB
Focus	Rotary VR type mounted on PCB
Sub-Brightness	Rotary VR type mounted on PCB
Contrast	Rotary VR type mounted on Main PCB (Optional)
Brightness	External, user supply
Raster centering	Raster centering rings (magnet type) mounted on Deflection Yoke

Input Connector . . . . . 10 pin cardedge board connector. (refer to attached Input Signal Interface)

Performance

Horiz. Resolution	
Center	650 lines, nominal.
Corner	500 lines, nominal.
Video Bandwidth	12 MHz, nominal. (−3 dB)
Geometric Distortion	±2.5 %, nominal
	±3.0 %, maximum.
Non-Linearity	
Vertical	7 %, nominal.
	10 %, maximum.
Horizontal	10 %, nominal
	13 %, maximum

Display Area (Picture centering and tilt specified in Fig. 1 & 2 are Sanyo's timing.)

*Horizontal	92±5 mm
*Vertical	70±5 mm

DO NOT SCALE THIS DRAWING

	SCALE	SPECIFICATIONS	
	DRAWN	DDC5NDG	PAGE 4/32
REVISION	CHECKED		

Electrical

Input Signal	
Video signal	4±1.5 Vpp thru 500 ohm contrast control VR, positive going white.
Horizontal drive	4±1.5 Vpp 5K ohms, positive going.
Vertical drive	4±1.5 Vpp 15K ohms, negative going.
**Horizontal rate	15.25 KHz min. – 16.6 KHz max.
**Vertical rate	49 to 61 Hz
Retrace time (nominal)	
Horizontal	7.0 uS
Vertical	850 uS
Power Requirement	DC 12V ±0.1V, regulated, 0.8A nominal 1.0A maximum Ripple 10 mVpp maximum

Environmental

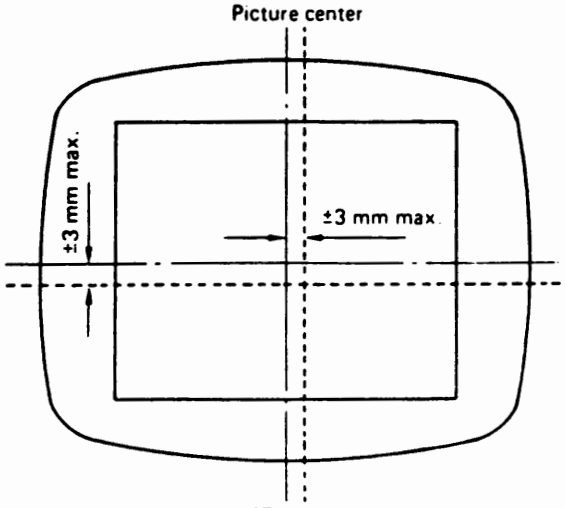
Temperature	
Operation	0°C to 55°C
Storage	–20°C to 70°C
Humidity	
Operation	10 % to 80 %, non-condensing
Storage	10 % to 80 %, non-condensing
Altitude	Up to 10,000 ft (3,050 m)
X-ray radiation	Less than 0.5 mR/H
MTBF	30,000 hours, without CRT

Factory adjusted rate

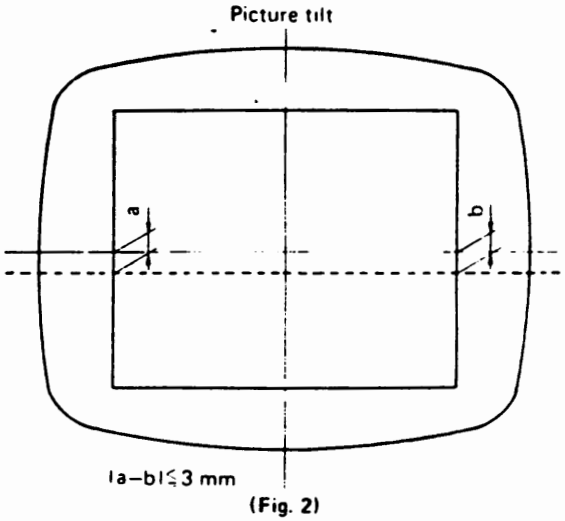
Power Source	DC 12±0.1 V, regulated
Scanning Frequency (depend on timing chart)	
Vertical	60 Hz
Horizontal	16.6 KHz
Brightness	Raster cutoff

NOTE: Items with "*" marks in this specifications indicate the Factory Adjusted Rates.
Items with "**" marks indicate Factory Timing. (Refer to Page 7)
Input Signal Format is specified on Page 8.

Picture centering & tilt



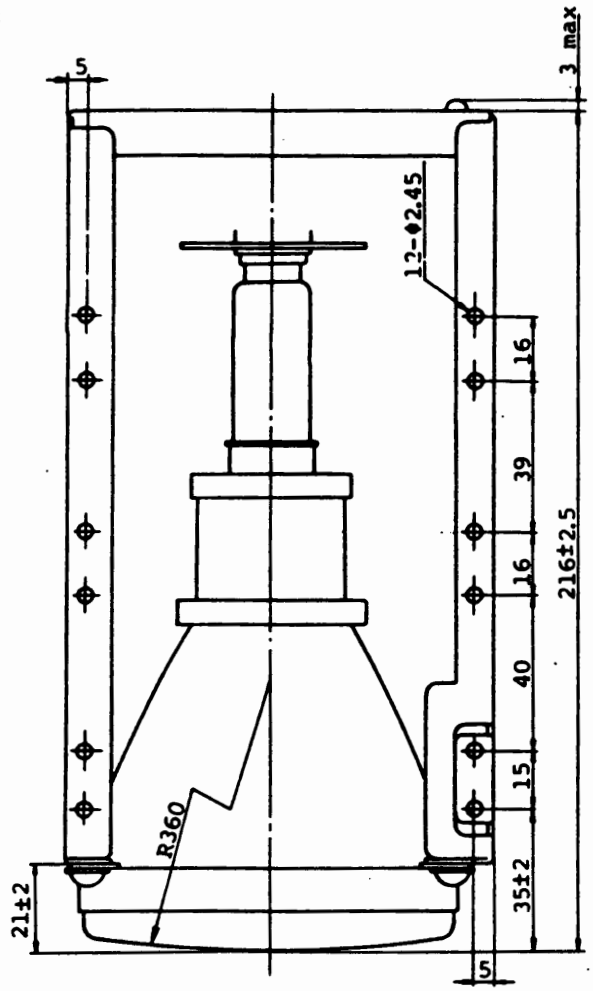
(Fig. 1)

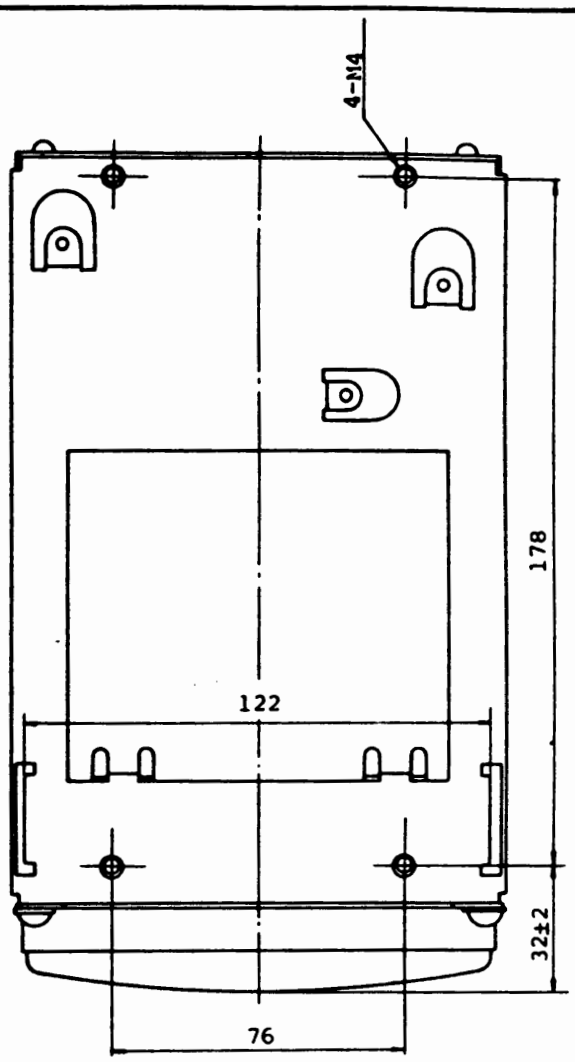


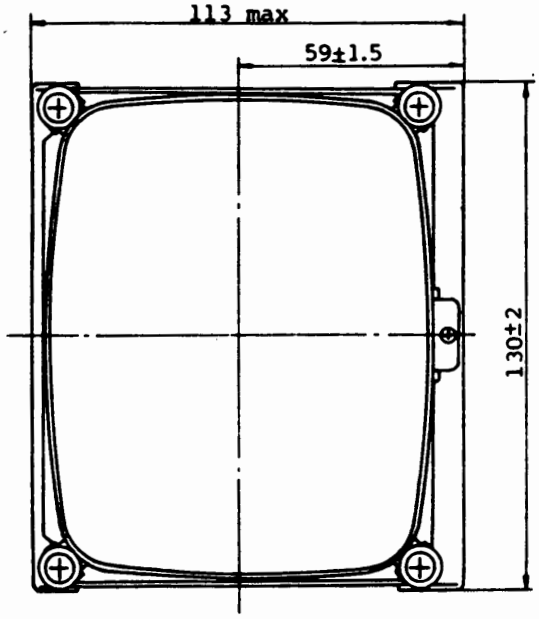
(Fig. 2)

DO NOT SCALE THIS DRAWING.

REVISION		SPECIFICATIONS	
		DDC5NDG	5/32





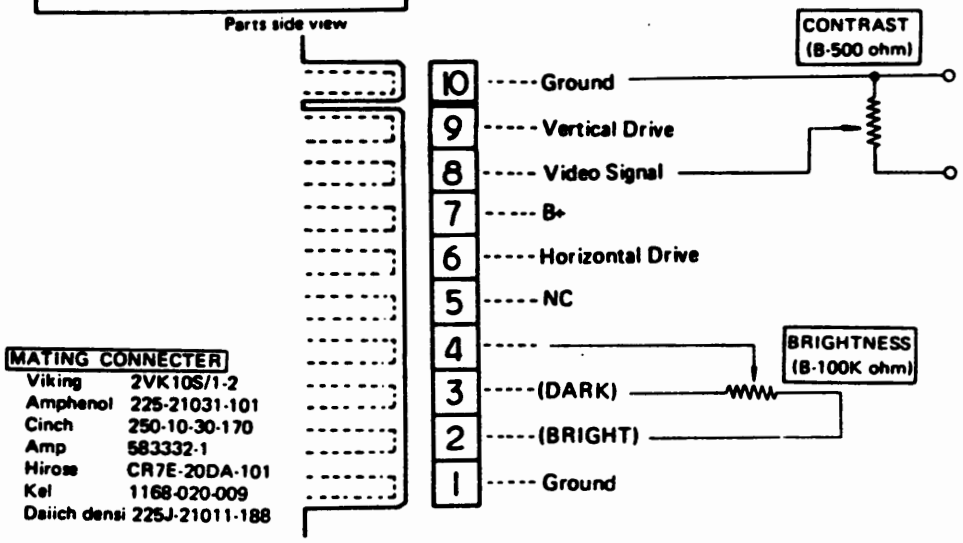


Unit: mm
DO NOT SCALE THIS DRAWING.

05MDK

	SCALE	TITLE CHASSIS DIMENSIONS	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE of PAGES 6/32
REVISION	CHECKED		

PIN CONNECTION



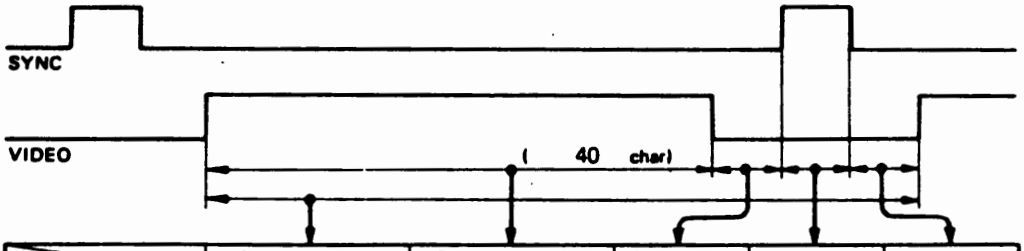
MATING CONNECTER

Viking	2VK10S/1-2
Amphenol	225-21031-101
Cinch	250-10-30-170
Amp	583332-1
Hirose	CR7E-20DA-101
Kel	1168-020-009
Daiich densi	225J-21011-188

CHARACTER INFORMATION

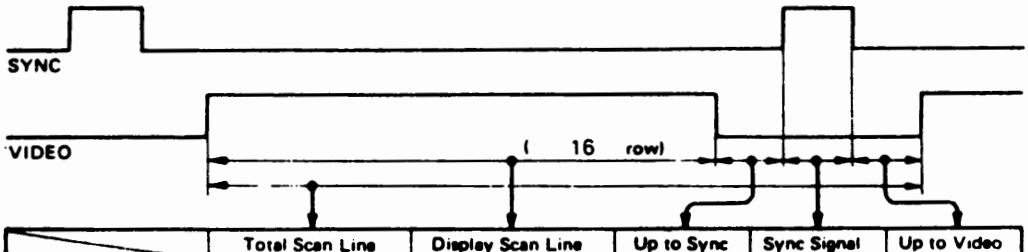
CHARACTER	5 x 7 dots	DOT CLOCK	8 MHz
CHARACTER BLOCK	50Hz : 8 × 12 60Hz : 8 × 10 dots	CHARACTER CLOCK	1 MHz

HORIZONTAL TIMING



	Total Character	Display Character	Front Porch	Sync Signal	Back Porch
Horizontal Rate	64 Char	40 Char	8 Char	8 Char	8 Char
15.625 kHz	64 uS	40 uS	8 uS	8 uS	8 uS

VERTICAL TIMING

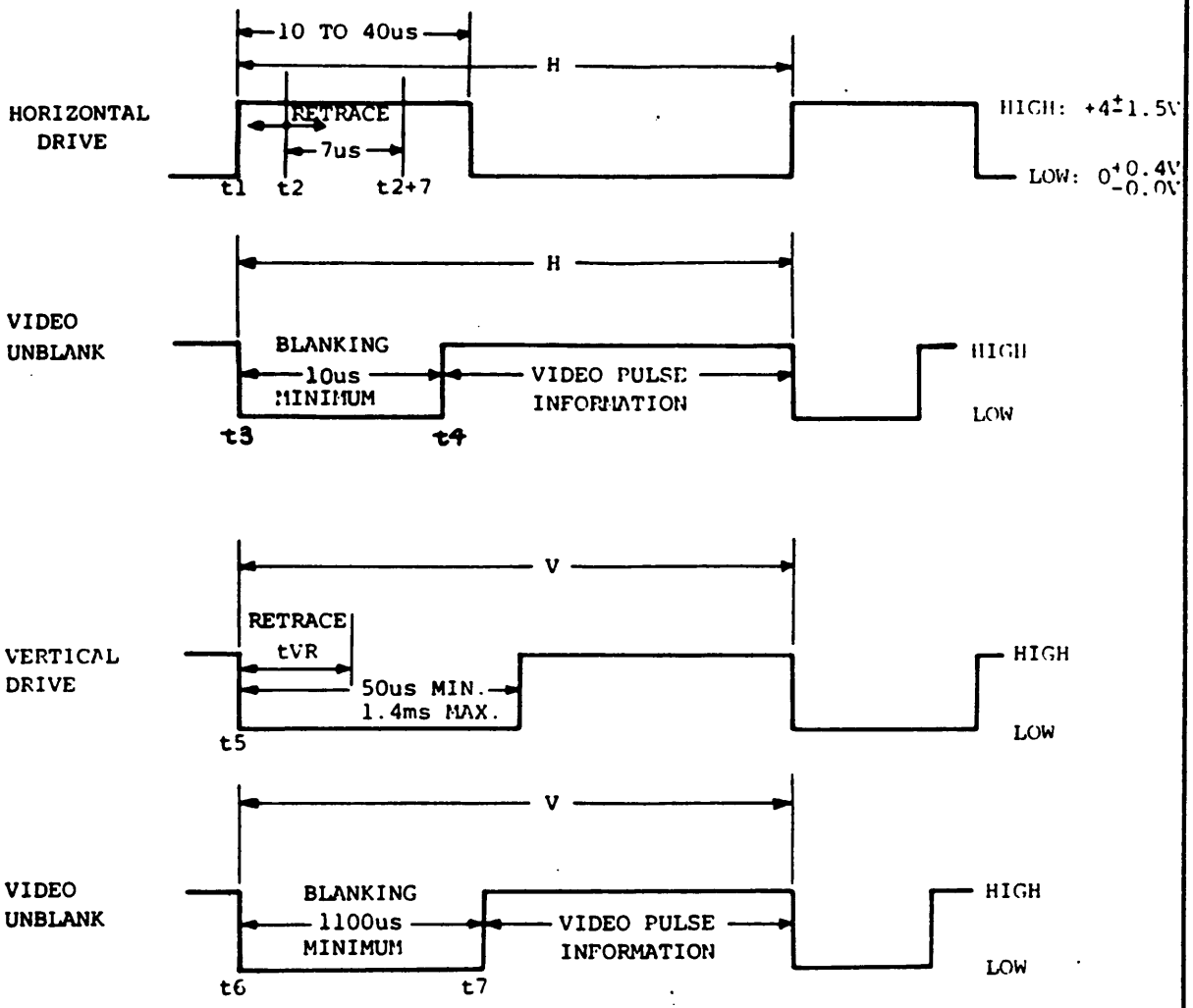


	Total Scan Line	Display Scan Line	Up to Sync	Sync Signal	Up to Video
Vertical Rate	312 (260) Line	192 (160) Line	48(40)Line	12(10) Line	60(50) Line
50 (60) Hz	20 (16.6) mS	12.3 (10.2) mS	3.07(2.56)mS	3.07(2.56)mS	3.84(3.20)mS

Card No.-15

DO NOT SCALE THIS DRAWING.

	SCALE	TITLE INPUT SIGNAL INTERFACE	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE of PAGES 7/32
REVISION	CHECKED		



NOTES: 1. HORIZONTAL RETRACE IS INITIATED AT t2 (1.5 TO 6.5μs AFTER t1, DEPENDING ON SETTING OF VR601)
2. H=PERIOD OF ONE LINE: 65.57μs MIN. TO 60.24μs MAX.
3. VERTICAL RETRACE IS INITIATED AT t5 WITHOUT DELAY.
4. V=PERIOD OF ONE FIELD: 16.4ms MIN. TO 20.4ms MAX.

TABLE 1 t3 VS t1 TIMING FOR CENTERED HORIZONTAL VIDEO AS FUNCTION OF H. BLANKING WIDTH

HORIZONTAL VIDEO BLANKING	
WIDTH t4 - t3	LEAD / LAG t1 - t3
10	5.0 TO 0μs
12	4.0 TO 1.0μs
14	3.0 TO 2.0μs
16	2.0 TO 3.0μs
18	1.0 TO 4.0μs
20	0 TO 5.0μs

TABLE 2 t6 VS t5 TIMING FOR CENTERED VERTICAL VIDEO AS FUNCTION OF V. BLANKING WIDTH

VERTICAL VIDEO BLANKING	
WIDTH t7 - t6	LEAD / LAG t5 - t6
1100	125μs
1150	150μs
1250	200μs
1450	300μs
1650	400μs

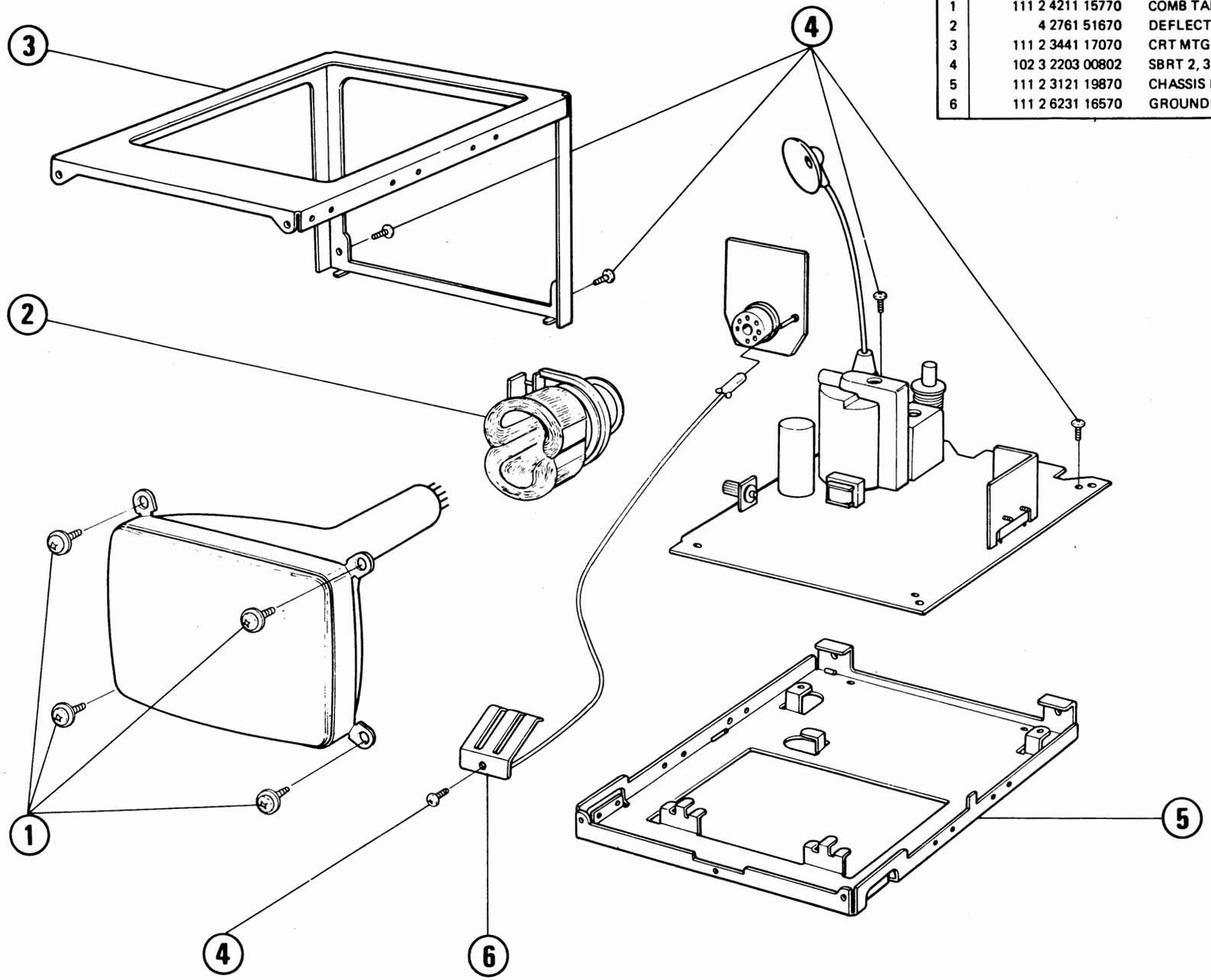
VERTICAL RETRACE TIME tVR=850us

DO NOT SCALE THIS DRAWING

	SCALE	TITLE INPUT SIGNAL FORMAT	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE of PAGES 8/32
REVISION	CHECKED		

EXPLODED VIEW

NO.	PART CODE	DESCRIPTIONS	QTY
1	111 2 4211 15770	COMB TAP SCREW-MBW	1
2	4 2761 51670	DEFLECTION YOKE	1
3	111 2 3441 17070	CRT MTG BRKT-MDK	1
4	102 3 2203 00802	SBRT 2, 3.0x8 Z1	5
5	111 2 3121 19870	CHASSIS FRAME-MDK	1
6	111 2 6231 16570	GROUNDING TIP-MDK	1



DO NOT SCALE THIS DRAWING.

REVISION		SCALE	TITLE EXPLODED VIEW	FILE CODE
		DRAWN	MODEL DDC5NDG	PAGE of PAGES 9/32
		CHECKED		

CONTROLS on PCB

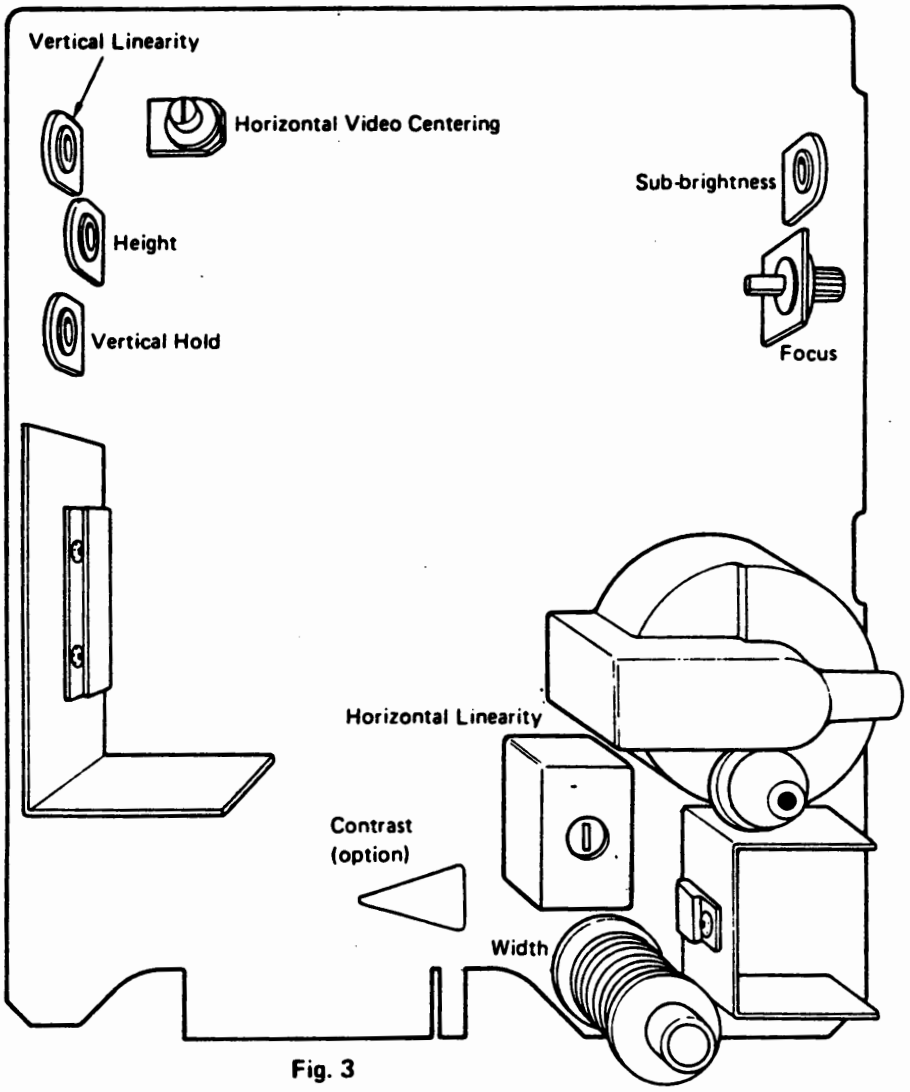


Fig. 3

DO NOT SCALE THIS DRAWING

REVISION	DRAWN	INSTRACTIONS	
		DDC5NDG	10/32

INSTALLATION

3-1. Safety Warning

1) Extreme care should be taken in handling the cathode ray tube as rough handling may cause it to implode. Any undue external pressure on glass, especially on the thin neck portion, should be avoided.
2) In case of CRT replacement, be sure to use the tube of the samy type number as specified. The use of the cathode ray tube type other than the specified may cause possible increase of X-ray radiation.

3-2. Mounting

A. It is recommended that all the Disk Portion is covered by silicon steel. In addition, it is an effective method to isolate between the Disk Portion and the FBT of the CRT Display Monitor by silicon steel. Special care should be taken when the Disk Portion is located on the right side.

B. Any power transformer, power unit or switching regulator should be located well apart from CRT, Deflection Yoke, and the printed circuit board (especially the vertical and horizontal circuit) as the external flux field or noise may cause mal-effect on displayed picture stability.

3-3. Power Input

The DC input power is applied through Pin 7 (B+) and Pin 1 (Ground) of 10-pin cardedge board connector.

CAUTION: A. As the picture size varies according to the variation of the voltage (Reference voltage: 12 V DC), the variation of ±0.1 or less is desirable.

B. The use of power source with many ripples may cause mal-effect on displayed picture stablility. The ripple of 10 mVpp or less is desirable.

3-4. Data Signal Input

Apply data signal to each pin of 10-pin cardedge board connector. (Refer to Input Signal Interface.)

CAUTION: If the amplitude of the video signal is 2.0 Vpp (nominal) or more, use the contrast control (B-500 ohm VR) for gain adjustment. Otherwise, the displayed picture will be out of focus because the video amplifier is saturated.

Some models are equipped with the contrast control on the p.c.b. Call the dealer for the details.

3-5. Controls

1) The following controls are factory adjusted for the optimum, and user's readjustments are not required.

Controls	PCB Marking	Location
Focus	FOCUS	VR652
Width		L602
Vertical Linearity	V-LIN	VR503
Horizontal Linearity		L601
Height	V-HEIGHT	VR502
Centering		DY

2) Under listed controls may be readjusted if necessary, though standard adjustments have been made on all controls in factory.

Controls	PCB Marking	Location
Contrast	CONT	VR201 If equipped with.
Brightness	SUB-BRIGHT	VR651
Horizontal video center	VIDEO CENTER	VR601
Vertical hold	V-HOLD	VR501

Note: 1. All controls are located on main PCB.
2. SUB BRIGHT can be used as main brightness control if no connection is made to external brightness control.

3) External Brightness and Contrast Control Connection
If necessary, an external brightness control (B-100K OHM) and external contrast control (B-500 OHM) can be used under the following method with 10 pin cardedge board connector. -
Refer to INPUT SIGNAL INTERFACE.

Note: If the contrast control is used, check the items below.
1. Contrast control is not equipped with the unit, use EXTERNAL CONTRAST CONTROL as the Input Signal Interface.
2. Contrast control is equipped with the main PCB (VR201).
   1) Remove the VR 201 from main PCB.
   2) Remove Signal Cable (coaxial cable) from Point-SI11 on main PCB.
   3) Then connect Signal Cable (coaxial cable) to Point-SI1 (Slider of control VR) of main PCB
   4) Use EXTERNAL CONTRAST CONTROL as the Input Signal Interface

OPERATION

4. Operation

4-1. Apply power and signals (Video, Vert-drive and Horiz-drive) as specified, and check the display synchronization.

4-2. Brightness Adjustment
Set external brightness (if connected) and contrast control (equipped with the unit or external) to its maximum, and adjust sub-brightness control for visual cutoff raster.

4-3. Contrast Adjustment
With brightness, set to visual raster cutoff, adjust the contrast control at the point where defocusing disappers when the control is turned down from its maximum.

Note:
Refer to ADJUSTMENT on page 14.

CAUTION FOR SERVICING

5. Caution

Before remove CRT, discharge the HIGH VOLTAGE throughly with the following procedures step 1 to 5 (Refer to Fig. 4)

WARNING: Great care must be taken because the High Voltage will be charged for approximately 30 hours or more after power is turned off. Dischage the High Voltage before assembling each of the units or servicing.

Procedures

Step 1. Remove the CRT Socket P.C.Board from CRT.
Step 2. Remove CRT Grounding Wire from CRT Socket P.C.Board.
Step 3. Discharge the High Voltage which has been charged in CRT. (See Fig. 4)
Step 4. Remove Anode Cap.

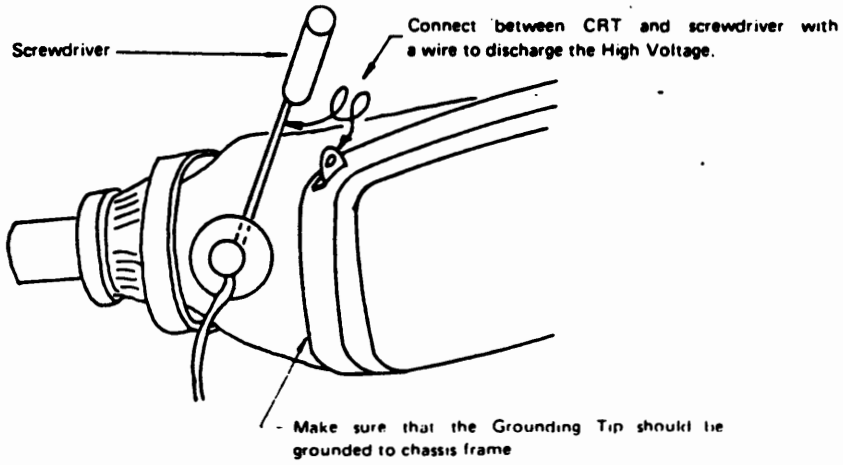


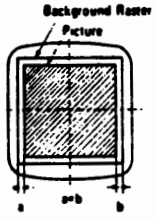
Fig. 4 Discharge of High Voltage

DO NOT SCALE THIS DRAWING.

		OPERATION CAUTION FOR SERVICING	
REVISION		DDC5NDG	13/32

ADJUSTMENT

1. **PREPARATION** Make sure preparatory adjustment is made before proceeding the adjustment procedure.
   - 1.1 **DC INPUT VOLTAGE** ..... Set specified DC input voltage. (12±0.1 V)
   - 1.2 **TEST SIGNAL** ..... Specified signal input voltage and timing. Character "H" should be displayed on the whole screen.
   - 1.3 **PICTURE SYNCHRONIZATION** ..... Synchronize the picture with V-Hold VR (VR501) for vertical.
2. **ADJUSTMENT PROCEDURE** (1. Refer to parts location diagram for points to be adjusted. 2. After servicing, make sure all the screws loosened for adjustment are re-tightened.)

	Item	Setting Value	Point to be Adjusted	Adjustment
2.1	Horizontal Video Centering		VIDEO CENTER (VR601)	(1) Set External Brightness or sub-bright VR (VR651) to where background raster slightly appears. (2) Adjust Horizontal Video Center (VR601) to where the displayed picture is center of the background raster in horizontal. (Leave even space at left and right between each side of the background.) (3) After Horizontal Video Center Adjustment, set Brightness (or Sub-brightness) to where the background raster disappears.
2.2	Horizontal Linearity		H. LIN Coil (L601)	Make width of character "H" at left, center and right even. Remarks: Horizontal width also change with this adjustment.
2.3	Horizontal Width	92±5 mm	WIDTH Coil (L602)	Obtain the specified value.
2.4	Vertical Sync		V-HOLD VR (VR501)	Center of hold range.
2.5	Vertical Linearity		V-LIN VR (VR503)	(1) Adjust Vertical Height to obtain 2/3 to 3/4 of the specified value.
2.6	Height	70±5 mm	HEIGHT VR (VR502)	(2) Adjust V-LIN to obtain equal height of character "H" at top and bottom. (3) Adjust HEIGHT VR to obtain specified value.
2.7	Contrast		CONTRAST VR (VR201)	Optimum point, but do not saturate character "H". (If equipped with.)
2.8	Brightness		SUB-BRIGHT VR (VR651)	(1) Set External Brightness VR (if equipped with) to maximum. (2) Set Sub-bright VR to where background raster disappears.
2.9	Focus		FOCUS VR (VR652)	Adjust Focus VR to obtain overall focus. Remarks; Make sure Brightness has been adjusted
2.10	Centering		CENTERING Magnets	(1) Place display area in the middle of the CRT. (Leave even space at top and bottom, left and right between each side and edge of the CRT.) (2) Correct picture slant with DY by loosing the screw securing the DY.

DO NOT SCALE THIS DRAWING.

FUNCTIONAL PRINCIPLE

6. Functional Principle

6-1. Video Amplifier

Video Amplifier consists of Q201, Q202, and its associated circuitry. A positive pulse is amplified and inverted by both transistors Q201 and Q202, and then injected to the cathode of CRT through R901. C201 compensates the high frequency of Video Amplifier, and VR651 controls the screen brightness of CRT. D654 and C653 are used as a spot killer when DC power source is cut off.

6-2. Vertical Circuit

The synchronous negative pulse inverted by Q501 through R501, C514 and R512 of differentiator circuit is injected to Pin 5 of IC501. The vertical free running frequency is determined by R504, R505, C503 and VR601. It is directly synchronized by the above pulse. As a result of the above opration, the rectangular pulse is generated at Pin 4 and is integrated to the sawtooth waveform by R506 and C505, and injected to Pin 7 through R607, VR502, and C504. Vertical linearity and height are respectively controlled by VR503 and VR502. The output at Pin 1 is loaded to L901 (Deflection Yoke) through C512. Q901 functions as ripple filter for the vertical circuit.

6-3. Horizontal Circuit

The base circuit of Q601 includes a clamp and a differentiator which makes Q601 output insensitive to drive pulse amplitude and width changes. The only requirement is that pulse amplitude be of 2.5 volts minimum and pulse width should be 10-40us. Q601 together with Q602 functions as a monostable multivibrator with Q603 being a slave that provides a positive feedback. Specifically, when Q601 is turned on by the drive pulse, it discharges C603 at a rate determined by the setting of VR601. When C603 is discharged to 2.75 volts, Q602 turns off. This change of state turns Q603 on and the base drive to Q602 from R606 is shunted thru Q603. Q602/Q603 remains in this state for nominally 25us until C603 recharges through A103 to 4 volts. At this time, Q602 is biased on again by the current through VR601. The multivibrator is now in a state that Q602 is on and Q601/Q603 is off. It will ramain in this state until the next drive pulse occurs or power is turned off. C603 is the only timing capacitor in the circuit and has two time constants associated with it. Primarily, the charge path between pin 1 and pin 3 of VR601 determines the on time of Q603 while the discharge path through the video centering control and Q601 determined the delay between application of the drive pulse and start of retrace (turn on of Q603).

6-4. High Level Stages

The output of Q603 is driven to the base of Q604 through T601. The horizontal output circuit consists of Q604, D604, L901, T602 and its associated circuitry. Q604 operates as a switch when affected by the driving pulse and supplies the sawtooth current to L901. D604 is a damper diode. C617, C605 and C606 are called resonance capacitors. The output pulse of T602 is rectified by D653, D652 and D651 for CRT G2, video amplifier, and brightness circuits respectively. L602 and L601 control the width and horizontal linearity.

7. TROUBLESHOOTING

- Plug in an edge input connector.
  - No Raster appears.
    - Line voltage drops. → Check B+ lines of the horizontal output.
    - Normal line voltage. → Check horizontal, CRT, and video circuits.
      - Only one horizontal raster line → Check for defects in Q701, vertical circuit, and deflection yoke for breaks or short in the wire.
      - Only one vertical raster line → Check for defects in horizontal output circuit and deflection yoke for breaks or short in the wire.
  - Raster appears.
    - Insufficient horizontal width → Check horizontal circuits.
    - Unusual vertical size → Readjust VR502 and VR503, or check Q701 and vertical circuit.
    - Dark screen → Readjust VR651 or check CRT's associated circuitry.
    - Vertical hold is not synchronized. → Check vertical circuit.
    - No picture → Check video circuit.
    - Picture appears.
      - Dot brightness is different horizontally and vertically. → Check video circuit.
      - Out of focus → Check CRT and VR652.
      - Picture appears intermittently. → Check for insufficient soldering in video and horizontal circuits.
      - Incorrect horizontal centering. → Readjust VR601.

8. HOW TO REPAIR

8-1. No Raster (1)

No Raster appears.

↓

Does the raster appear at maximum brightness ? ——YES——→ Readjust brightness.

↓ NO

Are there any troubles on B+ line and horizontal circuit ?

↓ NO

Is B+ applied to pin 7 of 10 pin-card connector ? ——NO——→ Check the card connector.

↓ YES

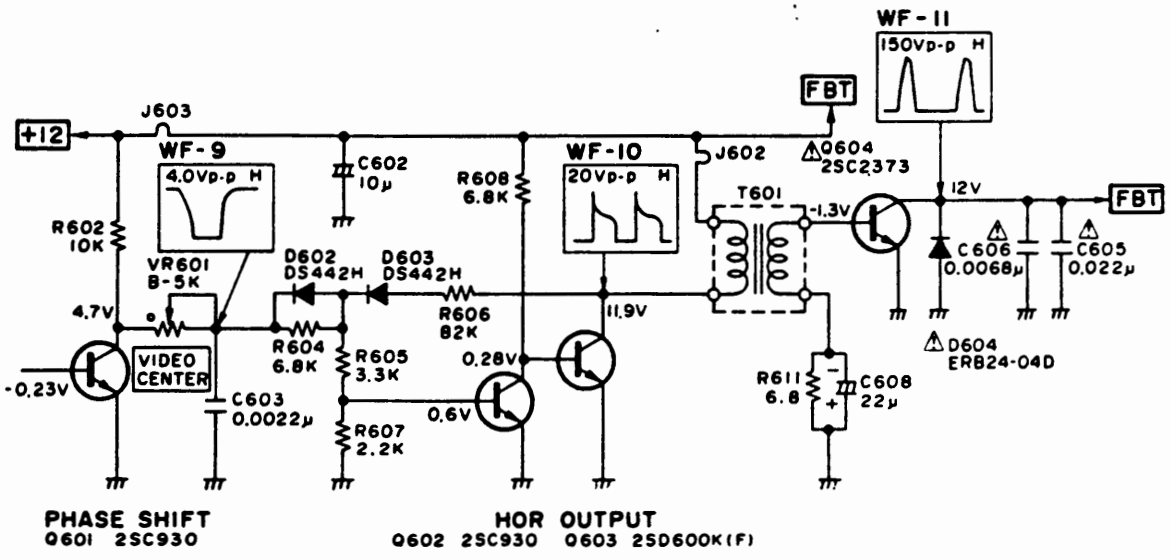
Is rectangular waveform applied to the collector of Q603 ? ——NO——→ Check horizontal phase shift circuit Q601. WF-9

↓ YES

Is power output of horizontal drive circuit applied to the Base of Q604 ? ——NO——→ Check horizontal drive circuit Q603. WF-10

↓ YES

Check horizontal output circuit Q604. WF-11



DO NOT SCALE THIS DRAWING

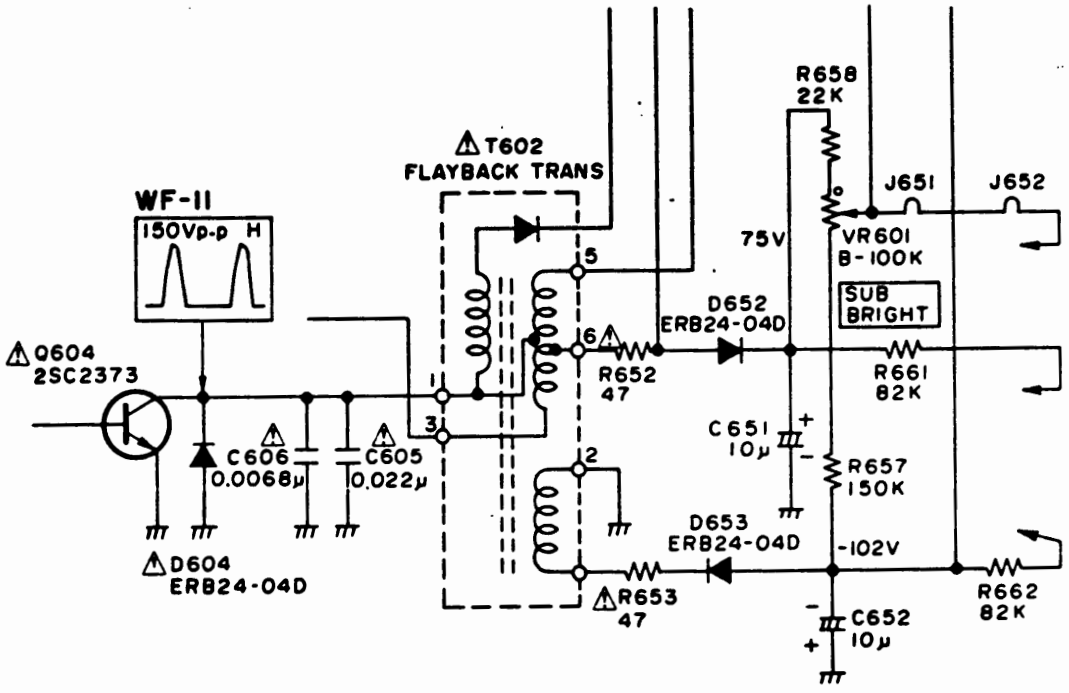
	SCALE	HOW TO REPAIR	
	DRAWN	DDC5NDG	17/32
REVISION	SHEET		

8-2. No Raster (2)

No Raster appears. (In the case of faulty high voltage and CRT circuits)

- Is high voltage applied to the anode of CRT ?
  - NO → Are pulses applied to the collector of horizontal output Q604 ? : WF-11
    - NO → Check horizontal output circuit.
    - YES → Check flyback transformer.
  - YES → Is normal heating voltage applied to CRT's Pin-3 and Pin-4 ?
    - NO → Check heating circuit.
    - YES → Is normal grid voltage (Eg2) applied to CRT's Pin-6 ?
      - NO → Check Eg2 circuit.
      - YES → Is normal cathode voltage applied to CRT's Pin-2 ?
        - NO → Check video circuit.
        - YES → Check CRT.

Note: Check high voltage by approaching the oscilloscope probe, or measure it with a high voltage meter, as high voltage is not able to be measured by a tester.



DO NOT SCALE THIS DRAWING.

REVISION	DRAWN / CHECKED	HOW TO REPAIR	
		DDC5NDG	PAGE 18/32

8-3. Only One Horizontal Raster Line

Only one horizontal raster line apprars.

↓

Troubles in vertical deflection circuit

↓

Is output voltage applied to DY's terminals (WD4) ? : WF-7

↓ NO

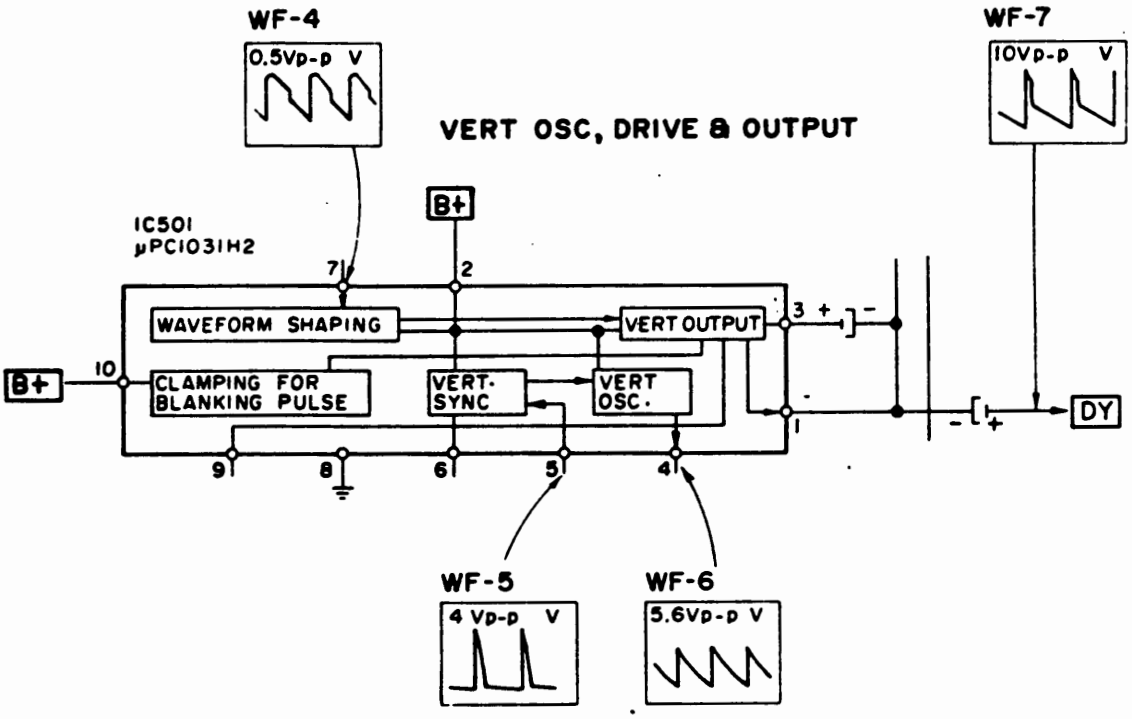
Is output applied to Pin-1 of IC ? ——— YES ——→ Check DY leads and defective connectors.

↓ NO

Is B+ applied to Pin-2 and Pin-10 of IC ? ——— NO ——→ Check B+ line.

↓ YES

Check IC and its associated circuits : WF-4,5 and 6



DO NOT SCALE THIS DRAWING.

	SCALE	TITLE: HOW TO REPAIR	FILE CODE
	DRAWN	ARCHIVE: DDC5NDG	PAGE 19/32
REVISION	CHECKED		

8-4. Vertical Synchronizing Trouble

Vertical hold is not synchronized.

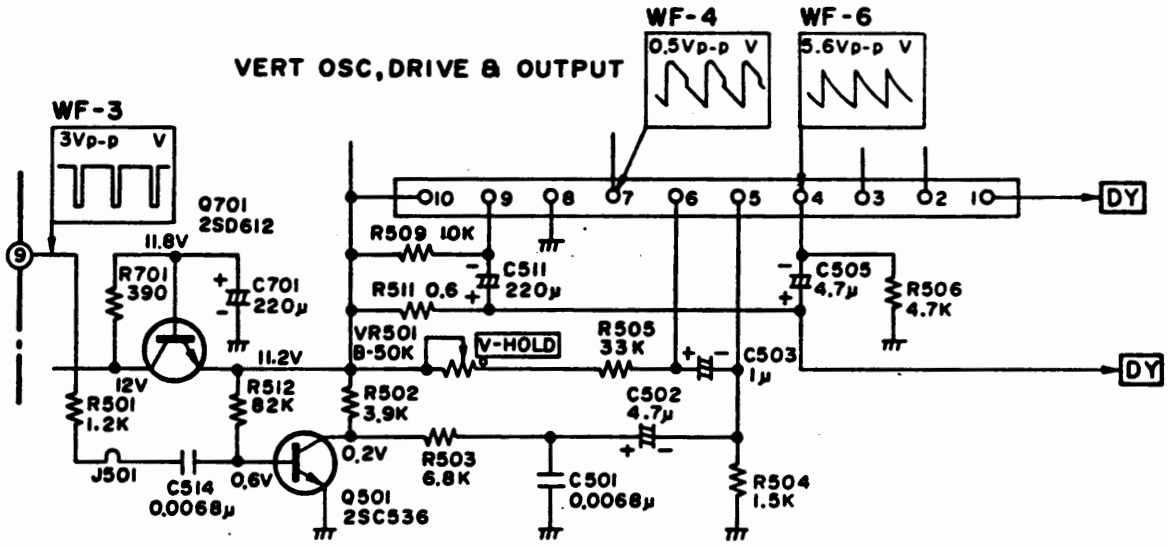
↓

Are the positive vertical synchronous pulses applied to WF-3 ? ——NO——→ Check defective connectors of deflection yoke.

↓ YES

↓

Check VR501.



DO NOT SCALE THIS DRAWING.

	SCALE	TITLE HOW TO REPAIR	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE 20/32
REVISION	CHECKED		

8-5. Improper Vertical Size

Improper vertical size

↓

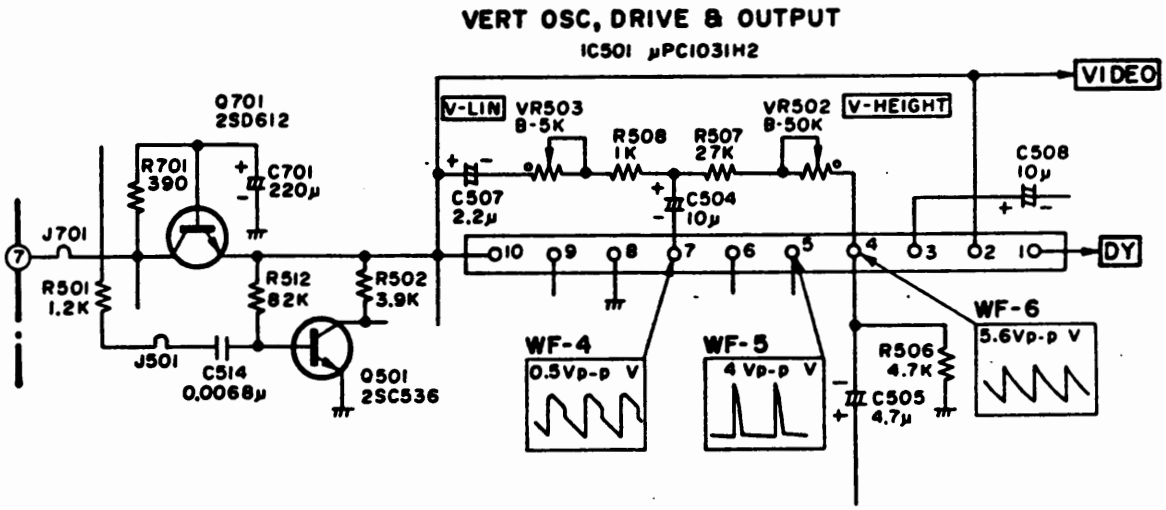
Is normal DC voltage applied to the emitter of Q701 ? ——NO——→ Check Q701.

↓ YES

↓ NO

Check VR502 and VR503

Check IC and its associated circuits : WF-4, 5 and 6



DO NOT SCALE THIS DRAWING.

	SCALE	TITLE HOW TO REPAIR	FILE CODE
	DRAWN	SHEET DDC5NDG	PAGE 21/32
REVISION	CHECKED		

8-6. No Picture

No picture appears.

↓

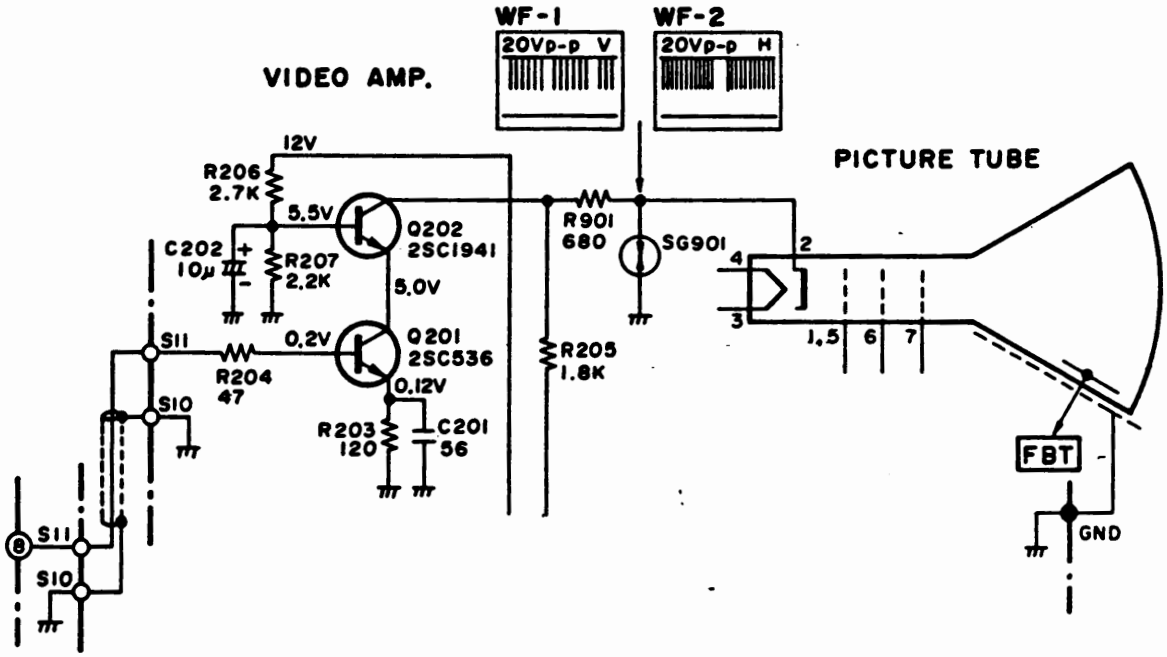
Does raster appear when brightness control is at maximum position ? ——NO——→ Refer to the troubleshooting "No Raster appears".

↓ YES

Are input signals completely supplied ? ——NO——→ Check the signal source.

↓ YES

Check video circuit : WF-1.



DO NOT SCALE THIS DRAWING.

	SCALE	TITLE: HOW TO REPAIR	FILE CODE
	DRAWN	MODEL: DDC5NDG	PAGE / PAGES: 22/32
REVISION	CHECKED		

8-7. Out of Focus

Out of focus

↓

Is normal heating voltage applied to the cathode of CRT ? ——— NO ———→ Check R902.

↓ YES

Is normal video signal injected ——— NO ———→ Check EXT. Control VR.
to Pin-8 of edge connector ?

↓ YES

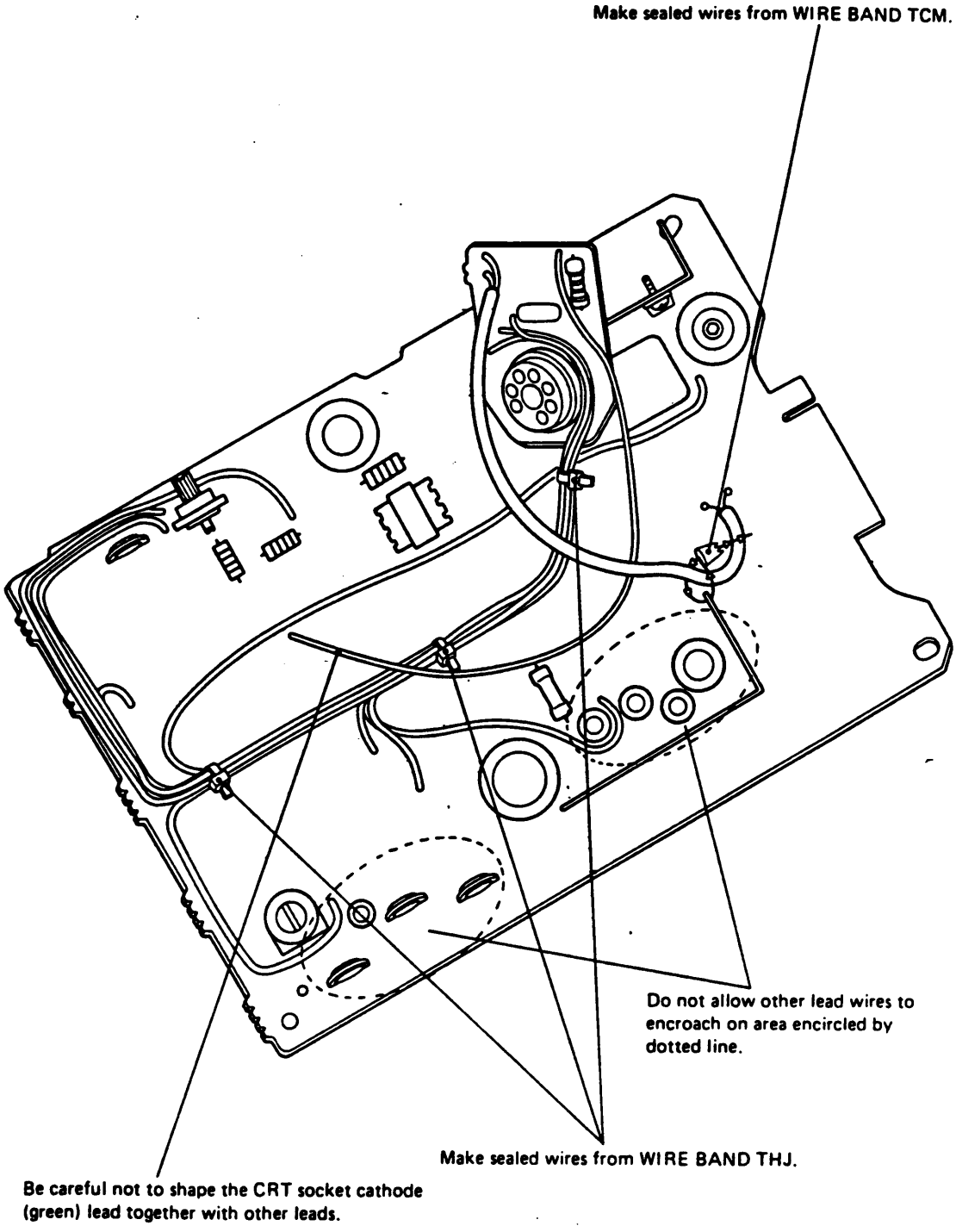
Adjust VR652 for optimum focus.

DO NOT SCALE THIS DRAWING.

	SCALE	TITLE: HOW TO REPAIR	FILE CODE
	DRAWN	MODEL: DDC5NDG	PAGE / PAGES 23/32
REVISION	CHECKED		

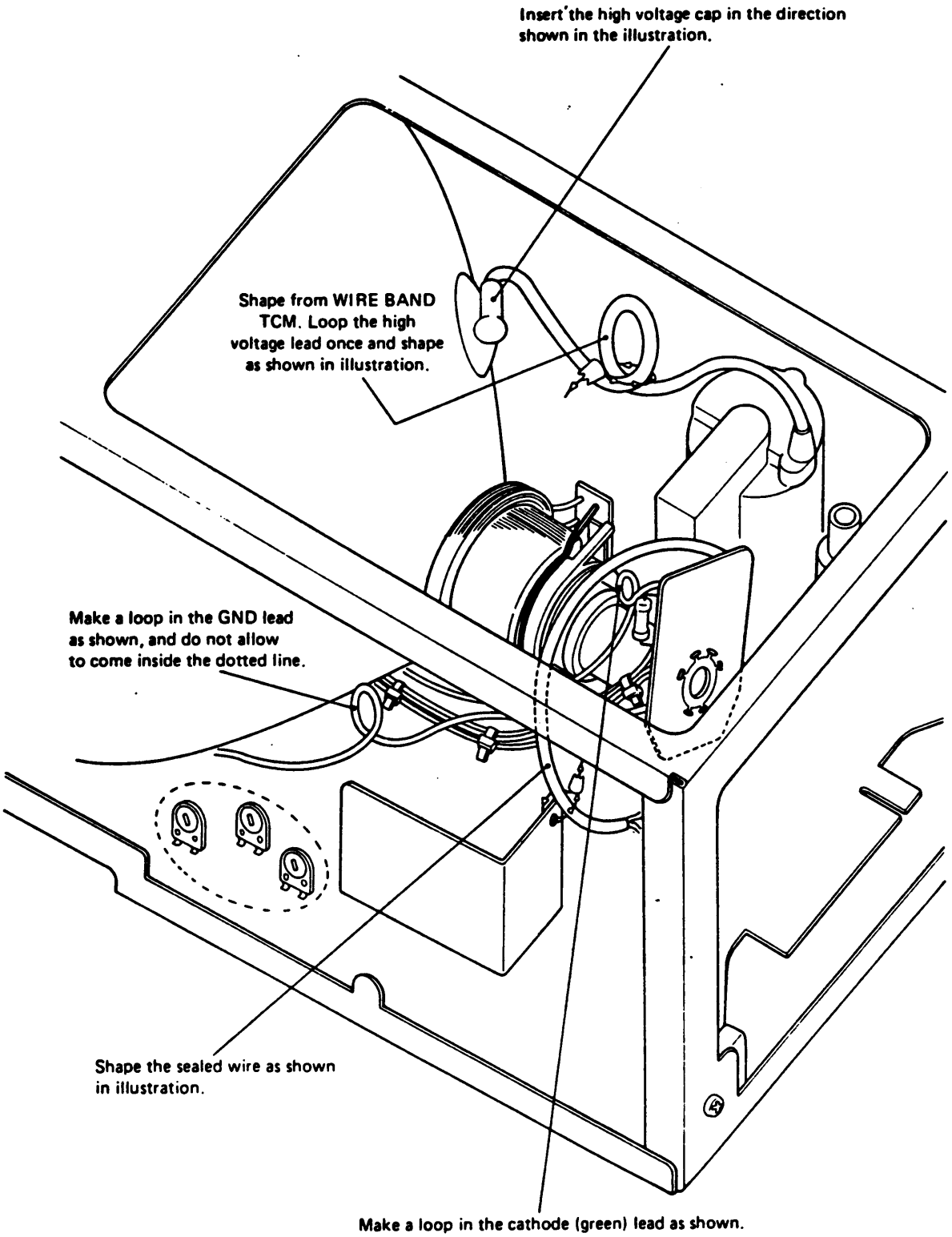
CAUTIONS TO OBSERVE DURING SET-UP

9-1 Configuration Of Lead Wires



DO NOT SCALE THIS DRAWING.

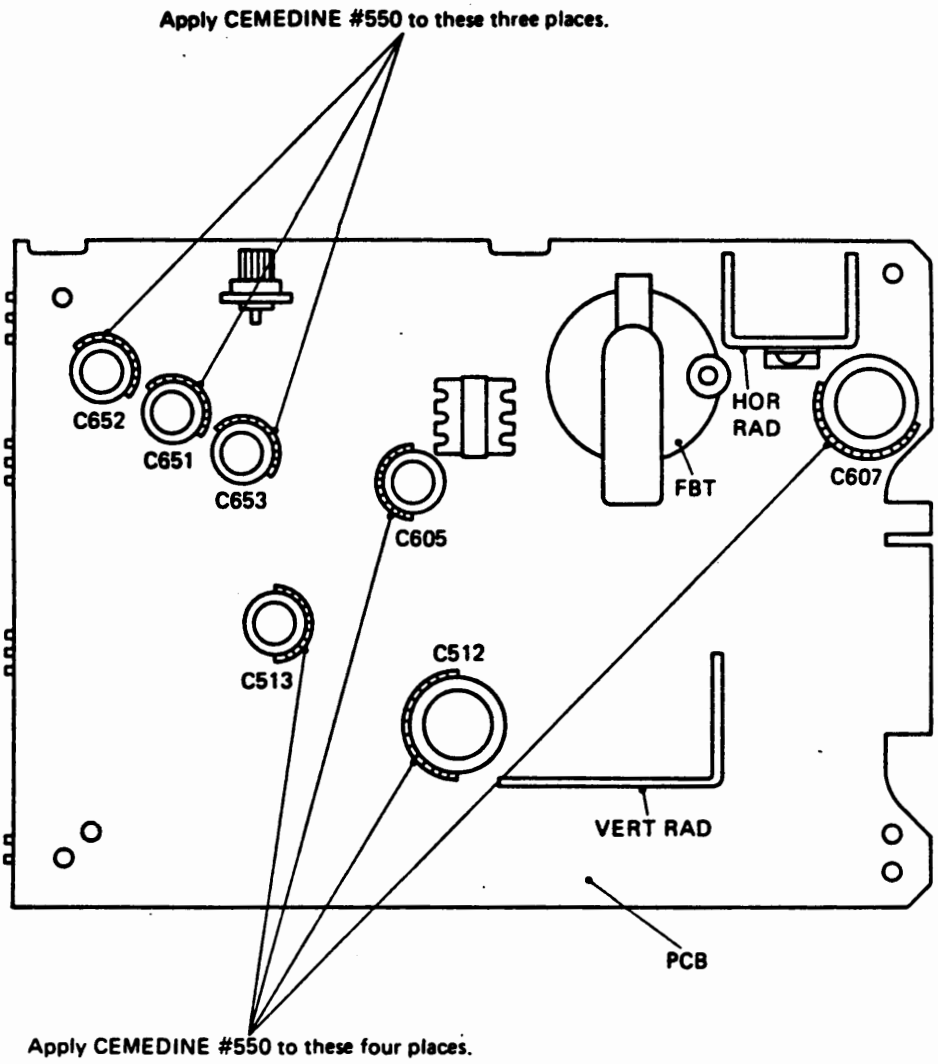
	SCALE	TITLE	FILE CODE
		CAUTION TO OBSERVE DURING SET-UP	
	DRAWN	MODEL	PAGE of PAGES
		DDC5NDG	24/32
REVISION	CHECKED		



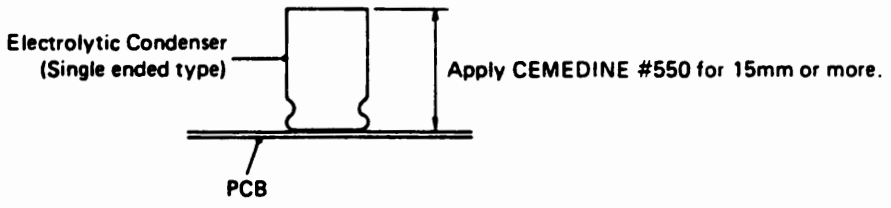
DO NOT SCALE THIS DRAWING.

REVISION	SCALE / DRAWN / APPROVED	TITLE: CAUTION TO OBSERVE DURING SET-UP	FILE CODE
		MODEL: DDC5NDG	PAGE OF PAGES: 25/32

9-2 Where to apply comedine.



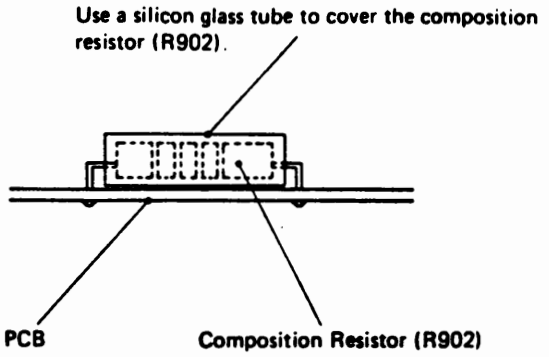
NOTE: When replacing electrolytic condenser (Single ended type), apply CEMEDINE #550 for 15mm or more to the condenser height above the base plate.



DO NOT SCALE THIS DRAWING.

	SCALE	TITLE: CAUTION TO OBSERVE DURING SET-UP	FILE CODE
	DRAWN	MODEL: DDC5NDG	PAGE 26/32
REVISION	CHECKED		

9-3 Where to use a silicon glass tube.



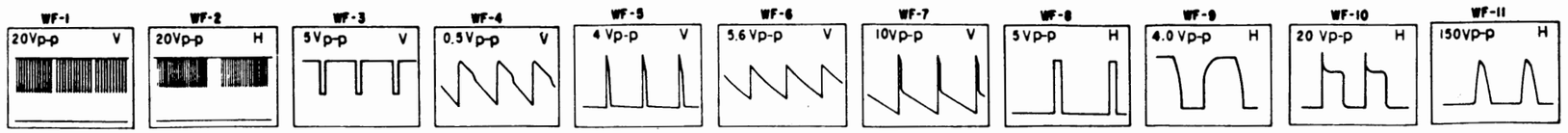
DO NOT SCALE THIS DRAWING.

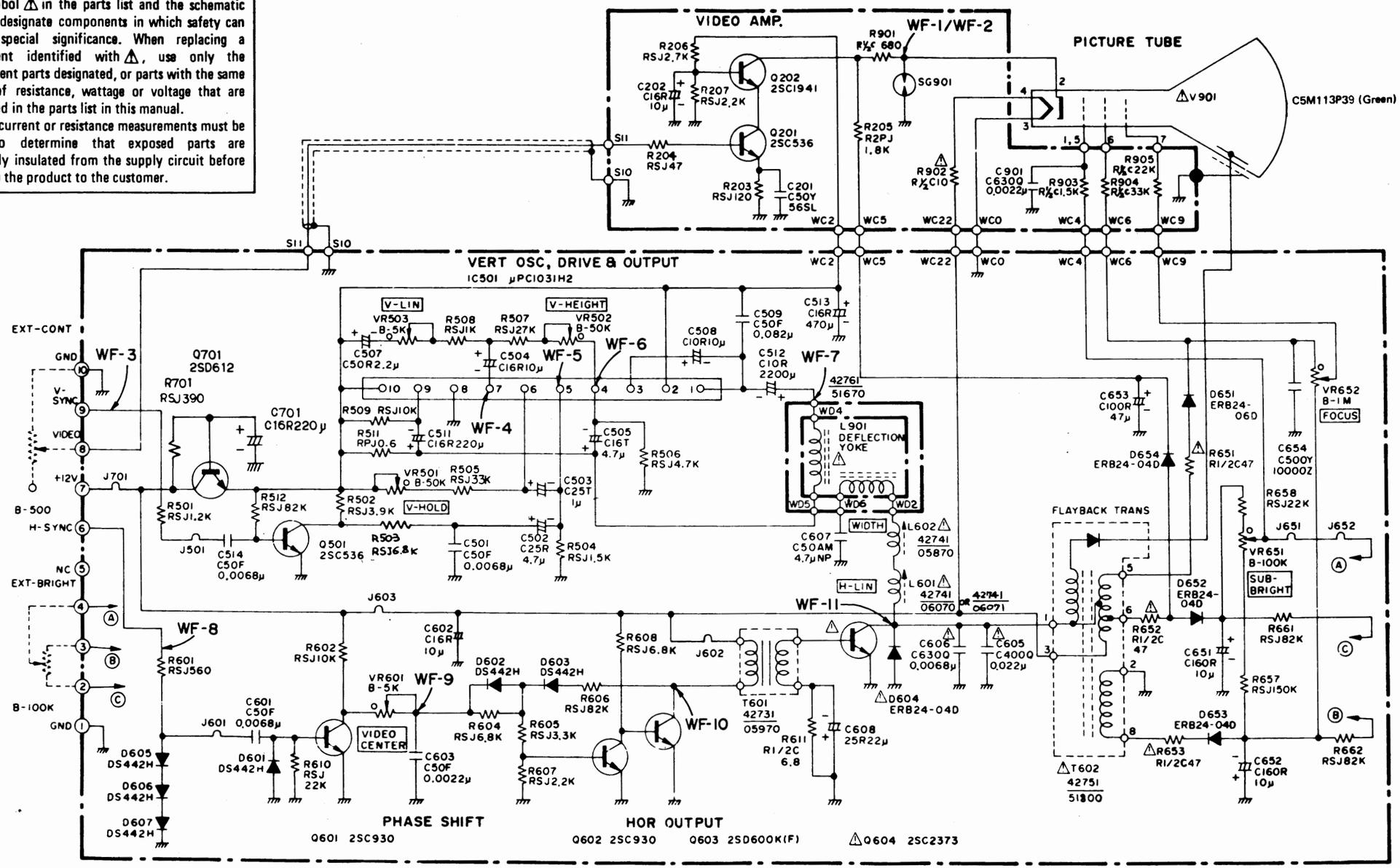
	SCALE	TITLE CAUTION TO OBSERVE DURINGSET-UP	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE OF PAGES 27/32
REVISION	CHECKED		

SCHEMATIC DIAGRAM

PRODUCT SAFETY NOTICE

Each precaution in this manual should be followed during servicing. Components identified with the IEC symbol ⚠ in the parts list and the schematic diagram designate components in which safety can be of special significance. When replacing a component identified with ⚠, use only the replacement parts designated, or parts with the same ratings of resistance, wattage or voltage that are designated in the parts list in this manual.
Leakage-current or resistance measurements must be made to determine that exposed parts are acceptably insulated from the supply circuit before returning the product to the customer.

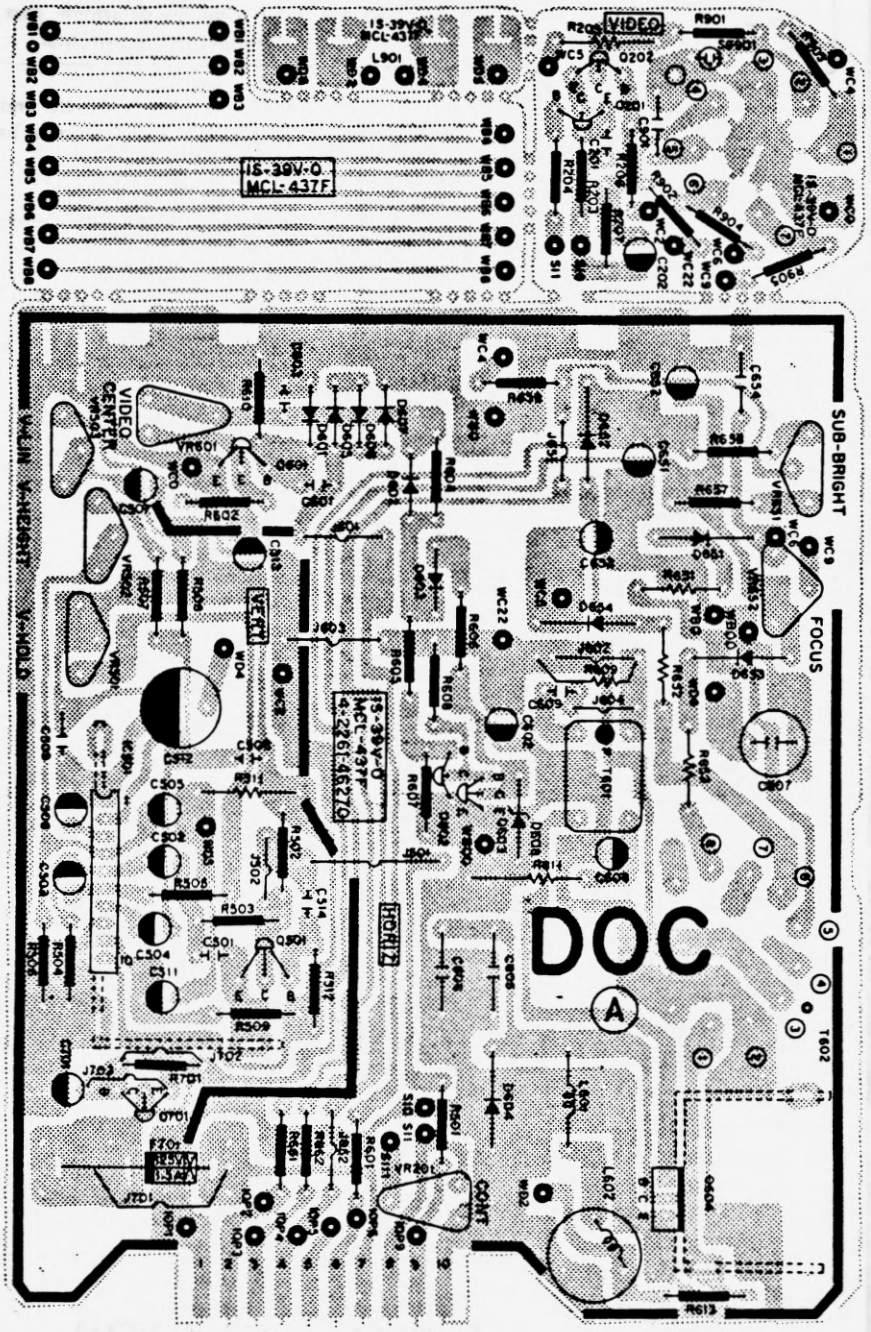




DO NOT SCALE THIS DRAWING.

NOTES:
1. All resistance values in ohm. K=1,000 M=1,000,000
2. Unless otherwise noted in schematic diagram, all capacitors less than 1 are expressed in mfd (μF) and the values larger than 1 are in pF.
3. Voltage reading taken with High Impedance Voltmeter from point indicated chassis ground, contrast at max., other controls at normal, local linevoltage (or specified DC 12V). Voltage reading may vary ±20%.
4. This is a fundamental circuit diagram. Some production changes may be made without revision of the diagram.
5. ⚠ : SAFETY use only equivalent replacement parts.

REVISION	SCALE	TITLE: SCHEMATIC DIAGRAM	FILE CODE
	DRAWN	MODEL: DDC5NDG	PAGE of PAGES: 28/32
	CHECKED		



DO NOT SCALE THIS DRAWING.

	SCALE	TITLE: CIRCUIT BOARD DIAGRAM	FILE CODE
	DRAWN	MODEL: DDC5NDG	PAGE OF PAGES: 29/32
REVISION	CHECKED		

PARTS LIST

PRODUCT SAFETY NOTICE

Each precaution in this manual should be followed during servicing. Components identified with the IEC symbol ⚠ in the parts list and the schematic diagram designate components in which safety can be of special significance. When replacing a component identified with ⚠, use only the replacement parts designated, or parts with the same ratings of resistance, wattage or voltage that are designated in the parts list in this manual.
Leakage-current or resistance measurements must be made to determine that exposed parts are acceptably insulated from the supply circuit before returning the product to the customer.

NOTES: 1. Parts orders must contain Model Number, Parts Number and Description.
2. Ordering quantity of resistors, capacitors and screws must be multiple of 10 pcs.

Schematic Location	Parts No.	Description	Q'ty
CHASSIS PARTS			
	111 2 3121 19870	CHASSIS FRAME-MDK	1
	111 2 3441 17070	CRT MTG BRKT-MDK	1
	111 2 6211 22770	VERT RAD PLATE-TJJ	1
	111 2 6211 23370	AUDIO RAD PLATE-TMB	1
	111 2 6231 16570	GROUNDING TIP-MDK	1
	111 2 7211 13270	WIRE BAND-TCM	2
	111 2 7211 14870	WIRE BAND-THJ-B	3
ACCESSORIES & LABELS			
	111 6 4551 16970	SERIAL NO LABEL	1
	111 6 4761 36170	SPEC LABEL-MDK	1
	111 6 4761 35971	HOR RATE LABEL-MBN	1
	111 6 4761 35971	HOR RATE LABEL-MBN	1
	111 6 4761 35971	HOR RATE LABEL-MBN	2
	111 6 4791 12154	MDL NO. LABEL-MDK	1
	111 6 4791 12154	MDL NO. LABEL-MDK	4
	111 6 4791 13376	CRT IND LABEL-G	4
	111 6 4791 13376	CRT IND LABEL-G	4
SCREW–CHASSIS			
	102 3 2203 00601	SBRT2, 3.0x6, Z1	2
	102 3 2203 00802	SBRT2, 3.0x8, Z1	6
	111 2 4211 15770	COMB TAP SCREW-MBN	4
ELECTRICAL PARTS			
⚠ L601	4 2741 06070	LINEARITY COIL	1
⚠ or	4 2741 06071	LINEARITY COIL	1
⚠ L602	4 2741 05870	WIDTH COIL	1
⚠ L901	4 2761 51670	DEFLECTION YOKE	1
T601	4 2731 05970	HOR DRIVE TRANS	1
⚠ T602	4 2751 51800	FLYBACK TRANS	1
SMALL PARTS			
	4 2261 46270	PC BOARD DOC	1
	4 2350 61600	TERMINAL SOCKET	1
	4 2351 05470	CRT SOCKET	1
	4 2361 05570	GT PIN	1
SG901	4 2341 06270	SPARK GAP	1
or	4 2341 07770	SPARK GAP	1

PARTS LIST

Schematic Location	Parts No.	Description				Q'ty
VARIABLE RESISTORS						
VR501	4 2221 24270	10FFRB-50K				1
VR502	4 2221 24270	10FFRB-50K				1
VR503	4 2221 23970	10FFRB-5K				1
VR601	4 2221 33870	9CVFR9B-5K				1
VR651	4 2221 24370	10FFRB-100K				1
VR652	4 2221 35070	15CHFR7B-1M				1
CAPACITORS						
C201	C1HCDK560SL-	CERAMIC	56P	SL	50V	1
C202	C1CRE-106A--	ELECT	10M		16V	1
C501	C1HFRK682A--	MYLAR	0.0068M		50V	1
C502	C1ERE-475A--	ELECT	4.7M		25V	1
C503	C1ETDM105A--	TANTAL	1M		25V	1
or	C1EUEM105A--	ELECT	1M		25V	1
C504	C1CRE-106A--	ELECT	10M		16V	1
C505	C1CTDM475A--	TANTAL	4.7M		16V	1
or	C1CUEM475A--	ELECT	4.7M		16V	1
C507	C1HRE-225A--	ELECT	2.2M		50V	1
C508	C1CRE-106A--	ELECT	10M		16V	1
C509	C1HFRK823A--	MYLAR	0.082M		50V	1
C511	C1CRE-227A--	ELECT	220M		16V	1
C512	C1ARE-228A--	ELECT	2200M		10V	1
C513	C1CRE-477A--	ELECT	470M		16V	1
C514	C1HFRK682A--	MYLAR	0.0068M		50V	1
C601	C1HFRK682A--	MYLAR	0.0068M		50V	1
C602	C1CRE-477A--	ELECT	470M		16V	1
C603	C1HFRK222A--	MYLAR	0.0022M		50V	1
⚠ C605	C2GQRK223A--	POLYPR	0.022M		400V	1
⚠ C606	C2JQRK682A--	POLYPR	0.0068M		630V	1
C607	C1HAEM009T--	ELECT	4.7M		50V	1
C608	C1ERE-226A--	ELECT	22M		25V	1
C651	C2CRE-106A--	ELECT	10M		160V	1
C652	C2CRE-106A--	ELECT	10M		160V	1
C653	C2ARE-476A--	ELECT	47M		100V	1
C654	C2HYDP103Z--	CERAMIC	0.01M	Z	500V	1
C701	C1CRE-227A--	ELECT	220M		16V	1
C901	C2JQRK222A--	POLYPR	0.0022M		630V	1
FIXED REGISTORS						
R203	R2ESPJ121A	CARBON	120		1/4W J	1
R204	R2ESPJ470A	CARBON	47		1/4W J	1
R205	R3DXPJ182A	OXIDE-M	1.8K		2W J	1
R206	R2ESPJ272A	CARBON	2.7K		1/4W J	1
R207	R2ESPJ222A	CARBON	2.2K		1/4W J	1
R501	R2ESPJ122A	CARBON	1.2K		1/4W J	1
R502	R2ESPJ392A	CARBON	3.9K		1/4W J	1
R503	R2ESPJ682A	CARBON	6.8K		1/4W J	1
R504	R2ESPJ152A	CARBON	1.5K		1/4W J	1
R505	R2ESPJ333A	CARBON	33K		1/4W J	1
R506	R2ESPJ472A	CARBON	4.7k		1/4W J	1
R507	R2ESPJ273A	CARBON	27K		1/4W J	1
R508	R2ESPJ102A	CARBON	1K		1/4W J	1

DO NOT SCALE THIS DRAWING.

	SCALE	TITLE PARTS LIST	FILE CODE
	DRAWN	MODEL DDC5NDG	PAGE OF PAGES 31/32
REVISION	CHECKED		

PARTS LIST

Schematic Location	Parts No.	Description				Q'ty
R509	R2ESPJ103A	CARBON	10K	1/4W	J	1
R511	R3APPJ0R6A	OXIDE-M	0.6	1W	J	1
R512	R2ESPJ823A	CARBON	82K	1/4W	J	1
R601	R2ESPJ561A	CARBON	560	1/4W	J	1
R602	R2ESPJ103A	CARBON	10K	1/4W	J	1
R604	R2ESPJ682A	CARBON	6.8K	1/4W	J	1
R605	R2ESPJ332A	CARBON	3.3K	1/4W	J	1
R606	R2ESPJ823A	CARBON	82K	1/4w	J	1
R607	R2ESPJ222A	CARBON	2.2K	1/4W	J	1
R608	R2ESPJ682A	CARBON	6.8K	1/4W	J	1
R610	R2ESPJ223A	CARBON	22K	1/4W	J	1
R611	R2HCPJ6R8A	SOLID	6.8	1/2W	J	1
⚠ R651	R2HCPK470A	SOLID	47	1/2W	K	1
⚠ R652	R2HCPK470A	SOLID	47	1/2W	K	1
⚠ R653	R2HCPK470A	SOLID	47	1/2W	K	1
R657	R2ESPJ154A	CARBON	150K	1/4W	J	1
R658	R2ESPJ223A	CARBON	22K	1/4W	J	1
R659	R2ESPJ153A	CARBON	15K	1/4W	J	1
R661	R2ESPJ823A	CARBON	82K	1/4W	J	1
R662	R2ESPJ823A	CARBON	82K	1/4W	J	1
R701	R2ESPJ391A	CARBON	390	1/4W	J	1
R901	R2HCPK681A	SOLID	680	1/2W	K	1
⚠ R902	R2HCPK100A	SOLID	10	1/2W	K	1
R903	R2HCPK152A	SOLID	1.5K	1/2W	K	1
R904	R2HCPK333A	SOLID	33K	1/2W	K	1
R905	R2HCPK223A	SOLID	22K	1/2W	K	1

TUBES & SEMICONDUCTORS

D601	4 2021 21070	SI DIODE DS442H	1
D602	4 2021 21070	SI DIODE DS442H	1
D603	4 2021 21070	SI DIODE DS442H	1
⚠ D604	4 2021 10270	SI DIODE ERB24-04D	1
D605	4 2021 21070	SI DIODE DS442H	1
D606	4 2021 21070	SI DIODE DS442H	1
D607	4 2021 21070	SI DIODE DS442H	1
D651	4 2021 10470	SI DIODE ERB24-06D	1
D652	4 2021 10270	SI DIODE ERB24-04D	1
D653	4 2021 10270	SI DIODE ERB24-04D	1
D654	4 2021 10270	SI DIODE ERB24-04D	1
IC501	4 2061 08670	IC-UPC1031H2	1
Q201	TG2SC536-----	SI TR 2SC536	1
Q202	TN2SC1941----	SI TR 2SC1941	1
Q501	TG2SC536-----	SI TR 2SC536	1
Q601	TG2SC930-----	SI TR 2SC930NP	1
Q602	TG2SC930-----	SI TR 2SC930NP	1
Q603	TG2SD600K-F--	SI TR 2SD600K	1
⚠ Q604	TN2SC2373---5	SI TR 2SC2373-5	1
Q701	TG2SD612-----	SI TR 2SD612	1
⚠ V901	QTME2765B4LNS	CRT E2765B4(LG)-HT White (DC6005NL)	1
⚠ V901	QTME2765B31LN	CRT E2765B31(LG)-HT Green (DC6105NL)	1
⚠ V901	QTME2765B31LS	CRT E2765B31(LG) Green (DC6105NL)	1
⚠ or	QNMC5M113P39S	CRT C5M113P39 Green (DDC5NDG)	1

DO NOT SCALE THIS DRAWING.

		PARTS LIST	
		DDC5NDG	32/32
REVISION			