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Part 1

651S-1/1A General Purpose HF Receiver

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651S-1/1A General Purpose HF Receiver

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description and principles of operation

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description and principles of operation

1. GENERAL

The 651S-1/651S-1A (figure 1) is a triple-conversion superheterodyne receiver that provides 297,500 channels in the 250-kHz to 29.9999-MHz frequency range. It is a completely solid-state desk-top receiver and features direct-reading digital display of the operating frequency.

The standard operating modes of the 651S-1/1A are AM, SSB, and CW. Standard if filter bandwidths are 6 and 16 kHz, 2.7 kHz USB, and 2.7 kHz LSB.

Optional operating modes are narrow-band FM and ISB (independent sideband). Additional if filters are available and are described in paragraph 5. Including standard bandwidths, as many as eight if bandwidths are available. The optional operating modes and bandwidths require additional or different plug-in circuit cards for implementation.

Frequency coverage can be extended down to 12 kHz by use of an optional VLF converter. The vlf converter is part of special plug-in rf module (A6) that is used in place of the standard rf module normally supplied. In addition an optional frequency scan (automatic frequency scan) capability is available with the addition of a special card. The 651S-1/1A is capable of operation with narrow-band secure voice vocoder systems (NBSV) and radioteletypewriter systems (RTTY).



NOTE:
SILK-SCREEN ON BANDWIDTH SWITCH MAY VARY FOR THE DIFFERENCE PART NUMBERS OF THE 651S-1. THE APPEARANCE OF THE 651S-1A IS IDENTICAL TO THE 651S-1 EXCEPT FOR TYPE NUMBER AND AND SILK-SCREEN ON BANDWIDTH SWITCH.

TP3-0870-017

651S-1/1A General Purpose HF Receiver
Figure 1

All controls necessary for complete local operation are on the front panel of the receiver; however, remote control options are available. Two types of remote control are possible, Collins 3-pair serial digital control and teletypewriter-coded control.

To use Collins 3-pair serial digital control, the interconnect card must be removed and two cards added: the DCFE (device control functional element) card and the DCU (device control unit) card. With these cards installed, one or more receivers can be controlled by a digital processor such as the Collins 8311A-1 or 8311B-1.

To use Collins teletypewriter-coded control, the interconnect card must be removed and two cards added: the DCFE card and the TCU (teletypewriter control unit) card. With these cards installed, the 651S-1/1A can be remotely controlled using a Collins 514S-1 Remote Control Unit. Table 1 lists the 651S-1/1A configuration and the optional cards included in each configuration. Paragraph 5 describes the variations. A 115- or 230-Vac power cable is supplied with each configuration as required.

Table 2 lists external equipment required for a completely operable receiver and optional equipment available for special applications.

Table 3 lists the electrical and environmental characteristics and limitations of the 651S-1/1A.

2. PHYSICAL DESCRIPTION

The 651S-1/1A (figure 2) is a desk-top model receiver featuring completely solid-state design. A 19-inch speaker panel is available to rack mount the receiver (table 2). Refer to the installation section for mounting details. All the controls for manual operation are on the front panel and all points for external wiring/connections are on the rear panel, except the headset connection point on the lower front panel. Refer to the operation section for details.

The top-front panel is of black glass for good visibility of the electronic digital frequency display and the af/rf level meter.

The 651S-1/1A contains a sheet-metal chassis with removable module/card construction. A ventilated cover allows airflow into the bottom and out the back.

The circuit cards and the shielded rf module slide into a metal card cage. Space between the card cage and the dust cover allows air circulation. The 2-speed fan is thermostatically controlled.

The unit is 6.25 inches (15.9 cm) high (less mounting feet), 13.2 inches (33.5 cm) wide, 15.8 inches (40.1 cm) deep (less knobs), and weights 30.2 pounds (13.7 kg).

3. ELECTRICAL DESCRIPTION

The 651S-1/1A incorporates a unique method of tuning. It tunes in discrete 100-Hz steps: tuning information is derived from a 22-bit binary coded decimal (bcd) accumulator. Operating frequency is selected manually or by 3-pair digital remote control.

For manual tuning, three front-panel tuning knobs select the desired operating frequency in steps of 1 MHz, 0.1 MHz, and 100 Hz. These control switches drive the accumulator that consists of six up-down bcd counters.

In typical operation the 1-MHz and 0.1-MHz controls are used to enter the proper band and the 100-Hz control is used for fine tuning. The selected frequency information is applied to the frequency synthesizer cards and the numeric frequency display tubes.

The 100-Hz tuning control is an infrared photoelectric tuning switch that produces two square-wave outputs in quadrature when the shaft is turned. Card A14 determines the direction of rotation from these pulses and sends up or down pulses to the synthesizer. Two infrared emitters generate light that is interrupted by opaque lines screened on a transparent disc.

An optional keep-alive power circuit is available. In receivers that have this special circuit, a 6- to 8-Vdc battery can be connected to a terminal strip at the rear of the receiver. The battery will supply keep-alive power to frequency control card A14 so a temporary power loss will not cause a loss of frequency information.

Operation of the frequency circuits for remote control applications is the same as local control except for the method of driving frequency control card A14. Using 3-pair serial digital control, all functions and frequency selection can be controlled by a processor. Up to 30

Table 1. 651S-1/1A Configuration.

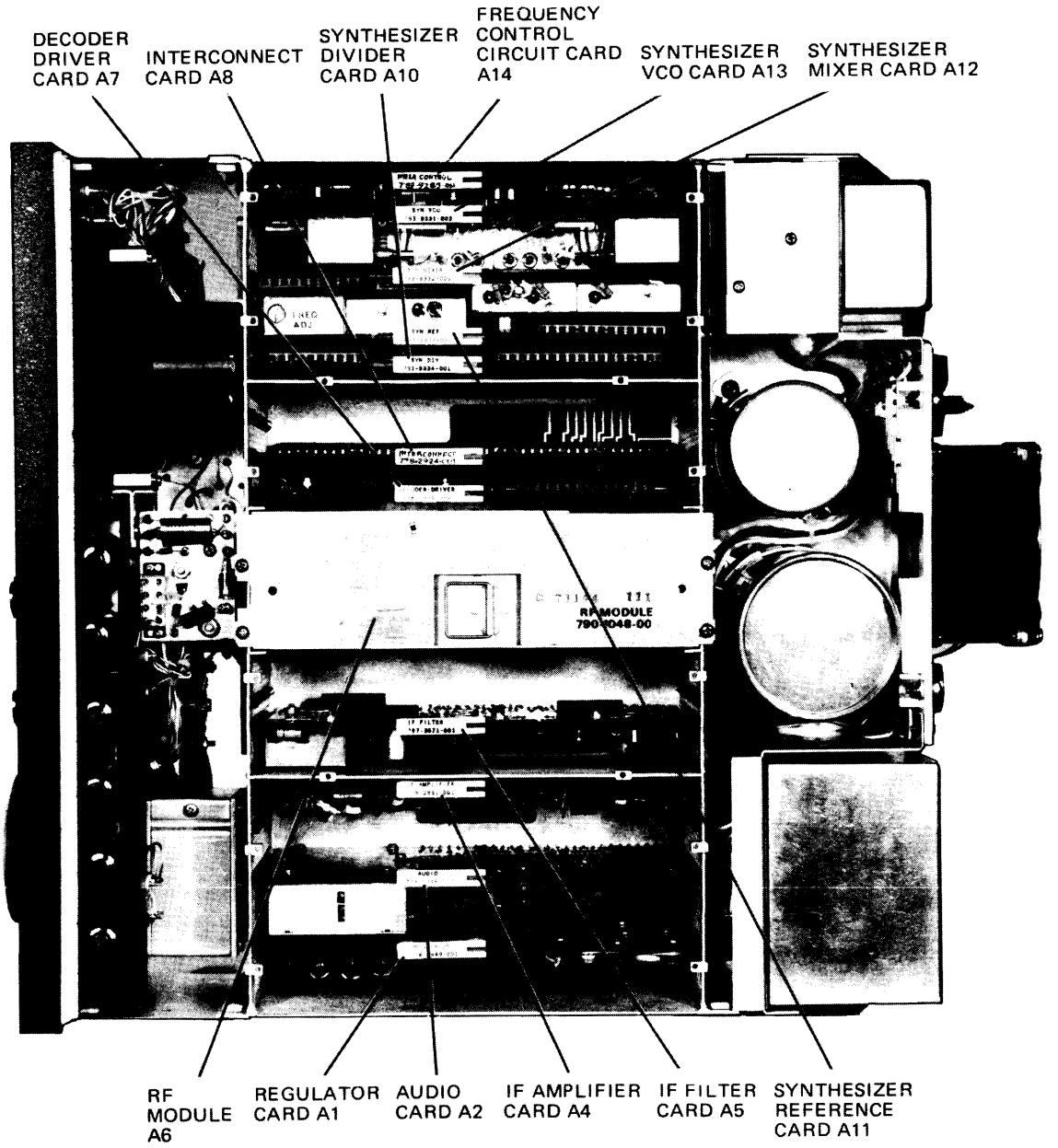
NOTES: 1. Power supply regulator card A1 (778-2949-001), synthesizer reference card A11 (793-9333-002), synthesizer mixer card A12 (793-9332-002), synthesizer vco card A13 (793-9331-003), and frequency control card A14 (783-9283-001) are used in all 651S-1/1A's.
2. Scan card 783-9368-001 is used in special applications of the 651S-1/1A.
3. Audio card *-003 is the current production model effectivity CI-72373.

TYPE	CONTROL TYPE	MODES/ BANDWIDTHS			OPT SQUELCH	OPT ISB	OPT VLF	FRONT PANEL COLOR	OPT IF FREQ	SUBASSEMBLY PN / 651S-1 PN 522-4836-	CHASSIS 606-9423-	AUDIO CARD A2 778-2948-	ISB CARD A3 778-2952-001	IF AMPLIFIER CARD A4 778-2951-	IF FILTER CARD A5A1 797-3571-	FILTER CARD A5A2 797-3585-	RF MODULE A6 790-1048-	DECODER/DRIVER CARD A7 778-2928-003	DECODER/DRIVER CARD A7 608-9087-001	DECODER/DRIVER CARD A7 608-9121-001	INTERCONNECT CARD A8 778-2924-	DCFE CARD A8 624-5744-001	DCU CARD A9 793-9414-001	DCU CARD A9 624-5781-001	DCU CARD A9 (HI-SPEED) 774-7842-001	TCU CARD A9 783-9480-001	SYNTHESIZER DIVIDER CARD A10 793-9334-
		STD	OPT AM	OPT CW																							
651S-1 -102 series (Cont)	Local control	16 kHz and 6 kHz AM; 2.7 kHz LSB; 2.7 kHz USB	3 kHz	1.1, 0.5, and 0.37 kHz	Squelch	No ISB	No vlf	Black	450 kHz if	004	005	002		001	001	010	008	X			006						002
					No squelch					104	003	003		001	001	002	008	X			006						002
			3 kHz	1.0, 3.0, and 0.2 kHz		ISB				110	003	003	X	001	001	003	008	X			004						002
						No ISB				111	003	003		001	001	003	008	X			004						002
					Squelch					121	005	002		001	001	003	008	X			004						002
						ISB				122	005	002	X	001	001	003	008	X			004						002
				0.5 kHz	No squelch		Vlf			106	003	003	X	001	001		008	X			004						002
						No ISB				102	003	003		001	001		008	X			004						002
					Squelch		No vlf			120	003	003		001	001		010	X			004						006
								Gray		124	005	002		001	001		008	X			004						002
					No squelch					126	003	003		001	001		008	X			004						002
			3 kHz	0.320, 1.1 and 3 kHz				Black		134	003	003		001	001	010	008	X			004						002
				0.2, 0.5, 1.0 and 3 kHz			Vlf			132	003	003		001	001	003	010	X			004						006
						ISB				133	003	003	X	001	001	003	010	X			004						006
				4.0, 2.0, and 1.1 kHz		No ISB			455.5 kHz	128	003	005		001	007	011	008	X				X		X			002
	Processor control			1.0, 3.0, and 0.2 kHz						107	003	003		001	001	003	008	X				X	X				002
						ISB	No vlf			108	003	003	X	001	001	003	008	X				X	X				002
										113	006	003		003	001	003	008	X				X	X				002
				0.5 kHz	Squelch				450 kHz if	125	005	002		001	001		008	X				X	X				002
					No squelch	No ISB				103	003	003		001	001		008	X				X	X				002
			3 kHz	0.5, 1.1 and 3 kHz						129	003	003		001	001	012	008	X				X	X				002

Table 1. 651S-1/1A Configuration (Cont).

NOTES: 1. Power supply regulator card A1 (778-2949-001), synthesizer reference card A11 (793-9333-002), synthesizer mixer card A12 (793-9332-002), synthesizer vco card A13 (793-9331-003), and frequency control card A14 (783-9283-001) are used in all 651S-1/1A's.
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		STD	OPT AM	OPT CW																							
651S-1 -102 series (Cont)	Processor control	16 kHz and 6 kHz AM; 2.7 kHz LSB; 2.7 kHz USB	3 kHz	0.2, 0.5, 1.0, and 3 kHz	Squelch	ISB	No vlf		450 kHz if	131	005	002	X	001	001	003	008	X				X					002
							Vlf			135	005	002	X	001	001	003	010	X				X					006
	Teletypewriter control			0.5 kHz		No ISB				123	003	003		001	001		008	X				X				X	002
651S-1 -152 series	Local control				No squelch	No ISB	No vlf	Black	455.0 kHz if	152	007	*003		004	010		020		X		004						002
						ISB				156	007	*003	X	004	010		020		X		004						002
			3 kHz	0.370, 0.5, 1.1 and 3 kHz		No ISB				154	007	*003		004	012	010	020		X		006						002
				0.5, 1.1, and 3 kHz		ISB				180	007	*003		004	011	012	020		X		007						002
										181	007	*003	X	004	011	012	020		X		007						002
							Vlf			182	007	*003		004	011	012	021		X		007						006
	Processor control									153	007	*003		004	010		020		X			X		X			002
										179	007	*003		004	010				X			X			X		002
			3 kHz	0.2, 0.5, and 3 kHz		No ISB	No vlf			183	006	*003		003	011	003	020			X		X		X			002
				1, 2, 3, and 4 kHz					455.5 kHz if	184	009	005		003	007	011	020		X			X		X			002
	Teletypewriter control								455.0 kHz if	173	007	*003		004	010		020		X			X				X	002
651S-1A	Local control		3 kHz	1.1, 0.5, and 0.37 kHz	Squelch					622-1062-001	005	004		004	006	010	020			X	006						002



Subassembly Location
Figure 2

Table 2. Required or Optional Equipment.

ITEM	USE	RECOMMENDED TYPE
Headset or Speaker } Required for a completely operable receiver	Audio output.	Headset: Collins HS-1 600 ohms unbalanced, 3 watts minimum or equivalent Speaker: 8 ohms, 4 watts capability
4800-bit/s serial digital remote control	Optional remote operation.	Collins 8311A-1 or 8311B-1 Device Control Computer system
Mount/speaker panel	Rack mount/audio output.	Collins 699J-1 Speaker Panel
Teletypewriter-coded control	Optional remote operation.	Collins 514S-1 Remote Control Unit
Auto scan control panel	Optional remote frequency scan operation.	Auto scan control panel, Collins pn 620-9030-001
Auto scan control	Optional frequency scan operation.	Collins pn 609-1565-001
Modification kit		
Plate, switch	Installed over REMOTE CONTROL switch on front panel.	Collins pn 609-0944-001
Adapter card	Installed in place of auto scan card to permit normal operation without restrapping the 651S-1/1A sideboard.	Collins pn 609-1554-001
*Auto scan control card	Provides automatic scanning of preset receiver frequencies.	Collins pn 783-9368-001
*Also available as an end item.		

receivers can be controlled by one processor. To use 3-pair digital control, the DCFE card is mounted in place of interconnect card A8 and DCU card A9 is added. Three twisted pairs of input wires provide the interface between the receiver and the remote control processor. All information is fed to the optional DCU and DCFE cards that override all manual controls (except audio gain) and automatically set up the 651S-1/1A for operation. The input is a 32-bit control word on a 4800-Hz or 76.8-kHz (for hi-speed DCU) biphase modulated format. The DCU must be strapped for proper addressing (refer to paragraph 4.1 of the operation section for details).

For 514S-1 remote control operation, the DCFE card is mounted in place of interconnect card A8 and TCU card A9 is added. Three pairs of input wires provide the interface between the receiver and the 514S-1. One pair of wires is for the audio lines; the other two pairs are for standard 20-mA teletypewriter loops. External jumpers may be used to wire the system for a single teletypewriter loop. Up to 15 receivers can be controlled by strapping 4 wires on the TCU for proper addressing (refer to the operation section paragraph 4.2 for details).

Independent sideband (ISB) operation is optional on the 651S-1/1A. ISB if amplifier card A3 is required for this option. In ISB operation, both USB and LSB filtering circuits are enabled and the stronger of the USB and LSB signals controls the rf AGC level for the front end of the receiver. Separate audio and if output points are on the rear chassis for ISB signals.

To obtain frequency scanning capability, auto scan card A9 (783-9368-001) is available. This card contains all the required circuits to provide frequency scan operation.

Table 3. Equipment Specifications.

CHARACTERISTIC	LIMITATIONS
	Note All voltages are "hard" volts, that is, open circuit voltage from 50-ohm resistive source, unless otherwise specified.
Frequency range	250 kHz to 29.9999 MHz; 12 kHz to 29.9999 MHz optional.
Frequency control	Phase locked in 100-Hz steps. Provisions for interpolation in 10-Hz steps.
Frequency stability	5 parts in 10^7 total.
Frequency adjustment	1-MHz and 0.1-MHz steps by rotary switches. 100-Hz steps by continuous tuning control. May be controlled remotely by Collins 3-pair serial digital method (optional) or by Collins 514S-1 Remote Control Unit.
Frequency readout	7-bar segment tubes, six places.
Modes	
Standard	AM, SSB, and CW.
Optional	Narrow-band FM, ISB (independent sideband)
Bandwidth	PASSBAND (3 dB) — REMARKS
Standard	16 kHz (nominal) — AM 6 kHz (-6 dB) — AM 2.7 kHz — LSB 2.7 kHz — USB
Optional	0.2 kHz — Increased selectivity for CW 0.370 kHz — Center frequency ±2 kHz, suitable for RTTY. 0.5 kHz — Increased selectivity for CW. 1.0 kHz — CW. 3.0 kHz — Suitable for narrow-band AM. 1.1 kHz — Center frequency +2 kHz suitable for RTTY. 2.0 kHz — Increased selectivity for CW. 4.0 kHz — Increased selectivity for CW.
Sensitivity for 10-dB signal-to-noise ratio	
0.250 to 0.4 MHz	SSB: 5 μV (2.7 kHz bandwidth) AM: 35 μV (6 kHz bandwidth)
0.4 to 1.999 MHz	SSB: 2.5 μV (2.7 kHz bandwidth) AM: 10 μV (6 kHz bandwidth)
2.0 to 29.9999 MHz	SSB: 0.7 μV (2.7 kHz bandwidth) AM: 3.5 μV (6 kHz bandwidth) NBFM: 1 μV (12 dB SINAD)
(Cont)	

Table 3. Equipment Specifications (Cont).

CHARACTERISTIC	LIMITATIONS
Sensitivity for 10-dB signal-to-noise ratio (Cont)	
12 to 559.9 kHz (50-ohm input) (with optional vlf converter)	SSB: 2.5 μV (2.7 kHz bandwidth) AM: 12 μV (6 kHz bandwidth)
Gain	In SSB, 3 μV produces 0.5 W of audio into 8-ohm load or 1 mW (0 dBm) into 600-ohm line output.
Audio output power	2 W into 8-ohm load at speaker terminal, with not more than 3% total distortion, 5-mW peak (+7 dBm), at 600-ohm line output with not more than 1% total distortion.
Audio output impedance	8 ohms nominal at speaker terminal, 600 ohms nominal at headphone jack. 600 ohms on line audio outputs, balanced, center tapped.
Audio response (600-ohm line audio)	With 1 dB from 100 Hz to 4 kHz. (If filter response will further modify overall receiver response; for example, 2.7-kHz SSB filter response is -3 dB from 350 Hz to 3050 Hz.)
If output	50 mV at 450-kHz, 50-ohm load. Same for the ISB channel.
Audio hum and noise	At least 40 dB below maximum output.
Antenna input impedance	50 ohms nominal unbalanced.
Automatic gain control	
Audio rise	No more than 6 dB for input signal of 3 μV to 0.3 V.
Release time	100 ms or 1 s, switchable. AGC can be disabled.
Cross modulation (-10 dB, 30% modulation with 50 μV desired signal)	±50 kHz from operating frequency, 0.35 V; ±10% from operating frequency, 0.50 V.
Spurious response, internal	Not more than 2 μV (except at 0.9, 9.9, 19.8, and 20.7 MHz not more than 10 μV).
Squelch (optional)	Adjustable squelch.
Bfo	Fixed 450 kHz bfo; derived from reference oscillator of synthesizer. Variable 450-kHz bfo may be tuned ±900 Hz in CW mode. SSB mode bfo tunes ±60 Hz in 10-Hz steps to interpolate between 100-Hz positions.
Antenna input protection	Overload diodes provide protection against strong signals up to 10 volts rms.
Metering	Front panel meter measures rf signal level in decibels above 1-μV input signal, or 600-ohm audio line level in dBm.
MTBF	3,000-h field operation.
Mounting	19-in (48.3 cm) rack panel kit or table top.

Table 3. Equipment Specifications (Cont).

CHARACTERISTIC	LIMITATIONS
Temperature	0 °C to +55 °C (+32 °F to +131 °F).
Humidity	90%.
Altitude	9144 m (30,000 ft).
Power requirements	115/230 V ±10%, 47 to 63 Hz, 70 W. An additional 40 W may be required to power optional circuits. Optional external battery for keep-alive function, +6 to +8 V, 1 A.

To obtain the optional if filter bandwidths, filter FL1 (mounts on if filter card A5A1) and/or subcard A5A2 (mounts on if filter card A5A1) is available. This subcard contains the additional desired optional filters.

4. PRINCIPLES OF OPERATION

4.1 Overall Operation

4.1.1 Signal Operation, Standard Configuration (Refer to figure 3.)

The received signal is routed through a 30-MHz low-pass filter that attenuates images and spurious responses. The signal is then applied through one of the diode-switched bandpass filters, depending on the operating frequency and rf module A6 being used. On Collins part numbers 790-1048-008/-010, there are 10 band-pass filters: the filter ranges are 0 to 0.5599 MHz, 0.56 to 1.9999 MHz, 2.0 to 2.9999 MHz, 3.0 to 3.9999 MHz, 4.0 to 5.9999 MHz, 6.0 to 7.9999 MHz, 8.0 to 11.9999 MHz, 12.0 to 15.9999 MHz, 16.0 to 23.9999 MHz, or 24.0 to 29.9999 MHz. On Collins part number 790-1048-020/-021, there are three bandpass filters: 0 to 0.5599 MHz, 0.56 to 1.9999 MHz, or 2.0 to 29.9999 MHz.

After proper bandpass filtering, the received signal is mixed with variable injection of from 79.3501 to 109.10 MHz to produce 109.35 MHz. This signal is applied through a 109.35-MHz crystal filter with 16-kHz bandwidth to a second mixer. At this stage the 109.35-MHz signal is mixed with a 99-MHz injection signal to produce 10.35 MHz. This signal is amplified and applied through either an 8-dB pad or one of three 10.35-MHz crystal filters. The crystal filters (various bandwidths) are used in cascade with mechanical filters to provide selectivity and good signal-to-noise ratio for various bandpass options of CW and AM operation. When 16-kHz bandwidth is desired, the 8-dB pad is inserted to maintain a nominal signal level.

The 10.35-MHz signal is mixed with 9.9 MHz to produce 450 kHz. It is then applied through one of three 450-kHz mechanical filters (USB, LSB, or AM) or a crystal filter (narrow-band CW mode), or the filters are bypassed (when 16-kHz bandwidth is desired). The inputs and outputs to and from the filters are FET switched.

The 450-kHz signal then goes through several stages of if amplification and if AGC is applied at these points to control the receiver gain. The signal path branches after three stages; part goes to an if output strip, part is used for SSB audio detection, part is used for AM and AGC detection, and part is used for FM detection.

The if output portion goes through three more stages of amplification and is applied to a rear connector for monitoring.

The signal portion for SSB product detection is amplified one more time to complete the step-up in the if strip. This output is applied with the bfo signal to a dual-gate FET to produce SSB audio. The signal portion for AM audio and AGC is applied to a 2-stage AGC amplifier. Its output is transformed and then demodulated by an emitter follower and used as AM audio and AGC. The FM signal is picked off at a high-level point in the 2-stage AGC amplifier and applied to an FM limiter/discriminator circuit.

All the audio signals are applied to the audio amplifier card. Specific enabling gate signals determine which mode audio signal is to be amplified; that is, AM enable, CW enable, etc. The audio is amplified in several stages and the

5-mW output from a 600-ohm transformer output is applied to a rear chassis terminal strip for external power amplification. Audio is also applied through the front panel volume control to a power amplifier circuit. This audio signal is amplified to provide a 20-W average into an 8-ohm speaker, and to provide an audio output for headphones.

Also contained on the audio card are variable bfo circuits and optionally, audio squelch circuit.

4.1.2 Signal Operation, Optional Configurations (Refer to figure 3.)

4.1.2.1 ISB

An optional card, 450-kHz independent sideband (ISB) if module A3, is available for ISB operation. With this card inserted and ISB mode selected, USB and LSB signals are simultaneously received and processed by the 651S-1.

Any signals passing through the LSB mechanical filter are switched by the FET filter output gates to ISB if module A3. Signals passing through the USB mechanical filter are routed through the regular if amplifier module, as in normal operation.

The ISB AGC amplifier develops an rf AGC voltage that is applied, along with another rf AGC voltage developed by the normal if/rf AGC detector, to the 109.35-MHz mixer and to the 10.35-MHz if amplifier. These two rf AGC signals represent the relative strengths of the USB and LSB signals. The rf AGC produced by the stronger signal predominates and automatically adjusts the receiver circuits for both USB and LSB reception. The ISB card provides the audio output for LSB signals. The USB audio signals are provided by the standard receiver circuits (refer to paragraph 4.1.1 for normal operation).

4.1.2.2 VLF

Two subassemblies are replaced to obtain vlf coverage: rf module A6 and synthesizer divider card A10. Table 1 lists these unique cards.

The rf module for vlf has an up-converter and filter circuit that mixes 9.9 MHz with the incoming vlf signal to produce 9.912 to 10.4599 MHz. This is then applied to the main 109.35-MHz mixer. All signals below 560 kHz will be processed by the up-converter.

The synthesizer divider card for vlf operation has vlf-enable and combinational logic circuits that cause injection frequencies 9.9 MHz above the incoming signals to be produced for signals below 560 kHz.

4.1.2.3 Automatic Frequency Scan Operation

An optional card, auto scan control card A9, is available for automatic frequency scan operation. With this card inserted, two jumper straps removed from the 651S-1 chassis sideboard (refer to installation section), and the receiver placed in the REMOTE mode, frequency scan coverage up to 100 kHz from an initial receiver frequency is provided. Scanning of the receiver frequency is conducted upward (higher in frequency) from the initial starting point. When the upper limit is reached, the receiver automatically returns (scans down) to the lower limit and repeats an upward scan.

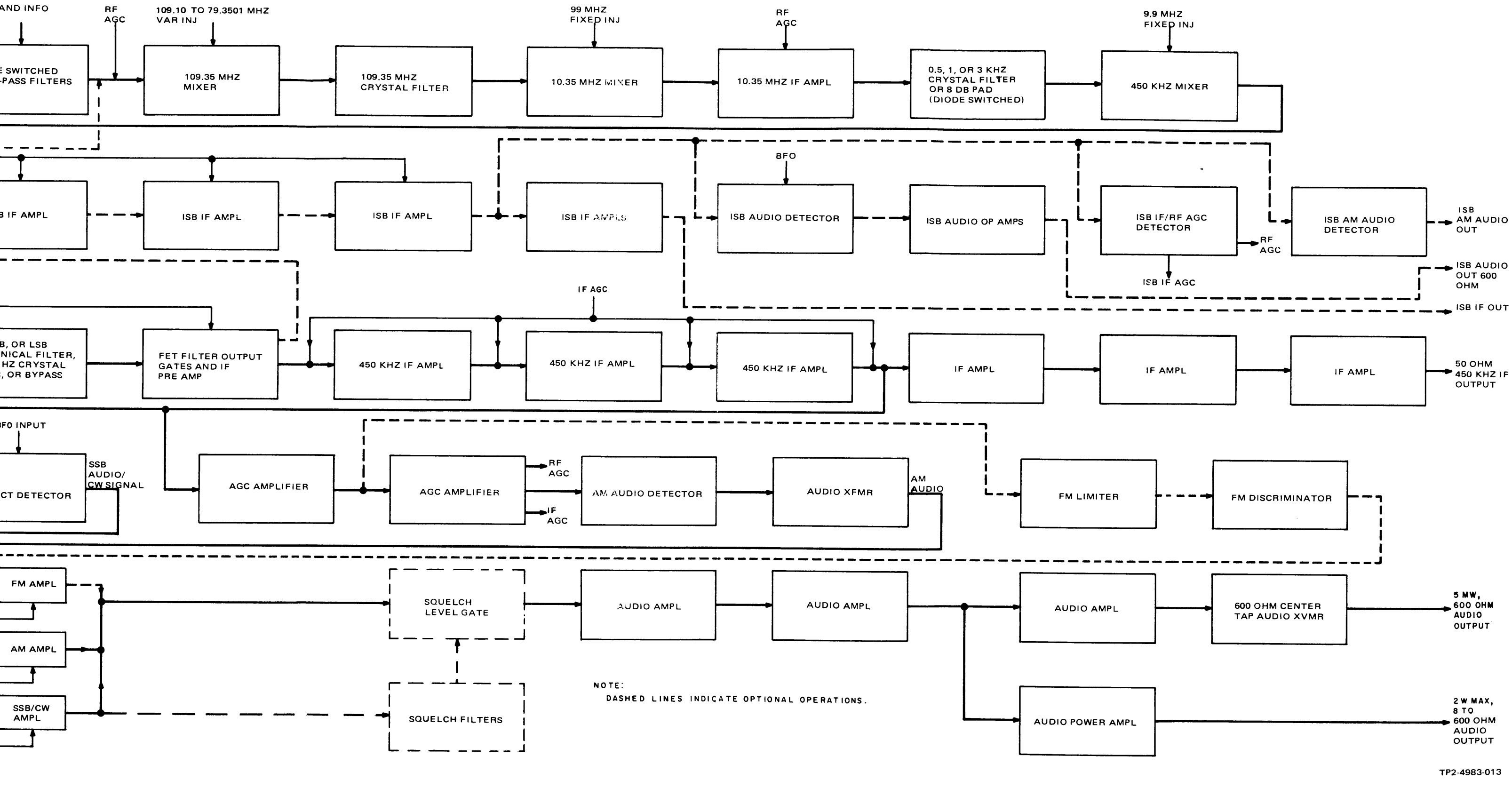
The frequency scanning steps will be in 100-Hz increments, compatible with the frequency synthesizer circuits in the receiver.

The frequency scan limits (range) are programmable internally (on-card strapping) in 100-Hz increments or externally in 1-kHz increments by using auto scan control panel, Collins part number 620-9030-001, interfaced through connector J62 at the rear of the receiver.

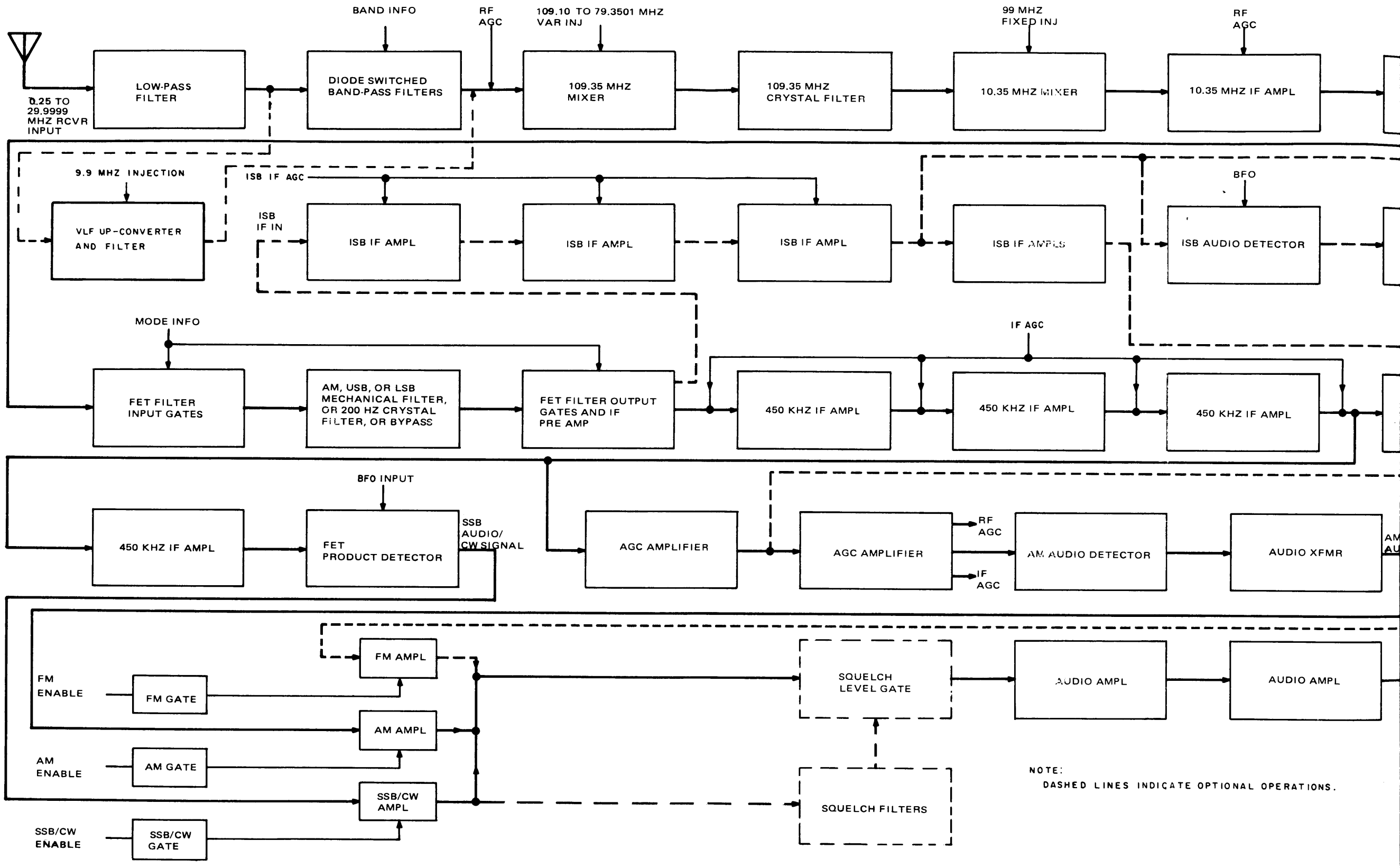
The dwell time (period in which the receiver remains on a discrete frequency) is programmable internally (on card strapping) in 100-millisecond increments from 100 to 600 miliseconds, or externally in 100-millisecond increments from 200 to 600 milliseconds using the auto scan control panel.

Frequency scan time (scan-up or scan-down) depends upon the frequency scan range and dwell time programmed. Scan-up shall not exceed 10 minutes and scan-down shall not exceed 5 seconds.

For card installation and strapping information, refer to the installation section.



Signal Operation, Functional Diagram Control
Figure 3


0.25 TO 29.9999 MHZ RCVR INPUT
LOW-PASS FILTER
BAND INFO
RF AGC
DIODE SWITCHED BAND-PASS FILTERS
109.10 TO 79.3501 MHZ VAR INJ
109.35 MHZ MIXER
109.35 MHZ CRYSTAL FILTER
99 MHZ FIXED INJ
10.35 MHZ MIXER
RF AGC
10.35 MHZ IF AMPL
9.9 MHZ INJECTION
VLF UP-CONVERTER AND FILTER
ISB IF AGC
ISB IF IN
ISB IF AMPL
ISB IF AMPL
ISB IF AMPL
ISB IF AMPLS
BFO
ISB AUDIO DETECTOR
MODE INFO
FET FILTER INPUT GATES
AM, USB, OR LSB MECHANICAL FILTER, OR 200 HZ CRYSTAL FILTER, OR BYPASS
FET FILTER OUTPUT GATES AND IF PRE AMP
IF AGC
450 KHZ IF AMPL
450 KHZ IF AMPL
450 KHZ IF AMPL
BFO INPUT
450 KHZ IF AMPL
FET PRODUCT DETECTOR
SSB AUDIO/ CW SIGNAL
AGC AMPLIFIER
AGC AMPLIFIER
RF AGC
IF AGC
AM AUDIO DETECTOR
AUDIO XFMR
FM AMPL
FM ENABLE
FM GATE
AM AMPL
AM ENABLE
AM GATE
SSB/CW AMPL
SSB/CW ENABLE
SSB/CW GATE
SQUELCH LEVEL GATE
SQUELCH FILTERS
AUDIO AMPL
AUDIO AMPL
NOTE:
DASHED LINES INDICATE OPTIONAL OPERATIONS.

4.1.3 Control Circuits, Local Operation (Refer to figure 4.)

In local operation, frequency selection, mode selection, and gain control are provided by the selector switches on the front panel of the receiver. Frequency information from the variable drum switch (100-Hz steps), the 0.1-MHz step selector, and the 1-MHz step selector, is applied to up-down counter circuits on frequency control card A14. The up-down counters provide parallel bcd frequency information to decoder/driver card A7, synthesizer divider card A10, and to the bcd to 7-bar decoder/drivers on card A14.

Decoder/driver card A7 uses the bcd frequency information from A14 to develop frequency band information that is routed to rf card A6. This band information is used by A6 to enable the proper bandpass filter on card A6.

The bcd to 7-bar decoder/drivers on card A14 decode the frequency information from the up-down counters and use this decoded frequency data to control the 7-bar numeric readout tubes on the front panel of the receiver.

The synthesizer circuits (made up of synthesizer divider card A10, synthesizer reference card A11, synthesizer mixer card A12, and synthesizer vco card A13) use the bcd frequency information from card A14 to develop the variable injection frequency that is applied to rf card A6. The synthesizer circuits also apply a fixed injection frequency to rf card A6, an if injection signal to if filter card A5, and the fixed bfo signal to if amplifier card A4.

The mode and gain information from the front-panel controls is applied to interconnect card A8. Card A8 routes this information to the applicable if and af cards.

4.1.4 Control Circuits, Remote Operation (Refer to figure 4.)

In remote operation, decoder/driver card A7, the bcd to 7-bar decoder/driver circuits on frequency control card A14, and the synthesizer circuits perform the same functions as in local operation. Interconnect card A8, however, is replaced by optional DCFE card A8, and optional DCU card A9 is added so the receiver can be controlled by an external serial digital control device. Optional DCFE card A8 and TCU card A9 are required so the receiver can be controlled by a 514S-1 Remote Control Unit.

DCU card A9 receives properly addressed biphase modulated sine-wave control data from the external digital control device. This control information appears on the control bus to the DCU, is converted by the DCU to digital control data, and is routed by the DCU to optional DCFE card A8. DCFE card A8 develops bcd frequency information and distributes this data to decoder/driver card A7, to the bcd to 7-bar decoder/drivers on card A14, and to the synthesizer circuits. The frequency information is then processed as in local operation (refer to paragraph 4.1.3).

Mode and gain control data (except audio gain) also appear on the control bus and are routed through DCU card A9 to DCFE card A8. The DCFE then sends this control data to the af and if cards as necessary to obtain the desired mode or gain level. Audio gain is controlled manually, as in local operation.

Monitor data is sent from the rest of the receiver circuits to DCFE card A8 in the form of digital monitor data. The DCFE routes this monitor data to DCU card A9 where it is converted to biphase modulated sine-wave data and sent to the external control device. This monitor data informs the control device that the receiver responded properly to the control information. The monitor data also indicates fault in the receiver circuits.

TCU card A9 receives properly addressed teletypewriter-coded control data from a 514S-1 Remote Control Unit. The control data is decoded and converted by the TCU to digital control data, and is routed to the optional DCFE card A8. The DCFE operates in the same manner as previously described, with the DCU. The TCU receives monitor data from the DCFE, encodes it into teletypewriter code, and transmits it to the 514S-1.

4.1.5 Frequency Synthesizer Circuits, Operation (Refer to figure 5.)

The 651S-1/1A frequency generating circuits provide all the injection frequencies required to select any 1 of 297,500 channels over the 0.25- to 29.9999-MHz tuning range in 100-Hz intervals. The outputs are selected and controlled by the operating frequency selected.

The synthesizer circuits are divided into two functional groups, the reference group and the frequency stabilizer group. The reference group consists of the 9.9-MHz frequency standard and the reference multipliers/dividers and produces the fixed injection signals. The frequency stabilizer group consists of phase-lock loops 1 and 2 and produces the variable rf injection signal.

The reference group generates all the reference signals required by the synthesizer circuits themselves, as well as the 450-kHz fixed bfo and 9.9-MHz if injection signals and the 99-MHz rf injection signals. The outputs from the reference group are all derived from the 9.9-MHz frequency standard. The 9.9-MHz standard signal is applied to the multipliers and dividers that provide the proper multiplication and division ratios to produce the required outputs.

The 9.9-MHz standard signal is multiplied by 10 to produce the 99-MHz injection output and divided by 22 to produce the 450-kHz injection signal. The standard signal is divided by 990 to produce the 10-kHz reference signal for phase-lock loop 2 and is divided by 1000 to produce the 9.9-kHz reference signal for phase-lock loop 1. All of the outputs from the reference group are coherent (in fixed phase relationship) with the 9.9-MHz standard signal.

The frequency group generates any one of 297.500 discrete injection frequencies at 100-Hz intervals from 79.3501 to 109.100 MHz. The 297.500 injection signals correspond to the 297.500 operating channels over the 0.25- to 29.9999-MHz tuning range of the receiver. These injection signals are selected by the bcd frequency codes applied to the two phase-lock loops by frequency control card A14 (or by optional DCFE card A8 in remote control).

The applied bcd codes control the division ratio of each loop. Operating channel frequencies and the corresponding bcd frequency codes, loop division ratios, and loop frequencies are summarized in table 4.

The first column in table 4 indicates the channel and the next six columns show the bcd frequency codes for each digit of the channel frequency. The last four columns show the corresponding division ratios and output frequencies of the two phase-lock loops. The channel frequency is changed in 100-Hz or 1-kHz steps by simultaneously changing the division ratios (N_1 and N_2) of the two phase-lock loops.

For 100-Hz steps, N_1 and N_2 are changed by a factor of 1, and for 1-kHz steps, by a factor of 10. This relationship is shown for the 2.0000- to 2.0090-MHz frequency range in the table. For 10-kHz, 100-kHz, 1-MHz, or 10-MHz steps, only N_2 is changed by 1, 10, 100, or 1000 while N_1 remains constant.

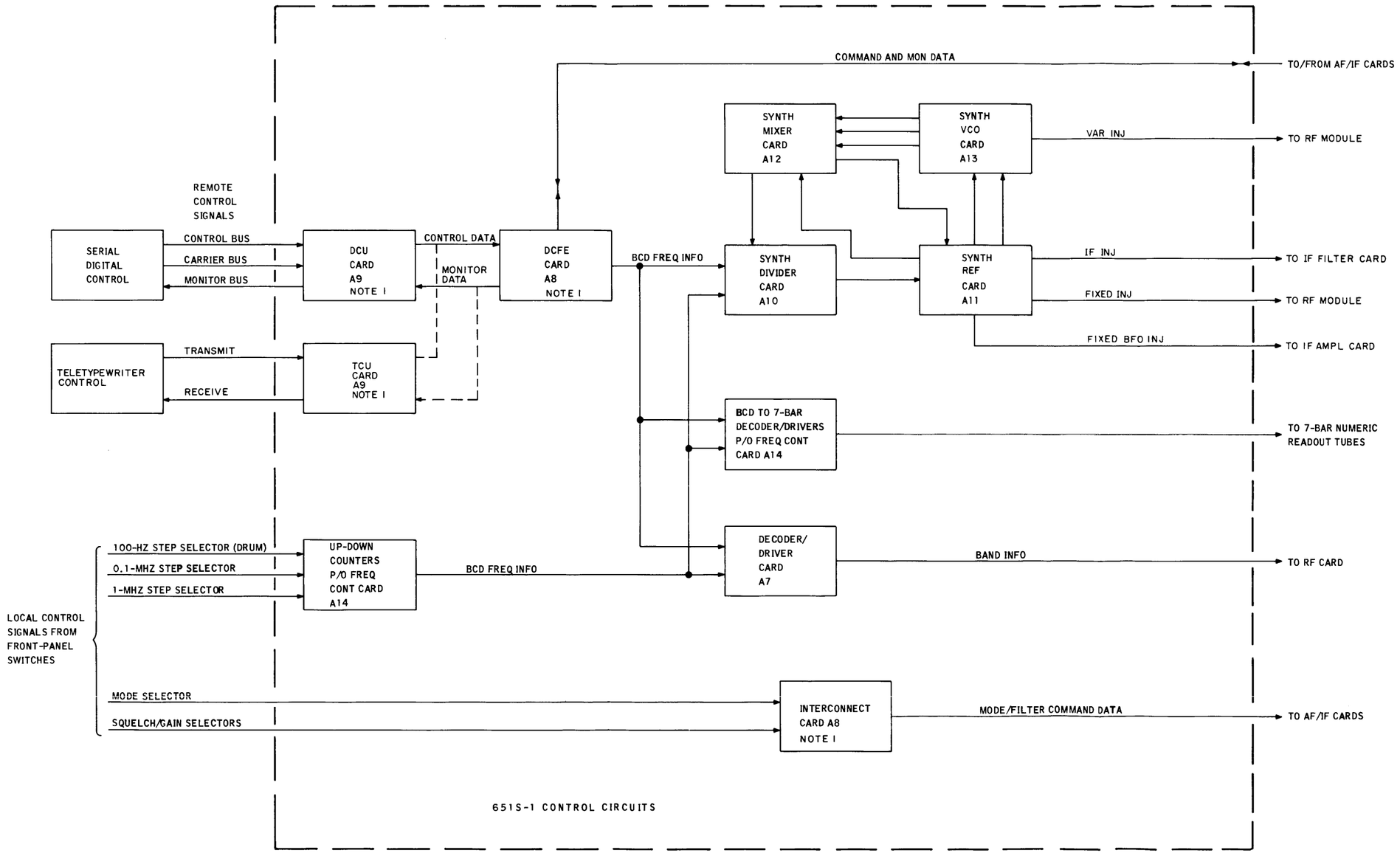
When the two least significant digits of the channel frequency reach 99 and then advance to 100, division ratio N_1 is reset to 1400 and N_2 is reset to the division ratio required for the selected channel frequency. This relationship is shown for the 2.0099-MHz channel in the table.

The variable injection output frequency (f_0) may be expressed as a function of loop frequencies and division ratios in the following equation:

$$f_0 \text{ (MHz)} = 99 + N_1 (9.9 \times 10^{-3}) - N_2 (10 \times 10^{-3})$$

The relationship of the variable injection to the corresponding channel frequency is established as the difference between the 109.3500-MHz signal developed in the associated receiver circuits and the variable injection frequency. For example, if the variable injection frequency is 107.3400 MHz, the corresponding channel is 2.0100 MHz. This relationship may be verified by referring to table 4.

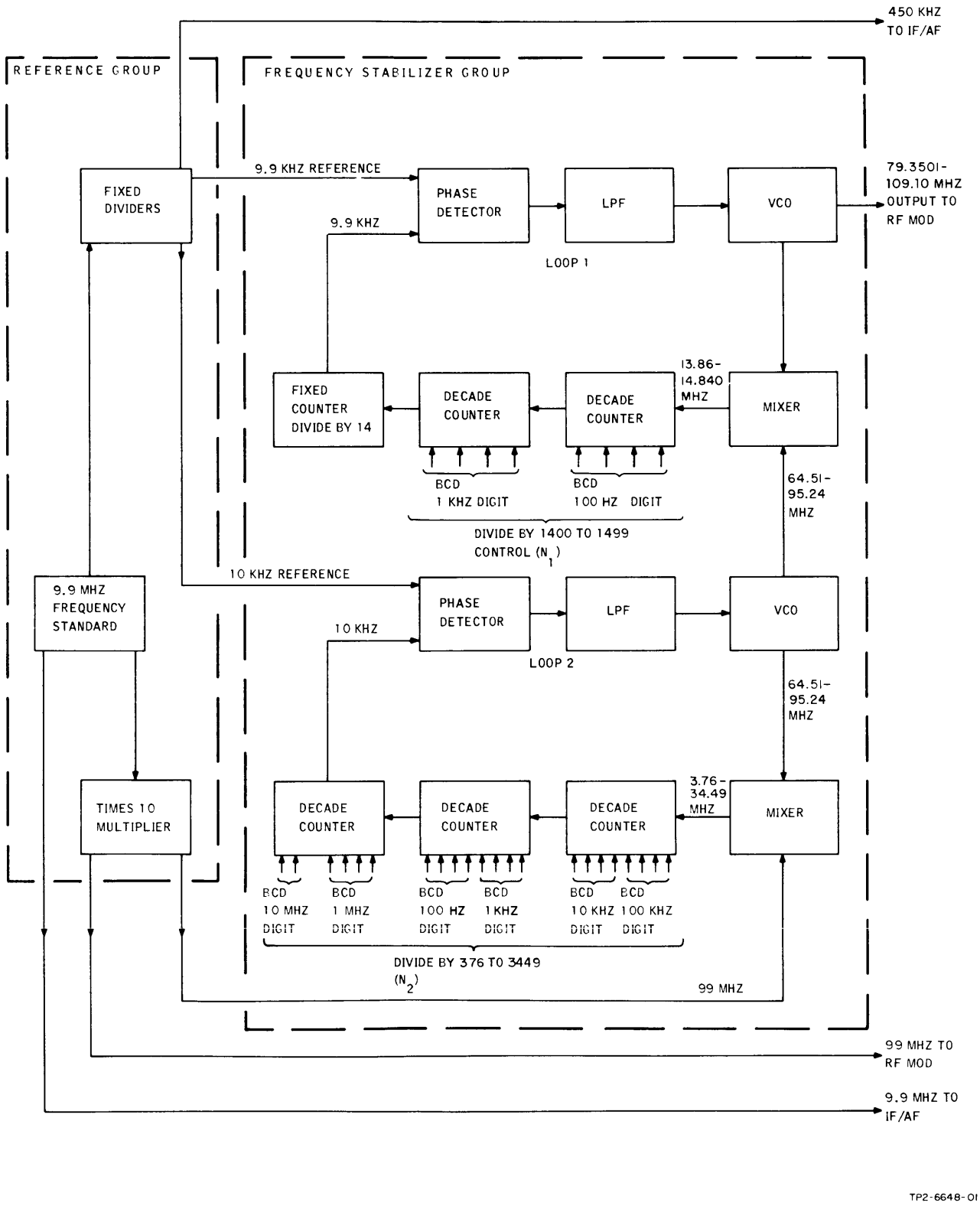
If the vlf option is installed, the synthesizer divider card (CPN 793-9334-006) for vlf replaces the normal divider card. No new mixing injection signals are generated; however, logic circuits are included that control the frequency of the mixing signals when vlf is enabled. These logic circuits command the variable injection synthesizers to produce injection frequencies for signals that are actually 9.9 MHz higher than the actual incoming signal. This is because 9.9 MHz fixed injection is added to all incoming signals below 560 kHz. For example, if 12 kHz is the incoming frequency, the synthesizer is directed to act as if 9.912 MHz were received, and so on up to 560 kHz.



NOTE:
1. IN REMOTE CONTROL OPERATION, DCFE CARD A8 REPLACES INTERCONNECT CARD A8 AND DCU OR TCU CARD A9 IS INSTALLED.
IN LOCAL CONTROL OPERATION, INTERCONNECT CARD A8 REPLACES DCFE CARD A8 AND DCU OR TCU CARD IS REMOVED.

TP2-6548-014

Control Circuits, Functional Diagram
Figure 4



Frequency Synthesizer Circuit, Functional Diagram
Figure 5

Table 4. Stabilizer Frequency Chart.

CHANNEL (MHz)	BCD FREQUENCY CODES						PHASE-LOCK LOOP 2		PHASE-LOCK LOOP 1	
	10-MHz DIGIT	1-MHz DIGIT	100-kHz DIGIT	10-kHz DIGIT	1-kHz DIGIT	100-Hz DIGIT	DIVISION RATIO (N_2)	OUTPUT FREQ (MHz)	DIVISION RATIO (N_1)	OUTPUT FREQ (f_o)(MHz)
00.2500	00	0000	0010	0101	0000	0000	376	95.24	1400	109.1000
00.4000	00	0000	0100	0000	0000	0000	391	95.09	1400	108.9500
00.5000	00	0000	0101	0000	0000	0000	401	94.99	1400	108.8500
00.6000	00	0000	0110	0000	0000	0000	411	94.89	1400	108.7500
00.7000	00	0000	0111	0000	0000	0000	421	94.79	1400	108.6500
00.8000	00	0000	1000	0000	0000	0000	431	94.69	1400	108.5500
00.9000	00	0000	1001	0000	0000	0000	441	94.59	1400	108.4500
01.0000	00	0001	0000	0000	0000	0000	451	94.49	1400	108.3500
02.0000	00	0010	0000	0000	0000	0000	551	93.49	1400	107.3500
02.0001	00	0010	0000	0000	0000	0001	552	93.48	1401	107.3499
02.0002	00	0010	0000	0000	0000	0010	553	93.47	1402	107.3498
02.0003	00	0010	0000	0000	0000	0011	554	93.46	1403	107.3497
02.0004	00	0010	0000	0000	0000	0100	555	93.45	1404	107.3496
02.0005	00	0010	0000	0000	0000	0101	556	93.44	1405	107.3495
02.0006	00	0010	0000	0000	0000	0110	557	93.43	1406	107.3494
02.0007	00	0010	0000	0000	0000	0111	558	93.42	1407	107.3493
02.0008	00	0010	0000	0000	0000	1000	559	93.41	1408	107.3492
02.0009	00	0010	0000	0000	0000	1001	560	93.40	1409	107.3491
02.0010	00	0010	0000	0000	0001	0000	561	93.39	1410	107.3490
02.0020	00	0010	0000	0000	0010	0000	571	93.29	1420	107.3480
02.0030	00	0010	0000	0000	0011	0000	581	93.19	1430	107.3470
02.0040	00	0010	0000	0000	0100	0000	591	93.09	1440	107.3460
02.0050	00	0010	0000	0000	0101	0000	601	92.99	1450	107.3450
02.0060	00	0010	0000	0000	0110	0000	611	92.89	1460	107.3440
02.0070	00	0010	0000	0000	0111	0000	621	92.79	1470	107.3430
02.0080	00	0010	0000	0000	1000	0000	631	92.69	1480	107.3420
02.0090	00	0010	0000	0000	1001	0000	641	92.59	1490	107.3410
02.0099	00	0010	0000	0000	1001	1001	650	92.50	1499	107.3401
02.0100	00	0010	0000	0001	0000	0000	552	93.48	1400	107.3400
02.0200	00	0010	0000	0010	0000	0000	553	93.47	1400	107.3300
02.0300	00	0010	0000	0011	0000	0000	554	93.46	1400	107.3200
02.0400	00	0010	0000	0100	0000	0000	555	93.45	1400	107.3100
02.0500	00	0010	0000	0101	0000	0000	556	93.44	1400	107.3000
02.0600	00	0010	0000	0110	0000	0000	557	93.43	1400	107.2900
02.0700	00	0010	0000	0111	0000	0000	558	93.42	1400	107.2800
02.0800	00	0010	0000	1000	0000	0000	559	93.41	1400	107.2700
02.0900	00	0010	0000	1001	0000	0000	560	93.40	1400	107.2600
02.1000	00	0010	0001	0000	0000	0000	561	93.39	1400	107.2500
02.2000	00	0010	0010	0000	0000	0000	571	93.29	1400	107.1500
02.3000	00	0010	0011	0000	0000	0000	581	93.19	1400	107.0500
02.4000	00	0010	0100	0000	0000	0000	591	93.09	1400	106.9500
02.5000	00	0010	0101	0000	0000	0000	601	92.99	1400	106.8500
02.6000	00	0010	0110	0000	0000	0000	611	92.89	1400	106.7500
02.7000	00	0010	0111	0000	0000	0000	621	92.79	1400	106.6500
02.8000	00	0010	1000	0000	0000	0000	631	92.69	1400	106.5500
02.9000	00	0010	1001	0000	0000	0000	641	92.59	1400	106.4500
03.0000	00	0011	0000	0000	0000	0000	651	92.49	1400	106.3500
04.0000	00	0100	0000	0000	0000	0000	751	91.49	1400	105.3500
05.0000	00	0101	0000	0000	0000	0000	851	90.49	1400	104.3500
06.0000	00	0110	0000	0000	0000	0000	951	89.49	1400	103.3500
07.0000	00	0111	0000	0000	0000	0000	1051	88.49	1400	102.3500
08.0000	00	1000	0000	0000	0000	0000	1151	87.49	1400	101.3500
09.0000	00	1001	0000	0000	0000	0000	1251	86.49	1400	100.3500
10.0000	01	0000	0000	0000	0000	0000	1351	85.49	1400	91.3500
20.0000	10	0000	0000	0000	0000	0000	2351	75.49	1400	89.3500
29.9999	10	1001	1001	1001	1001	1001	3449	64.51	1499	79.3501

4.2 Subassembly Operation

4.2.1 RF Module A6

4.2.1.1 Standard Version (CPN 790-1048-008/-020)

Refer to the appropriate schematic in the diagrams section. The received rf signal enters the 651S-1/1A at rear-panel coaxial connector J61 and is applied directly to low-pass filter FL201. The rf input is then applied to connector P5 on rf module A6 and is routed through low-pass filter FL501 on A6 to 1 of the diode-switched bandpass filters on A6. Functionally, the -008 and -020 part numbers are identical. The -008 has 10 diode-switched bandpass filters and the -020 has only 3 diode-switched bandpass filters. The -020 part number is the current production model.

The proper filter is selected by band information from band decoder card A7 (refer to table 5 for the outputs from card A7). For example, if an operating frequency within the 3- to 3.9999-MHz band is selected, +5 V appears at A6P8-7 and -15 V is applied to all other band inputs. The +5 V at A6P8-7 forward biases diode CR113, allowing the rf input signal to pass through the 3- to 3.9999-MHz bandpass filter. The -15 V on the other band inputs disables the remaining bandpass filters.

The received rf input passes through the selected bandpass filter and is transformer coupled to multiple FET mixer U1 where a variable injection signal from 79.3501 to 109.10 MHz is added to produce a 109.35-MHz signal. (For example, if the operating frequency is 2.901 MHz, the injection signal supplied by the synthesizer is 106.449 MHz.) The injection frequencies are applied through broadband injection amplifier Q5. The injection amplifier uses feedback control to eliminate gain and sensitivity changes due to varying injection voltages across the frequency spectrum. Resonant transformer T2 matches the output of mixer U1 to 109.35-MHz crystal filter FL1. This crystal filter has a 16-kHz bandwidth.

After passing through crystal filter FL1, the 109.35-MHz signal is applied to an FET balanced mixer (Q1 and Q2) where 99 MHz is injected and the 109.35-MHz signal is converted to 10.35 MHz. The injection signal is supplied by the synthesizer cards and is amplified by transistor A6Q6. The mixed signal is applied through resonant transformer T4 to if amplifier A3. AGC is applied at this point and the final 10.35-MHz signal is sent to if filter card A5.

4.2.1.2 VLF Version (CPN 790-1048-010/-021)

Refer to the appropriate schematic in the diagrams section. The received signal is applied to A6P5 and then to K701. If the incoming signal is above 560 kHz, K701 is deenergized and the rf is applied to the filter assemblies and everything is as in the CPN 790-1048-008/-020 versions of A6.

If the incoming signal is below 560 kHz, K701 is energized and the rf is applied to the vlf up-converter (sheet 2 of the schematic). The signal is filtered by FL601 and applied to balanced FET mixer U601 and mixed with 9.9-MHz. The output range of frequencies from this mixer is 9.912 MHz to 10.4599 MHz.

This range of outputs is then applied to multiple FET mixer U1 and the signal is processed as in the CPN 790-1048-008/-020 versions of A6.

4.2.2 IF Filter Card A5

Refer to the schematic in the diagrams section. The if filter card is subcard A5A1 only for standard bandwidths; however, optional filter A5A1FL1 is added and/or subcard A5A2 is sandwiched with A5A1 to provide optional bandwidths. Refer to table 1 and paragraph 5 for receiver configuration/subcard part number information. Also refer to table 1 in the optional section for the operational bandwidths available with respect to the mode switch positions required to enable the proper filter.

The 50-ohm, 10.35-MHz if signal from rf module A6 comes in at A5P5 and is switched through one of three 10.35-MHz crystal filters, or the filters are bypassed. The signal is applied through A5A1FL1 (optional bandwidth) if BANDWIDTH .5, CW, or 2 (as appropriate) is selected, through A5A2FL2 (optional bandwidth) if BANDWIDTH 1, 4, WSRT, or WBTY (as appropriate) is selected, or through A5A2FL3 (optional bandwidth) if BANDWIDTH 3 is selected. For all other modes, these three filters are bypassed and the 10.35-MHz signal is applied through an 8-dB pad (made up of A5A1R2, R3, and R4). When the operating bandwidth is selected, transistor gates switch

the appropriate filter (or the pad) into the signal circuit. This switching differs when certain subcards are used; refer to paragraph 5 for differences. The resultant 10.35-MHz signal is then converted to 450 kHz by balanced FET mixer Q9 and Q10. The 9.9-MHz mixing injection signal is supplied by the synthesizer cards and is controlled by buffer amplifier A11.

The 450-kHz signal is then applied through tuned transformer T2 to another group of filters; either a 450-kHz AM, USB, or LSB mechanical filter; an optional-bandwidth crystal filter A5A2FL4 for BANDWIDTH .2, 1, or NSRT (as appropriate) or an 8-dB pad (A5A1C50, R64, and C51) for 16-kHz bandwidths of AM and FM. If operating in the optional ISB mode, the LSB mechanical filter passes the ISB signal. The inputs and outputs of the mechanical filters are tuned by fixed capacitors. The appropriate filter is again selected by enabling the correct transistor gate. The FET's at the filter outputs serve as low-noise if preamplifiers and the final 450-kHz signal is routed to if amplifier card A4.

4.2.3 IF Amplifier Card A4

Refer to the appropriate schematic in the diagrams section. If amplifier card CPN 778-2951-001 is the standard if amplifier card with FM. The -003 and -004 part numbers are functionally identical to the -001 except the -003 provides for a special fast reaction external rf gain control and the -004 has no FM detector. The -004 part number is the current production model. Refer to table 1 and paragraph 5 for receiver configuration and difference data.

The 50-ohm, 450-kHz if signal from if filter card A5 passes through 1:5 step-up transformer T1 and three transistor amplifiers Q1, Q2, and Q3 on if amplifier card A4. Shunt diode AGC is applied to each of the three transistor amplifiers. The 450-kHz signal then branches four ways: one for if output, one for AM/AGC detection, one for SSB/CW detection, and one for NBFM detection.

The signal for if output passes through two additional transistor amplifiers, Q6 and Q7, to emitter follower Q8. The output from Q8 is routed through 3:1 step-down transformer T2 to output connector P3 on the rear of the chassis.

The signal for SSB/CW detection passes through transistor amplifier Q4 and 1:4 voltage step-up transformer T3 to dual-gate FET product detector Q12. The bfo signal is injected at this point to derive the SSB/CW intelligence. The SSB/CW signal is then routed to audio amplifier card A2.

The signal for AM/AGC detection is applied to AGC amplifier transistors Q10 and Q11. The output from Q11 is transformed and then demodulated by emitter follower Q13. This signal is the AM audio signal and is sent to audio card A2. The signal for FM is taken from the high-level output of AGC amplifier Q10 and is applied to buffer transistor Q12. The FM signal is then applied to FM limiter/detector U2 and the audio output is sent separately to audio card A2.

The output from AGC amplifier transistors Q10 and Q11 is also applied to an adjustable AGC time constant circuit. The AGC release time is controlled at this point by an AGC release time control input from DCFE card A8 or the AGC FAST-SLOW front panel switch. The AGC line is highly filtered to protect against in-band intermodulation. The dc level of AGC is amplified by operational amplifier U1 and complementary emitter follower Q17 then drives the AGC bus. AGC can also be completely disabled by the front panel switch (center position), or by DCFE card A8.

4.2.4 ISB Amplifier Card A3 (Optional)

Refer to the schematic in the diagrams section. In the ISB mode of operation, the signal passing through the LSB mechanical filter on if filter card A5 is applied to ISB if input connector P1 on ISB amplifier card A3. This signal is processed the same as the if signal on if amplifier card A4 (see paragraph 4.4 for circuit operation). ISB if and AM audio signals are developed and appear as outputs from card A3. The SSB af signal developed by dual-gate FET product detector Q12, however, is not sent by card A3 to audio card A2. This signal is routed through operational amplifiers U2A, U2B, and U3 and transformer T5. The output from T5 is a separate 600-ohm ISB audio signal.

4.2.5 Audio Card A2

Refer to the appropriate schematic in the diagrams section.

All audio signals are fed to audio card A2 for final amplification. The three types of signal (AM, FM, and SSB/CW) are applied to gated amplifiers. The appropriate type signal is passed and amplified when the front-panel mode selector is in the proper position to enable the selective gate. The selected audio signal is applied to linear operational amplifiers U3A and U3B through blanking gate transistor Q15. Two types of audio output are developed, 600-ohm line output for external power amplification and 8- to 600-ohm loudspeaker/headset output.

The 600-ohm output is developed through operational amplifier U4 and 600-ohm center-tap transformer T1. The loudspeaker/headset output goes through the front-panel volume control to a power amplifier mounted on the rear chassis.

Fixed bfo signals from synthesizer reference card A11 are routed through card A2 directly to if amplifier card A4. In local control, front panel control switch S105 (BFO switch) selects either a fixed (450 kHz) or variable bfo (vbfo) frequency. When BFO switch S105 is in the FIXED position, logic 0's are applied by interconnect card A8 to interpolate vbfo enable pin A2P1-43 and to CW vbfo enable pin A2P1-41. These logic 0's turn off transistors A2Q3 and A2Q4, disabling crystal oscillators A2Y1 and A2Y2. The fixed 450-kHz bfo input frequency, phase-locked to the 9.9-MHz reference frequency, is then applied to 450-kHz bfo input connector A2P3 by synthesizer reference card A11. The bfo frequency is then diode switched by A2CR7 and A2CR8 to bfo output connector A2P2.

Circuit card A2 also generates the vbfo signals and routes these signals to if amplifier card A4. The vbfo circuits produce bfo variations in SSB of ±60 Hz in 10-Hz steps and in CW of ±900 Hz.

When BFO switch S105 is in the VAR position and USB or LSB mode is selected by front panel mode switch S102, a logic 1 is applied to interpolate vbfo enable pin A2P1-43 by interconnect card A8. This logic 1 turns on transistor A2Q3, enabling crystal oscillators A2Y1 and A2Y2. A 3- to 12-Vdc vbfo signal from 13-position front panel VBFO control switch S112 is applied to vbfo frequency input pin A2P1-45. This variable voltage is divided by resistor networks on card A2 and is applied to Varicaps A2CR1 and A2CR3. These Varicaps then pull the crystal oscillators, resulting in variable frequency outputs from the crystal oscillators. These outputs are applied to and mixed by mixer A2U1 to produce the bfo variation in SSB of ±60 Hz. On audio card A2 (CPN 778-2948-002) and the older versions of -003 (refer to paragraph 5 for difference data), this signal is amplified by operational amplifier A2U2 and routed through low-pass filter circuit (A2T1, -T2, -C42, -C43, and -C44) to BFO output connector A2P2. The low-pass filter shapes the bfo output sine-wave signal and prevents the oscillator frequencies (4.00 and 4.45 MHz) from being applied to the bfo output line. On audio card A2 (CPN 778-2948-004) and the current production model of -003, -005, the bfo variation signal is amplified by transistor amplifier Q6 and routed to bfo output connector A2P2.

When BFO switch S105 is in the VAR position and CW mode is selected by front panel mode switch S102, a logic 1 is applied to CW vbfo enable pin A2P1-41 by interconnect card A8. This logic 1 turns on transistor A2Q3, enabling crystal oscillators A2Y1 and A2Y2 and turns on transistor A2Q4, energizing relays A2K1 and A2K2. The 13-step vbfo control signal from front panel switch S112 is applied to vbfo frequency input pin A2P1-45 as in USB or LSB mode. However, in CW mode, relays A2K1 and A2K2 switch different resistors into the divider circuits and different fixed capacitors into the oscillator circuits. The crystal oscillators then produce different frequencies when pulled by Varicaps A2CR1 and A2CR3. The outputs from the oscillators are applied to and mixed by mixer A2U1 as in SSB. The output from the mixer in CW mode, however, is a bfo variation of ±900 Hz. The signal is then amplified and routed to bfo output connector A2P2 as in SSB.

In remote control, the operation of the bfo and vbfo circuits on audio card A2 is the same as in local control. The interpolated vbfo enable, CW vbfo enable, and vbfo frequency control inputs to card A2, however, are generated by control word commands from the associated processor unit. Refer to the DCFE theory of operation for control word content and format.

The optional squelch circuit on audio card A2 (CPN 778-2948-002/-004) consists of two integrated active filters (high pass U1A and low pass U1B), two rectifier transistors Q1 and Q2, and differential amplifier U2 that compares the rectified levels from Q1 and Q2.

The output from U2 controls gating transistors that turn on squelch gate Q15. Squelch gate Q15 is also controlled by squelch on/off and audio blanking signals. The squelch on/off control signal is sent from the front panel SQUELCH control or DCFE card A8. The audio blanking signal is developed when manual tuning is initiated and blanks out the audio signal until a new operating frequency is selected by the manual tuning control.

The squelch level input is developed by the front panel SQUELCH control. Received speech signals have a greater level of low-frequency components than high-frequency components. The squelch level signals are therefore applied to the output of low-pass filter U1B.

4.2.6 Synthesizer Divider Card A10

4.2.6.1 Standard Version (CPN 793-9334-002)

Refer to the schematic in the diagrams section. The circuits on synthesizer divider card A10 form a programmable frequency divider with variable division ratios ranging from 391 through 3449. The division ratio for a particular operating frequency is determined by the bcd frequency control information from card A8 or card A14 plus fixed number 351. The variable divider contains two programmable decade counters and one programmable digit counter. The first decade counter consists of U21, U11, U13, U14, U24, and U34; the second decade counter consists of U41, U23, U54, U22, and U73; and the digit counter consists of U71, U61, and U72.

A 3- through 35-MHz input is applied to the first programmable decade counter. Frequency control information is applied to converter circuits within the variable counter circuits in parallel binary bcd form. The 10-kHz output is applied to the phase-locked loop phase detector on synthesizer reference card A11.

Altering the count of the first decade counter by 1 during each count cycle will change the net division ratio of the complete circuit by 1. Therefore the first decade is controlled by the 100-Hz and 10-kHz frequency control information in addition to a fixed number 1 (the 1 of the fixed number 351). Similarly, altering the count of the second decade by 1 during each count cycle changes the net division ratio of the complete circuit by 10. The second decade then is controlled by the 1-kHz and 100-kHz frequency control information in addition to a fixed number 5 (the 5 of the fixed number 351). Altering the count of the programmable digit counter by 1 during each count changes the overall net division ratio by 100. This section then is controlled by the 1-MHz and 10-MHz frequency control information along with the fixed number 3 (the 3 of the fixed number 351). The net division ratio of the complete variable divider circuit can be determined as shown in the following example.

	10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz
Operating frequency	0	2	0	0	9	9
Add 1-kHz and 100-Hz digits			9	9		
Add fixed number	0	3	5	1		
Total	0	6	5	0		

Determine the division ratio by adding 6, 5, and 0 as follows:

6 = 600

5 = 50

0 = 0

Division ratio = 650

The following explanation describes the general events that occur in the 10-kHz phase-lock loop when the operating frequency is changed in small steps.

Assume that the phase-lock loop is in an in-lock condition, which means that both inputs to the phase detector circuits are 10 kHz. When the operating frequency of the radio set is changed, the division ratio of the programmable divider circuits also changes and causes the output of the divider circuits to be some value other than 10 kHz. The output pulse width of the phase detector circuit on card A11 changes and applies a different error voltage level to the vco on card A13. When the error voltage is applied, the vco begins to change frequency and continues to change until the output of the divider circuit is again 10 kHz. At this point the output pulse width of the phase detector stops changing, the vco remains at that frequency, and the 10-kHz phase-lock loop is again in an in-lock condition. The phase detector controls both frequency and phase. For small frequency changes as just described, the frequency function of the detector does not operate, but for large frequency changes, the phase function is inhibited and the output of the detector locks in a high or low state. It remains in this state until the vco frequency passes through the desired value, at which time it switches back to the phase detection mode.

4.2.6.2 VLF Version (CPN 793-9334-006)

At 560 kHz and above, the vlf version of A10 functions the same as card A10 (CPN 793-9334-002). However, below 560 kHz, combinational logic circuits alter the 10-MHz, 1-MHz, and 100-kHz inputs by adding 9.9 MHz to the incoming signals. For example, if 12 kHz is the incoming control frequency, the synthesizer is directed to act as if 9.912 MHz was received. The resulting synthesizer injection frequencies are actually 9.9 MHz above the vlf selected frequencies.

4.2.7 Synthesizer Reference Card A11

Refer to the schematic in the diagrams section. Synthesizer reference card A11 provides all reference signals required by the synthesizer circuits as well as the injection signals to the if/af cards, and rf module. It contains the 9.9-MHz frequency standard, multiplier, fixed dividers, and phase detectors for both phase-locked loops 1 and 2.

Frequency standard A1 is a temperature-compensated 9.9-MHz crystal-controlled oscillator. Buffer/driver circuit U45 is used primarily for signal distribution. It also prevents loading of the frequency standard and isolates the digital circuits from the 9.9-MHz output and X10 multiplier A2.

The X10 multiplier multiplies the 9.9-MHz reference frequency by 10 to provide two fixed 99-MHz injection frequencies for use in the phase-locked loop 2 mixer (on synthesizer mixer card A12) and the rf mixers on rf module A6.

The 9.9-MHz filter (L5, C17, and C18) provides impedance matching and harmonic filtering for the 9.9-MHz injection frequency applied to if filter card A5. The 9.9-MHz frequency standard is fed through three fixed divide-by-10 decade counters (U25, U13, and U12) to provide the 9.9-kHz reference frequency to loop 1 phase detector circuit U21, U31, U41, and U42.

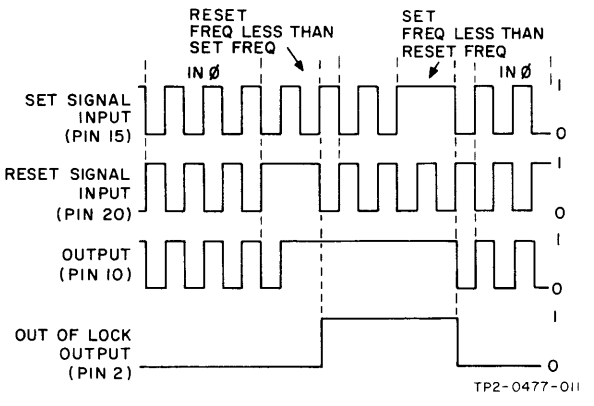
The output of divide-by-10 decade counter U25 is also applied to a divide-by-99 counter circuit to provide the 10.0-kHz reference frequency to loop 2 phase detector circuit U34, U44, U43, and U33. The divide-by-99 counter is formed by two 4-binary counters (U23 and U24) plus two logic gates U11A and U11B). U23 is connected as a divide-by-nine decade counter and the output of U23 (110 kHz) is applied to the divide-by-11 decade counter (U24). The 10-kHz output of U24 is applied to the phase detector circuit. Logic gates U11A and U11B improve the waveshape of the output pulse.

The 9.9-MHz frequency standard is also applied to a divide-by-two counter (U14B). The 4.95-MHz output of this circuit is applied to a divide-by-11 decade counter U15 to provide the 450-kHz injection signal for the if/af cards. L1 and C3 through C5 form a pi-section LC filter to provide impedance matching and harmonic filtering for the 450-kHz injection signal.

The phase detector circuits for phase-locked loops 1 and 2 are identical. They provide positive output pulses at their respective frequencies (9.9 kHz/10 kHz) to the low-pass filter drivers on synthesizer vco card A13. Since both detectors are functionally the same, only the operation of loop 1 detector circuit will be discussed.

Phase detector U21 receives two input signals: a 9.9-kHz reference or set signal (U21B), and a 9.9-kHz reset signal from phase-locked loop 1 variable dividers (U21A). The detector circuit compares the phase relationship of the set and reset input signals and generates an output pulse, the width of which is equal to the phase difference between two inputs (figure 6). If the reset input falls below 9.9 kHz, the resulting phase differential causes the error output to lock at logic 1. If the reset signal rises above 9.9 kHz, the error output locks at logic 0. The output remains at logic 1 or logic 0 until the vco passes through the desired in-lock frequency. It then starts responding again to the set and reset inputs. The phase detector circuit is totally unaffected by harmonics of the basic frequencies involved in the phase-lock loop. The error output of the detector is applied to low-pass filter driver Q3 on synthesizer vco card A13.

Out-of-lock monitor U32 output is a logic 0 when either loop 1 or loop 2 is in an in-lock condition. When either loop is in an out-of-lock condition, out-of-lock monitor output goes to logic 1 indicating to monitor circuits on DCFE card A8 that one of the phase-lock loops is not operating properly.



Frequency Phase Detector Timing Diagram
Figure 6

4.2.8 Synthesizer Mixer Card A12

Refer to the schematic in the diagrams section. Synthesizer mixer card A12 is comprised of phase-locked loops 1 and 2 mixers and the variable divider circuit used in loop 1.

The 79.3501- to 109.100-MHz signal from loop 1 vco is applied to loop 1 mixer A1 along with the 64.510- to 95.240-MHz signal from loop 2 vco. The difference frequency from A1 ranges from 13.860 to 14.840 MHz and is applied through inverter amplifier U11B to the variable frequency divider circuit.

The variable divider circuit used in loop 1 is a programmable frequency divider with variable division ratios ranging from 1400 through 1499. The division ratio for a particular operating frequency of the radio set is determined by the 100-Hz and 1-kHz frequency information from frequency control card A14 or DCFE card A8. The divide-by-100-to-199 circuit consists of two decade programmable counters: U1 through U5 and U7 form the first decade counter, and U9 the second.

The bcd frequency control information (100 Hz and 1 kHz) is applied to code converter circuits within the counter circuits that inhibit the decade counters for a number of pulses equal to the 100-Hz and 1-kHz value (digit) of the operating frequency. If the 100-Hz and 1-kHz digits are both 0, the counters are not inhibited and function as basic decade (divide by 10) counters. If the digits are both 9, the counters are both inhibited for 9 pulses prior to dividing by 10.

In the first instance, the resulting count (division ratio) is 100. In the second instance, the division ratio is 199.

The remaining counter circuit U10 is a fixed divide-by-14 binary counter circuit that, when operating in series with division ratios ranging from 100 to 199, provides an overall division ratio of 1400 to 1499. Table 5 provides the division ratios of the 9.9-kHz divider circuits for various operating frequencies. The division ratio for any operating frequency can be calculated as follows:

Operating frequency: 2.0049 MHz

Fixed division ratio:	1	4	0	0
Add 1-kHz digit:			4	
Add 100-Hz digit:				9
Total (division ratio):	1	4	4	9

The 9.9-kHz output signal is applied to the phase detector on synthesizer reference card A11.

The 64.510- to 95.24-MHz signal from loop 2 vco is applied to loop 2 mixer A2 along with the 99-MHz injection frequency from the X10 multiplier on synthesizer reference card A11. The difference frequency of A2 ranges from 3.76 to 34.490 MHz and is applied to the input of phase-locked loop 2 variable divider circuit on synthesizer divider card A10.

4.2.9 Synthesizer VCO Card A13

Refer to the schematic in the diagrams section. Synthesizer vco card A13 receives phase detector outputs from synthesizer reference card A11 and provides injection outputs to synthesizer mixer card A12 and rf module A6.

The 10-kHz input at P1 is positive pulses from the phase detector on synthesizer reference card A11. The width of the positive pulses is proportional to the phase error. When the phase error increases, the width of the positive pulses also increases. The positive pulses are amplified by driver Q2 and applied to the loop 2 low-pass filter. The low-pass filter provides a positive dc output to the vco (voltage controlled oscillator) that is proportional to the width of the square-wave input.

The loop 2 vco generates two identical 64.510- to 95.24-MHz output frequencies that are supplied to synthesizer mixer card A12. The loop 2 vco also provides positive and negative voltage outputs to the loop 1 vco. The vco contains an FET oscillator that is controlled by a varactor with the varactor controlled by the positive voltage output of the low-pass filter. As the positive voltage output of the low-pass filter increases, the frequency output of the vco increases.

The loop 1 low-pass filter and vco operate similarly to the loop 2 low-pass filter and vco. The loop 1 vco is controlled by outputs from the loop 1 low-pass filter and the loop 2 vco. The loop 1 vco supplies two identical 79.3501- to 109.100-MHz outputs, one to rf module A6 and the other to synthesizer mixer card A12.

4.2.10 Decoder/Driver Card A7

Table 5 lists the logic inputs to card A7 and A7's outputs to module A6.

4.2.10.1 Decoder/Driver A7, 778-2928-003

Refer to the schematic in the diagrams section. The decoder/driver card converts the bcd frequency information from frequency control card A14 into 10 frequency band outputs. The individual circuits that produce the 10 bands are similar; only the 16- to 23.9999-MHz enabling circuit and how the other bands are disabled are described. For this purpose, assume an input frequency of 18 MHz.

The 10-MHz-2 and 1-MHz-4, -2 and -1 input lines are logic 0, and the 10-MHz-1 and 1-MHz-8 input lines are logic 1.

The 10-MHz-2 (logic 0) input is inverted by U1D and U1E with the U1E logic 0 output applied to U6A-3 as an enabling signal and to U11C-8 and U11D-12 as a disabling signal. The U1E output is also inverted by U1F to logic 1 and applied to U6B-6 as a disabling signal and to U15B-5.

The 10 MHz-1 (logic 1) input is inverted by U1A and U1B with the U1B logic 1 output applied to U7C-11 and U11B-6 as an enabling signal and

Table 5. Decoder/Driver Input/Output Table.

		OPERATING BAND (MHz)																																					
		29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	.9	.8	.7	.6	.56	.5	.4
Bcd input to A7	20	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	10	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	4	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	2	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0
	0.8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
	0.4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	0.2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
	0.1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0
	0.08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0.04	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	0.02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Band output to A6	24-29.9999	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	16-23.9999	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	12-15.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	8-11.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	6-7.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	4-5.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
	3-3.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	2-2.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	0.56-1.9999	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
	0-0.5599	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	1

CPN 608-9087-001 and 608-9121-001 each has only 3-band output: Band 1, 0 to 0.5599 MHz; band 2, 0.56 to 1.9999 MHz, and band 3, 2 to 29.9999 MHz.

to U8A-3, U8C-11, and U8B-6 as a disabling signal. The U1B output is also inverted by U1C to logic 0 and applied to U6B-8 as a disabling signal and to U15B-6. The U15B logic 1 output is inverted by U16A and this logic 0 is applied as a disabling input to U7A-2, U7B-6, and U14B-5.

The 1 MHz-8 (logic 1) input is inverted by U3D and U3E with the U3E logic 1 output applied to U11B-5 as an enabling signal and to U11C-9 and U14B-6 as a disabling signal. The U3E output is also inverted by U3F to logic 0 and applied to U6A-1 as an enabling signal and to U15A-1.

The 1 MHz-4 (logic 0) input is inverted by U3A and U3B with the U3B logic 0 output applied to U7C-13 as an enabling signal and to U8C-13, U7A-3, U7B-7, and U11D-13 as a disabling signal. The U3B output is also inverted by U3C to logic 1 and applied to U6A-2 as an enabling signal and to U8A-1, U8B-7, and U6B-7 as a disabling signal.

The 1 MHz-2 (logic 0) input is inverted by U2A and U2B with the U2B logic 0 output applied to U7C-12 as an enabling signal and to U7A-1, U8A-2, U12A-1, and U12C-12 as a disabling signal. The U2B output is also inverted by U2C to logic 1 and applied to U7B-8 as a disabling signal and to U15A-2. The U15A logic 1 output is inverted by U16B to logic 0 and applied to U8B-8, U8C-12, and U13A-1 as a disabling input.

The 1 MHz-1 (logic 0) input is inverted by U2D and U2E with the U2E logic 0 output applied to U12A-2 as a disabling signal. The U2E output is also inverted by U2F to logic 1 and applied to U12C-13 and U13C-9 as a disabling signal.

The 18-MHz enabling decode circuit consists of U6A, U7C, and U11B. The enabling signals derived above for this circuit are two logic 0's and one logic 1 for the U6A and U7C, and two logic 1's for U11B. The two logic 1's and one logic 0 output of this circuit are applied to U6C. The U6C logic 1 output turns on Q3 and in turn Q4 turns on. This produces a logic 1 (+5 Vdc) output at P1-45 (16- to 23.9999-MHz enable).

The disabling logic (for all frequencies except 18 MHz) derived above acts to cut off the output band-driver circuits. The 24- to 29.9999-MHz band is disabled by disabling logic on U11C and U11D. A logic 1 and a logic 0 input to U11C and two logic 0 inputs to U11D produce two logic 1 outputs. Two logic 1 inputs to U11A produce a logic 0 output. This cuts off Q1 and Q2 in turn. Pin P1-62 (24 to 29.9999 MHz) then has a logic 0 (-15 Vdc) as an output to the band circuits of rf module A6. The 12- to 15.9999-MHz and the 8- to 11.9999-MHz bands are similarly disabled.

The 6- to 7.9999-MHz band is disabled by U7A. The disabling logic (all 0's for U7A) produces a logic 1 at U7A-5. This prevents VR1 from breaking down and keeps Q9 cut off. Pin P1-43 then has a logic 0 (-15 Vdc) as an output to the band circuits of rf module A6. The 4- to 5.9999-MHz, the 3- to 3.9999-MHz, the 2- to 2.9999-MHz, the 560-kHz to 1.9999-MHz, and the 0 to 560-kHz bands are similarly disabled.

4.2.10.2 Decoder/Driver Card A7 608-9087-001

Refer to the schematic in the diagrams section. The decoder/driver card converts the bcd frequency information from frequency control card A14 into three frequency band outputs: band 1, 0 to 0.5599 MHz; band 2, 0.5600 to 1.9999 MHz; and band 3, 2 to 29.9999 MHz. The operation of each band is described using one assumed input frequency in each band.

On band 1, assume an input frequency of 440 kHz. The 10-MHz and 1-MHz input lines are logic 0; the 100-kHz-2-8 and 10-kHz-8-2 input lines are logic 0, and the 100-kHz-4 and 10-kHz-4 input lines are logic 1.

The logic 0 on the 10-MHz and 1-MHz input lines to the base of Q1 maintains Q1 in an off state. The +5 Vdc (logic 1) on the collector of Q1 cuts off Q2 and disables band 3 (pin P1-56). The logic 1 from the collector of Q1 is applied as one of the enabling signals to the input of U3A.

The other enabling signals for U3A (band 1) are derived from the logic inputs to the 10-kHz, 100-kHz, and 1-MHz-1 input lines. The 10-kHz-2 (logic 0) and -4 (logic 1) are applied to U1B. The logic 1 output of U1B is applied to U1C, the 10-kHz-8 (logic 0) is inverted by U2C and applied to U1C. The logic 0 output of U1C is applied to U3B-9 and 10. The 100-kHz-1 (logic 0) and -4 (logic 1) are applied to U3B. The logic 1 output of U3B is applied to U3A-5. The 100-kHz-2 (logic 0) and -4 (logic 1) are applied to U1A. The

logic 1 output of U1A is applied to U1D, the 100-kHz-8 (logic 0) is inverted by U2B and applied to U1D. The logic 0 output of U1D is inverted by U2E and applied to U3A-4. The 1-MHz-1 (logic 0) is inverted by U2F and applied to U3A-2. The logic 0 output of U3A enables Q3 and in turn enables band 1 (pin P1-86). The logic 0 output of U3A is applied through CR7 as a disabling signal to band 2 (U2D and Q4).

To enable band 2, assume an input frequency of 1 MHz. All bcd input lines are at logic 0 except 1 MHz-1. The 1-MHz-1 (logic 1) is inverted by U2F and applied to U3A-2, the output of U3A goes to a logic 1 that disables Q3 (band 1) and is inverted by U2D and applied to Q4. Q4 conducts, and band 2 (pin P1-84) is enabled.

To enable band 3, assume any input frequency between 2 and 29.9999 MHz. A logic 1 on the 10-MHz input lines or the 1-MHz-2, -4, -8 input lines will cause Q1 to conduct; the logic 0 output of Q1 turns on Q2 and enables band 3 (pin P1-56). Simultaneously the logic 0 output of Q1 disables U3A (band 1) and is applied through CR6 and U2D as a disabling signal to Q4 (band 2).

4.2.10.3 Decoder/Driver Card A7 608-9621-001

Refer to the schematic in the diagrams section. Decoder/driver card 608-9121-001 is functionally the same as decoder/driver card 608-9087-001 except in addition to the 3-band output, all bcd inputs are routed through two buffer stages (inverters) and applied to P1 as bcd outputs. Bcd information is required when an external preselector is used with the 651S-1/1A.

4.2.11 Frequency Control Card A14

Refer to the schematic in the diagrams section. Frequency control card A14 receives frequency control inputs from the following three front-panel tuning controls: 1-MHz control S111 that selects frequencies in 1-MHz steps, 0.1-MHz control S110 that selects frequencies in 0.1-MHz steps, and variable tuning control S109 that selects frequencies in 100-Hz steps.

Card A14 converts the frequency information from the front-panel controls to 22-bit bcd parallel data. This frequency data is sent to the frequency synthesizer cards and to the bcd to 7-bar decoder/driver circuits on card A14. The 7-bar decoder/drivers control the 7-bar numeric readout tubes on the front panel of the receiver (refer to the chassis schematic in the diagrams section).

Card A14 uses 5 up-down bcd counters to develop 20 bits of the 22-bit bcd frequency information. These counter outputs represent 100-Hz, 1-kHz, 10-kHz, 0.1-MHz, and 1-MHz 4-bit bcd (1, 2, 4, and 8) frequency information. The remaining 2 bits, representing 10-MHz, 2-bit bcd (1 and 2) frequency information, are developed by flip-flops U27 and U34 on card A14. Each up-down counter controls a 7-bar decoder/driver, and flip-flops U27 and U34 control a 7-bar decoder/driver.

4.2.11.1 Counter Operation

Up-down counters U21 through U25 require certain inputs for proper operation. A logic 1 signal must be applied to count enable input pins 13 through 18 and to parallel entry enable pin 23. A count direction signal (logic 1 for up, logic 0 for down) must be applied to pin 2, and a clock pulse must be applied to pin 1.

The logic 1 parallel entry enable signal on pin 23 is provided by Q7. This logic 1 also enables the first stage of NAND gates following each up-down counter, allowing the outputs from each counter to be inverted by these NAND gates.

The logic 1 count enable signals on pins 13 through 18 are provided by a +5-Vdc keep-alive voltage and by terminal count signals from preceding up-down counters. A terminal count logic 1 output appears at pin 11 of an up-down counter when the counter reaches state 9 (1001) and the count direction signal is logic 1 (up), or when the counter reaches state 0 (0000) and the count direction signal is logic 0 (down).

The local/remote line is logic 1 during local operation. This logic 1 enables the second stage of NAND gates following each up-down counter, allowing a second inversion of the up-down counter outputs. The outputs from these NAND gates are routed to the frequency synthesizer cards and to the bcd to 7-bar decoder/drivers on card A14. The local/remote line is logic 0 during remote operation. This logic 0 disables the second stage of NAND gates, allowing remote frequency information to be fed into the control card.

The clock pulse and count direction signals are generated when any one of the three front-panel frequency controls is changed. Three clock pulse signals (CP, CP', and CP") and three up-down signals (U/D, U/D', and U/D") are developed by card A14.

Clock pulse CP is developed when the position of variable tuning control S109 on the front panel is changed. This clock pulse is applied to terminal 1 of up-down counters U21, U22, and U23, and to gate U32B. Clock pulse CP1 is developed either by clock pulse CP or by changing the position of 0.1-MHz control S110 on the front panel. This clock pulse is gated through U32B, inverted by U31D, and applied to terminal 1 of up-down counter U24 and gate U40B. Clock pulse CP" is developed either by clock pulse CP' (which can be developed by clock pulse CP) or by changing the position of 1-MHz control S111 on the front panel. Clock pulse CP" is gated through U40B, inverted by U39D, and is applied to terminal 1 of up-down counter U25 and to the clock inputs of flip-flops U27 and U34.

The three clock pulses permit tuning in 100-Hz, 0.1-MHz, or 1-MHz steps. A clock pulse, however, does not produce a count change from an up-down counter output unless a terminal count signal (logic 1) has been received from the preceding up-down counter (or counters). For example, if tuning were progressing upward in 100-Hz steps, a 1-kHz count pulse from counter U22 would be developed only on the pulse following the 900-Hz count pulse from counter U21.

On 0.1-MHz counter Q24 and 1-MHz counter U25, a terminal count signal may be forced by one of the front-panel frequency controls. As the 0.1-MHz control S110 is being rotated through position A or B, a logic 0 is applied to input pin 13 of gate U30C. This logic 0 forces a logic 1 input to count enable pins 13, 14, and 15 of up-down counter U24 and permits tuning in 0.1-MHz steps. Likewise, as the 1-MHz control S111 is being rotated through position A or B, a logic 1 is applied to pins 13, 14, and 15 on counter U25 and permits tuning in 1-MHz steps. When either switch S110 or S111 is turned one position clockwise, contacts A and B are shorted, then opened in the detent position. Contact C is shorted in the detent position.

The up-down signals are developed by the same controls that produce the clock pulse signals. Signal U/D is developed by changing the position of variable tuning control S109 on the front panel, signal U/D' is developed either by signal U/D or by changing the position of 0.1-MHz control S110 on the front panel, and signal U/D" is developed by signal U/D' or by changing the position of 1-MHz control S111 on the front panel. The up-down signals indicate the direction of change of the up-down counters. A logic 1 up-down signal produces a count increase with a properly enabled clock pulse and a logic 0 produces a count decrease with a properly enabled clock pulse.

4.2.11.2 Local/Remote Control

Local or remote control is selected by LOCAL/REMOTE switch S108 on the front panel. In local operation, a logic 1 input is applied to pin P1-57 on card A14 by LOCAL/REMOTE switch S108. This logic 1 is inverted by U36B and the resulting logic 0 disables remote frequency load gate U35D. The logic 1 at P1-57 is also applied to gates U36A, U37A, U37B, U29C, and to the second stage of NAND gates following each up-down counter. The logic 1 on gates U37A and U37B allows the parallel entry enable logic 1 from Q7 to be applied to pin 23 on each up-down counter and to the gates in the first stage of NAND gates following each counter. Normal tuning then proceeds by making use of the three front-panel frequency controls.

DIAL LOCK switch S113 on the front panel is used to prevent accidental change of frequency during local operation. In the LOCK position, switch S113 applies a logic 0 to P1-5 on card A14. This logic 0 disables 100-Hz tuning gate U36A and prevents the recognition of any change in position of variable tuning control S109.

In remote control operation, a logic 0 input is applied to pin P1-57 by LOCAL/REMOTE switch S108. This logic 0 disables gate U36A and prevents and frequency change by the .1 MHZ selector. The logic 0 is also applied to gates U37A, U37B, U29C, and to the second stage of NAND gates following each up-down counter. The resulting logic 1 from U37A turns on transistor Q7 and Q7 turns off all the up-down counters by applying a logic 0 to terminal 23 of each

counter. This logic 0 allows each up-down counter to be preset to the logic levels appearing on pins 19, 20, 21, and 22 in the event of a clock pulse on pin 1. The logic 0 from Q7 also forces a logic 1 output from each gate in the first stage of NAND gates following the up-down counters. The gates in the second stage of NAND gates have logic 0 on the local/remote inputs, resulting in logic states at the outputs from these NAND gates corresponding to the remote bcd frequency data from the DCFE circuits. The frequency load input at A14 P1-64 generates a clock pulse that loads each counter with the logic state appearing at the outputs of the second stage NAND gates.

In remote operation, the inputs to the 7-bar decoder/drivers come from the DCFE circuits, rather than from the second stage of NAND gates following the up-down counters. The bcd frequency information from the DCFE circuits appears on the signal lines that served as outputs to the frequency synthesizer cards during local operation. The bcd to 7-bar decoder/drivers then control the 7-bar numeric readout tubes on the front panel as in local operation.

4.2.12 Power Supply Circuits and Regulator Card A1

Refer to the chassis schematic and card A1 schematic in the diagrams section. The power supply circuits are in two locations in the receiver. The supply circuits are on the rear chassis and the regulator circuits are on card A1. In the chassis circuits, multiple-secondary transformer T201 converts the 115/230 V, 47- to 420-Hz input power to 10-, 15-, and 18-V ac levels. Bridge rectifiers, RC ripple filters, and series regulator transistors provide +5, +25, and -15 Vdc for the regulator card.

Also on the rear chassis are connection points for a 6-V battery (available option). This battery power is used for the +5-VKA (keep-alive voltage) input to frequency control card A14 for up to 30 seconds if a primary power shortage occurs. This prevents A14 from losing frequency information. The battery is switched off when the POWER switch is set to OFF. A lamp on the front will light if primary power is lost and the battery is being drained.

Regulator card A1 uses +25 Vdc to provide +25-Vdc switched, +15-Vdc switched, and +15-Vdc continuous outputs. The +5-Vdc input is used to provide +5 Vdc switched and continuous outputs and the -15-Vdc input is used to provide -15 Vdc switched and continuous outputs.

Integrated circuit regulators are used for all three major inputs. Series regulating transistor Q1 is used in addition to integrated circuit U3 for +5-Vdc regulation.

The +15-Vdc switched, -15-Vdc switched, and +5-Vdc switched outputs are applied to performance monitor gate U4A. This gate activates the fault monitor circuits in the optional DCFE card when optional 3-pair serial digital remote control is employed.

The blanking circuits are also on card A1. An 8-ms blanking pulse is generated on frequency control card A14 any time one of the frequency tuning controls is changed to allow the frequency synthesizer circuits to lock on the newly selected frequency. The circuits on card A1 switch the pulse and apply an af blank signal to audio card A2. The af signals are blanked (muted) to keep background noises out while tuning.

4.2.13 Interconnect Card A8

Refer to the schematic in the diagrams section. Interconnect card A8 routes the manual mode control information and other miscellaneous controlling functions to the various cards and circuits that would be controlled by the optional cards when remote control is employed. Interconnect card A8 is replaced by DCFE card A8 when 3-pair serial digital or teletypewriter code remote control is used (card A9 must also be installed for remote control operation).

4.2.14 DCFE Card A8 (Optional)

Refer to the schematic in the diagrams section. The DCFE (device control functional element) controls all the operations of the receiver based on the commands from the external control. Serial digital control information from the control is demodulated in and gated through DCU card A9, and is applied to the DCFE in serial form. TTY-coded control information is decoded in and gated through TCU card A9, and is applied to the DCFE in serial form. The

DCFE then converts the serial control commands to parallel form and enables or disables the appropriate functions in the receiver.

The control commands to the DCFE are divided into four control words (I, II, III, and IV), and may be sent in any order depending on the processor programming. Word I is frequency control, word II is mode I control, word III is mode II control, and word IV is monitor request. Each word comes in separately, and immediately after the reception of each properly addressed control word, a monitor word is returned to indicate the receiver's reaction to the control word. If the receiver reacted improperly, the control word is retransmitted; if it reacted properly, the next control word will be transmitted. Word IV (monitor request) is repeated continuously until something faults or is changed, to indicate the operational status of the receiver at all times. Table 6 lists the content and format of all the control words. Table 7 shows control word II programming for mode selection.

Other cards in the receiver generate the monitor signals that indicate the operational status of the receiver during the word period immediately following a properly addressed control word. These parallel binary signals are applied to the DCFE for transfer to the processor control unit (through DCU card A9 that converts the parallel data to serial data) or to the TTY (through TCU card A9). The monitor data sampled and sent to the DCFE depends upon the type of control word received. Table 8 lists the content and format of the monitor words.

Table 6. Control Words, Content and Format.

BIT POSITION	CONTROL WORD I (Freq info)	CONTROL WORD II (Mode I info)	CONTROL WORD III (Mode II info)	CONTROL WORD IV (Monitor request)
0	Dialogic bit	Dialogic bit	Dialogic bit	Dialogic bit
1	X	X	X	X
2	X	X	X	X
3	X — 5-bit DCU address	X — 5-bit DCU address	X — 5-bit DCU address	X — 5-bit DCU address
4	X	X	X	X
5	X	X	X	X
6	0 — DCFE subaddress	0 — DCFE subaddress	1 — DCFE subaddress	1 — DCFE subaddress
7	0	1	0	1
8	Parity	Parity	Parity	Parity
9	X	X	X	X
10	(2) — 10 MHz	FM enable	X	X
11	(1)	AM enable	X	X
12	(8) — 1 MHz	SSB/CW enable	X	X
13	(4)	ISB enable	X	X
14	(2)	Fixed BFO enable	X	X
15	(1)	VBFO enable	X	X
16	(8) — 100 kHz	Interpolate enable	X	X
17	(4)	X	X	X
18	(2)	AGC fast enable	X	X
19	(1)	0.2-kHz filter enable — 450-kHz filters	X	X
20	(8) — 10 kHz	2.7-kHz USB filter enable — 450-kHz filters	X	X
21	(4)	2.7-kHz LSB filter enable — 450-kHz filters	X	X
22	(2)	6-kHz filter enable — 450-kHz filters	X	X
23	(1)	450-kHz bypass — 450-kHz filters	X	X
24	(8) — 1 kHz	0.5-kHz filter enable — 10.35-MHz filters	(8) — VBFO	X
25	(4)	1-kHz filter enable — 10.35-MHz filters	(4) — VBFO	X
26	(2)	3-kHz filter enable — 10.35-MHz filters	(2) — VBFO	X
27	(1)	10.35-MHz bypass — 10.35-MHz filters	(1) — VBFO	X
28	(8) — 100 Hz	AGC off	(8) — Rf gain	X
29	(4)	Operate	(4) — Rf gain	X
30	(2)	Local/remote	(2) — Rf gain	X
31	(1)	X	(1) — Rf gain	X

Note: X = don't care

Table 7. Control Word II Mode Selection Programming.

DESIRED MODE OF OPERATION AND BANDWIDTH	WORD II BIT POSITION (LOGIC 1 FOR DESIRED FUNCTION)			
	MODE SELECT	BFO ENABLE (Choose one Only)		
		BFO (Fixed)	VBFO	INTERPOLATE BFO
FM 6 FM 16	10, 22, 27 10, 23, 27, 28			
AM 3 AM 6 AM 16	11, 22, 26 11, 22, 27 11, 23, 27			
SSB 2.7 kHz USB SSB 2.7 kHz LSB ISB	12, 20, 27 12, 21, 27 12, 13, 20, 27	14 14 14		16 16 16
CW .2/1/NSRT CW .5/CW/2 CW 1/4/WSRT/WBTY	12, 19, 24 12, 22, 24 12, 22, 25	14 14 14	15 15 15	

Table 8. Monitor Words, Content and Format.

BIT POSITION	MONITOR WORDS I, III, AND IV	MONITOR WORD II
0	Dialogic bit	Dialogic bit
1	0	0
2	1	1
3	0 *5-bit DCU address	0 *5-bit DCU address
4	1	1
5	0	0
6	0, 1, 1 DCFE subaddress	0 DCFE subaddress
7	0, 0, 1	1
8	Parity	Parity
9	Power interrupt	Power interrupt
10	(2)	Power supply performance
11	(1) 10 MHz	Synthesizer lock
12	(8)	Local/remote
13	(4)	Operate
14	(2) 1 MHz	Audio performance
15	(1)	Store frequency
16	(8)	Mode
17	(4)	Mode
18	(2) 100 kHz	Mode Refer to table 9.
19	(1)	Mode
20	(8)	(8)
21	(4)	(4)
22	(2) 10 kHz	(2) VBFO
23	(1)	(1)
24	(8)	(8)
25	(4)	(4)
26	(2) 1 kHz	(2) 1 kHz
27	(1)	(1)
28	(8)	(8)
29	(4)	(4)
30	(2) 100 Hz	(2) 100 Hz
31	(1)	(1)
*Example address		

Table 9. Mode Selection for Monitor Word II.

MODE	BIT			
	16	17	18	19
FM	0	0	0	0
AM	1	0	0	0
USB, VBFO	0	1	1	0
USB, FIXED BFO	1	1	1	0
LSB, VBFO	0	1	0	1
LSB, FIXED BFO	1	1	0	1
CW, VBFO	0	1	0	0
CW, FIXED BFO	1	1	0	0
ISB, VBFO	0	1	1	1
ISB, FIXED BFO	1	1	1	1

4.2.14.1 Control Word Processing

The control data from the DCU or TCU is applied to the DCFE along with the control gate, monitor gate, bit clock, and weight 4 signals. The control data input to the DCFE consists of bits 6 through 31 of the control word received by the DCU. Bits 0 through 5, dialogic bit, and address bits, are extracted by the DCU or TCU. Bits 6 and 7 (subaddress) of control word define which of the control words (I, II, III, or IV) is present, and bits 8 through 31 contain the control information to be processed by the DCFE for use throughout the receiver. The logic levels of the control gate, monitor gate, monitor data, bit clock, and weight 4 signals are shown in figure 12 (DCU theory).

One of the initial functions of the DCFE is the generation of word I, word II, and word III load commands to enable the loading of the control information (bits 8 through 31) into the proper storage registers. The word I storage registers are U16, U20, U24, U28, U32 and U36; word II storage registers are U19, U23, U27, U31 and U35; and word III storage registers are U34 and U38. Shift register U6 stores the subaddress information from bits 6 and 7 of the control word and provides inputs to the word load gate circuits where the appropriate load gate is generated.

U6 is a 4-bit shift register that provides one of two alternate shift modes (serial shift right or parallel). The shift mode is selected by the application of a logic 0 or logic 1 to mode input pin M.

Refer to figure 7. The control data and control gate inputs are applied in both the true and inverted states to SR flip-flop circuits U2A and U2B. The control word used as an example in figure 7 is control word II with subaddress bit 6 at logic 0 and subaddress bit 7 at logic 1.

The T-output (control data) of U2A is applied to the shift right serial (DS) input of U6. The T-output of U2B (control gate) is combined with the inverted output from U6-6 and applied to the mode control input (U6-M).

The F-output of U2B is combined with the control gate input and applied to the parallel strobe input (U6-S).

During a 36-bit monitor word period and the dialogic and 5-bit address period of the following control word, the mode control signal is held at logic 1, which holds U6 in the parallel shift state. Also, the logic 0 to 1 change of the control gate causes a logic 1 to 0 transition at the U6-S input and U6 shifts the parallel inputs (1, 7, 9, 12) to the outputs of U6 (6, 8, 11, 13). At the middle of bit period 6, the mode control signal changes to logic 0 and causes U6 to switch to the shift right state. When the clock signal goes to logic 0 at the end of bit period 7, U6-6 goes to logic 1 causing U6 to return to the parallel shift state where it remains until the control gate delayed by 1/2 bit ($CG_{1/2}$) from U2B-12 goes to logic 1. During the 2-bit shift right period, subaddress bits 6 and 7 are shifted to outputs 11 and 13 of U6 where they also remain for the same period. The subaddress bits are removed at the logic 0 to 1 change of the next control gate signal when the logic 1 to 0 strobe signal is applied to the parallel strobe input of U6. The subaddress outputs from U6 are applied to the word load logic circuits.

The output of the word gate timing circuit (U8B, U3A, U3B and U1E) that is applied to the word load logic circuits, is at logic 0 when the control gate is at logic 1. This logic 0 signal inhibits the word load logic circuits during this period by holding the outputs of U13A, U13B, and U13C at logic 1 (the enable signal is logic 0). Assuming control word II was sent, subaddress output from U6 (control word II) is applied to the word load logic circuits and the three outputs remain at logic 1 through bit period 31. At bit period 32 the control gate changes to logic 0 causing

the output of the word gate timing circuit to change to logic 1. The logic 1 timing signal causes the output of U13A to change to logic 0, the enable signal for the word II load output. The remaining two load gate outputs are unchanged. The logic 0 word II load gate is inverted and applied to the proper storage registers as a logic 1 load word II signal. The reason the load gate appears at the end of the control word period is to allow the entire control word to be loaded through the shift registers to the storage registers. The entire word is then shifted out when the load gate triggers the storage registers. The load pulse lasts 1/2 clock pulse and load storage is enabled by a logic 1.

The primary mode output signal is produced by the primary mode logic circuit and is at logic 0 only when both the control gate delayed by 1/2 bit ($CG_{1/2}$) and monitor gate inputs are at logic 0. The primary mode output is used for mode control (serial shift right or parallel shift) of the shift registers.

Power interrupt circuit U5 (refer to the schematic) provides a logic 1 power interrupt signal to the monitor circuits whenever a power interruption of more than 50 μs occurs. Depending upon processor programming, the line processor upon reception of a power interrupt signal may retransmit all three control words to prevent the possibility of a voltage transient being interpreted as control information.

The frequency load output is produced whenever a frequency control word (word I) is received. Under normal conditions, the load word I signal from U12C, except during the period when word I is being processed, is at logic 1, causing the frequency load output (U7A-11) to be logic 0. At the end of a word I control period, the word I load output from U12C changes to 0 and clocks U7A, causing a logic 1 frequency load output from U7A-11 for 1/2 bit period. This logic 1 is applied to frequency control card A14 to enable the frequency change circuits.

4.2.14.2 Shift and Storage Register Functions

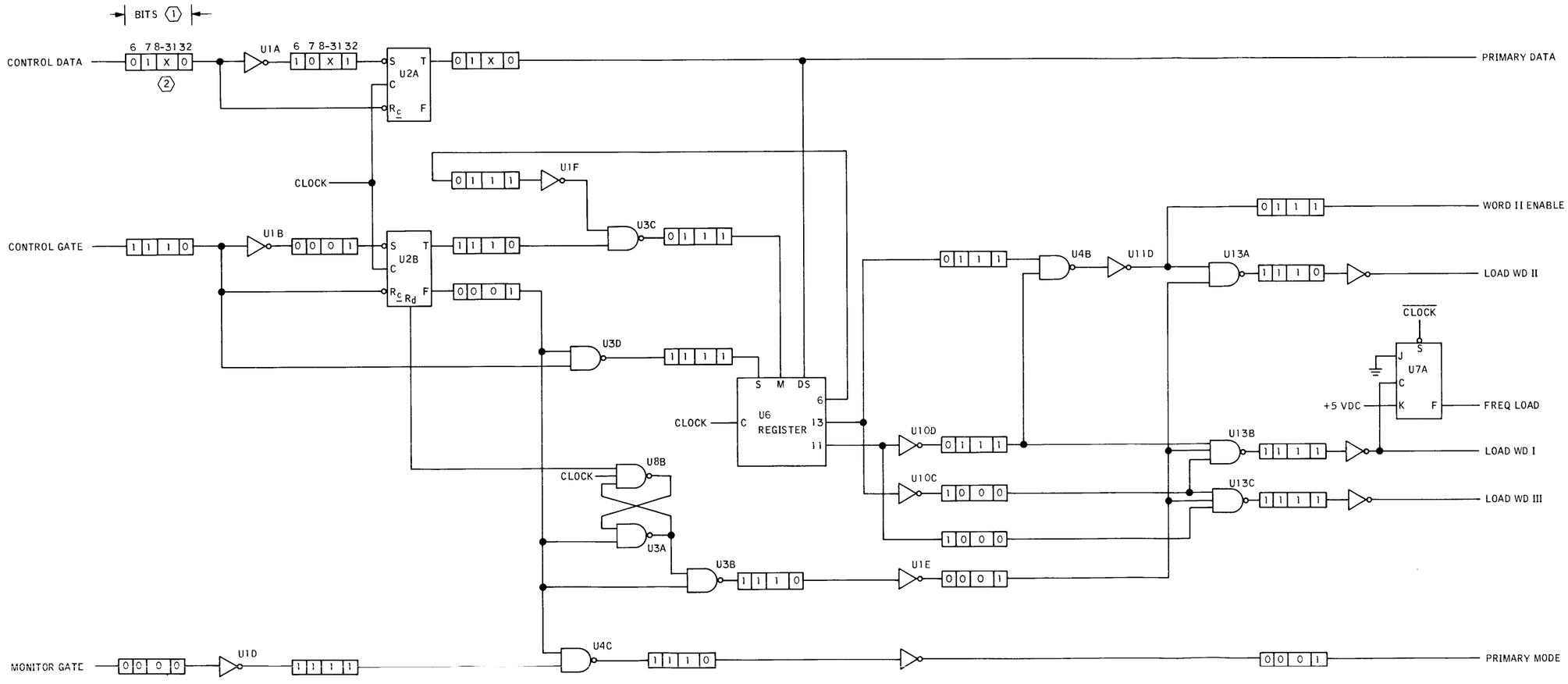
Figure 8 shows the typical operation of one shift register and two associated output storage registers. The operation of all these registers in the DCFE is identical. During a control word command period (bits 8 through 31) the primary mode signal is at logic 0 and is applied as the shift-right mode signal to U37-5. During this period, primary data (control information) is applied to data shift input U37-14 and is shifted serially from the four output lines of U37 to the inputs of U35 and U36. Shift register U37 is the first register to receive control information so all control bits in the control word must be shifted through it. At the end of bit period 31, the primary mode signal changes to logic 1, U37 then switches to the parallel shift mode and holds the last four bits of the control word (28 through 31) on the four parallel output lines. The previous bits have been shifted out on output number 4 (pin 6) of U37 to the shift right serial input (pin 14) of the succeeding shift registers (U33, U29, U25, U21, and U17).

Assume that frequency control information, control word I, is being processed. At bit period 31, the last four bits of frequency control information are on the four outputs of U37 and are held there because U37 is in the parallel shift mode. At bit period 32 the word I load gate input goes to logic 1 for 1/2 bit and is applied to the load input (pin 2) of storage register U36. The logic 1 load signal loads the frequency information onto the four outputs of U36 where it remains until the appearance of another logic 1 load gate. The other storage register has the same frequency information at the input, but the absence of the required load gate prevents the information from being loaded onto its output. These frequency outputs are applied, at this point, to all the applicable cards in the receiver and the cards then perform their respective functions.

Control bits 24 through 31 are loaded onto U34 and U38 for word III storage and generation. These registers operate the same as the registers mentioned above.

4.2.14.3 Monitor Word Processing

At the completion of a control word, monitor responses throughout the receiver are applied through the DCFE to the DCU for modulation. After control word I is processed by storage registers U16, U20, U24, U28, U32 and U36, the bcd frequency selected is monitored. Bcd information for 10 MHz-2 through 10 kHz-1 is applied to the B inputs of U18, U22, U26, and

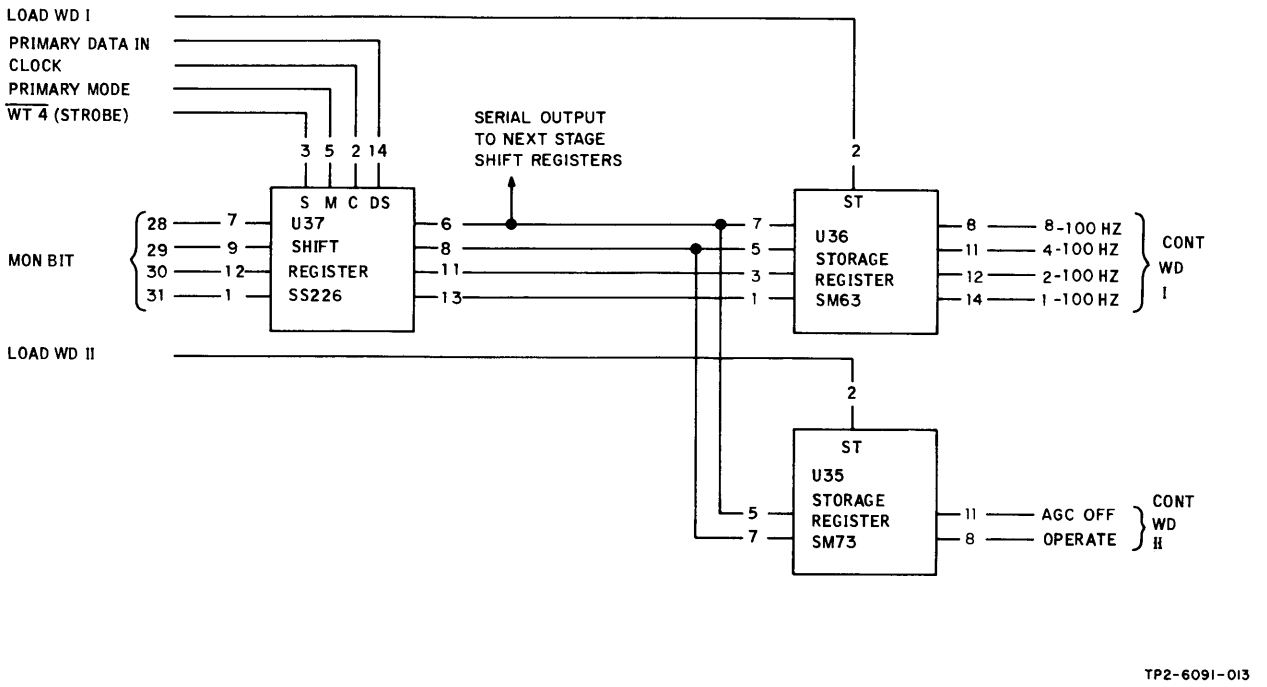


NOTES:

1. LOGIC STATE OF CONTROL WORD II SHOWN IN ALL LOGIC STRIPS.
2. X IN LOGIC STRIP DENOTES EITHER LOGIC 1 OR 0, NO EFFECT ON EXAMPLE.

TP3-0687-014

DCFE Control Word Routing, Functional Diagram
Figure 7



DCFE Shift Register/Storage Register Operation Functional Diagram
Figure 8

U30. Refer to figure 10. Bcd information for 1 kHz-8 through 100 Hz-1 is applied to U33 and U37. That portion applied to the 2-input, 4-bit multiplexers (U18, U22, U26, and U30) is sent directly to U17, U21, U25, and U29 because there is no word II enable signal at pin 9 of the multiplexers.

All the monitor bits are now at the parallel inputs of shift registers U17, U21, U25, U29, U33, and U37. The strobe (WT 4) input goes to logic 1 after bit 3 resulting in a logic 0 $\overline{\text{WT 4}}$ signal The $\overline{\text{WT 4}}$ strobe signal allows the inputs to be loaded onto the output lines of the registers. When the monitor gate goes to logic 1, the primary mode input changes to logic 0 (figure 9) and the registers switch to the serial shift right state. The monitor data is then serially shifted out of all the registers through U9 to the DCU.

Storage registers for the control words are unaffected during this operation due to the lack of proper control word gate signals. (Figure 9 also shows the timing relationship between monitor gate, control gate, control gate delayed 1/2 bit ($CG_{1/2}$), U6 enable and output signals, LD WD I, frequency load, and primary load signals.)

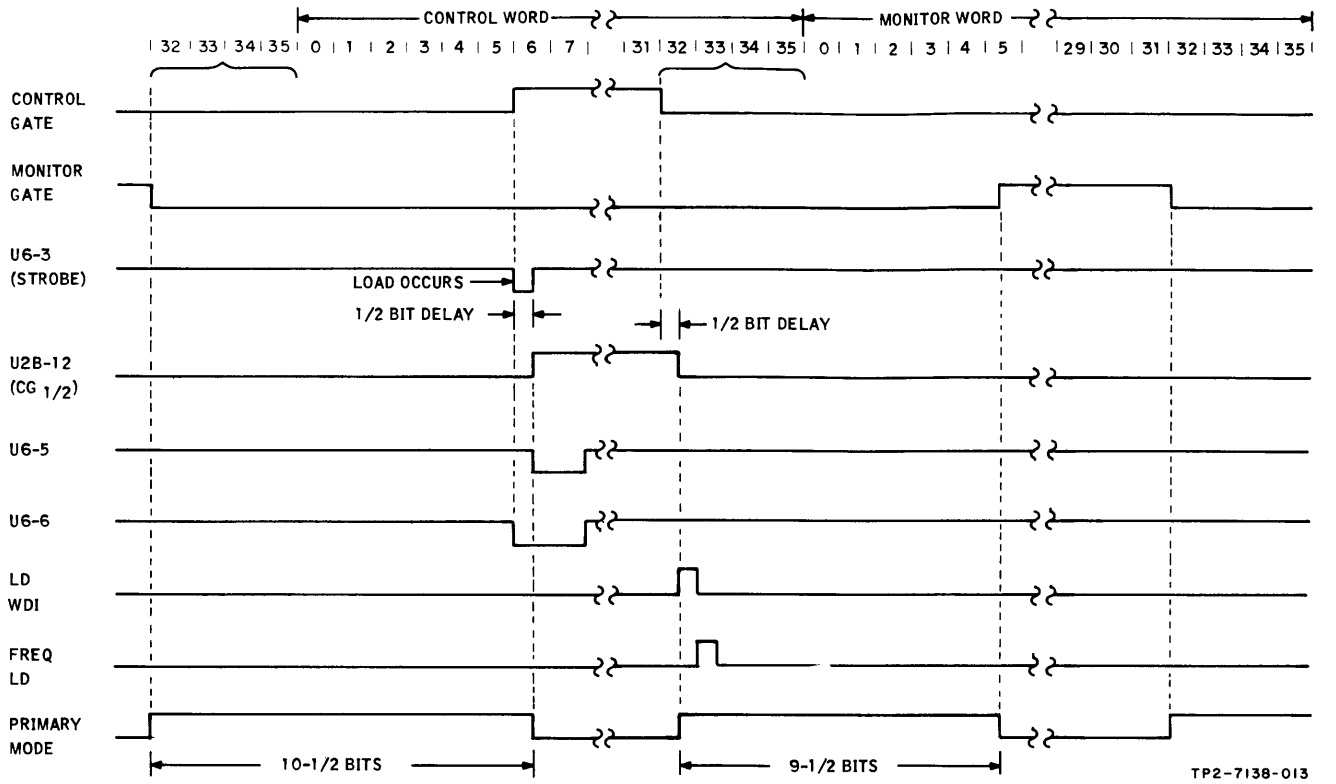
After control word II is processed, the same operation occurs, except that mode type monitor data is sent to the DCU. This mode monitor information is applied from various points in the receiver to the A inputs of multiplexers U18, U22, U26, and U30. This information is gated through the multiplexers upon the application of the word II enable signal. Word II enable occurs during control word II and during the following monitor word period (figure 7).

4.2.14.4 Local/Remote Switching

If the DCFE card is in place during local operation, control signals must pass from the front panel through the DCFE to the applicable cards. The local mode signals are applied to a diode matrix that applies them to the same output pins as the storage registers during remote control.

Relay K1 switches local/remote mode information to the pertinent cards. This relay is energized during remote control and is deenergized during local control.

Frequency tuning control information bypasses the DCFE during local operation and is applied directly to frequency control card A14. Frequency information, however, is monitored by



DCFE Enabling Signals, Timing Diagram
Figure 9

the DCFE in local operation and is transferred to the line processor by monitor words as described in 4.2.14.3.

4.2.15 DCU Card A9 (Optional)

4.2.15.1 DCU Card 793-9414-001

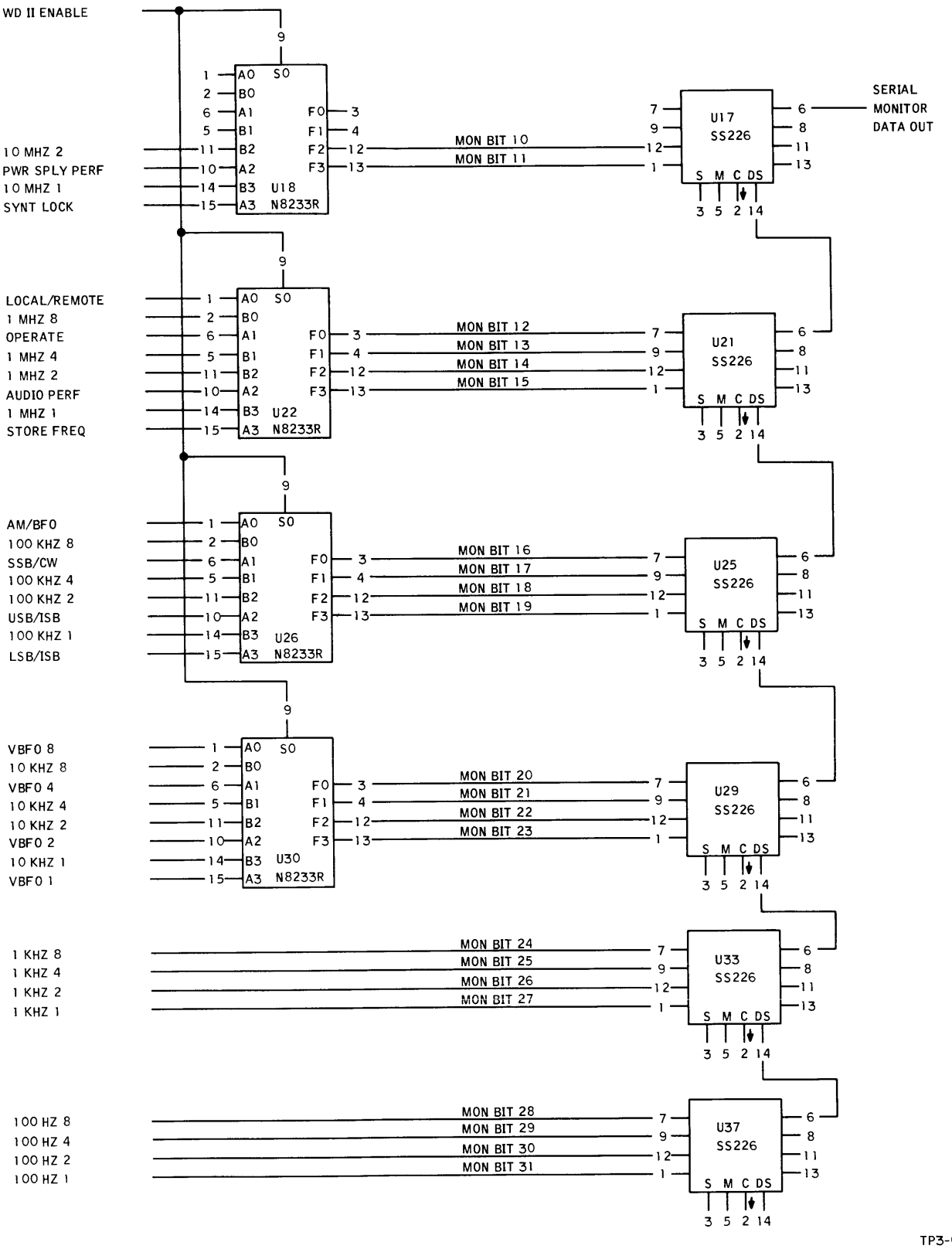
Refer to the schematic in the diagrams section. The DCU (device control unit) is a half-duplex device that accepts phase shifted sine-wave data from a digital processor on the control bus, converts it to digital data, and when properly addressed, permits DCFE card A8 to process the controlling portion (oper field) of this digital data. Alternatively, the DCU accepts digital data in serial form from the circuits of the DCFE, converts it to phase shifted sine-wave data, and transmits the sine-wave data to the DCU driver on the monitor bus. All operations within the DCU are synchronized by a sine-wave timing signal that is applied to the DCU on the carrier bus. The DCU converts this sine-wave signal to a digital bit clock signal. Figure 11 shows the three interface signals that are transmitted to and from the DCU.

4.2.15.2 DCU Control Bus to DCFE Data Transfer

Data from the digital processor is applied to the DCU on the control bus in the form of a biphase modulated sine wave. The control word formats are explained in the DCFE theory. The control word is routed through DCU interface amplifier U502 and is applied to U602 and U603. The half-wave rectified signal from U602 is filtered by integrator R12 and C7 to establish a dc reference level for comparator U603. The dc level is maintained at approximately one-half the peak value of the signal at the control bus terminals.

The output from U603 is a string of positive pulses that represents the demodulated serial data. (During the supervisory interval, the output from U603 is low.) The demodulated data from U603 passes through voltage shaper U404B and is then applied to the detector circuit.

The serial control information is detected by noting the relative position of the positive



DCFE Monitor Operation, Functional Diagram
Figure 10

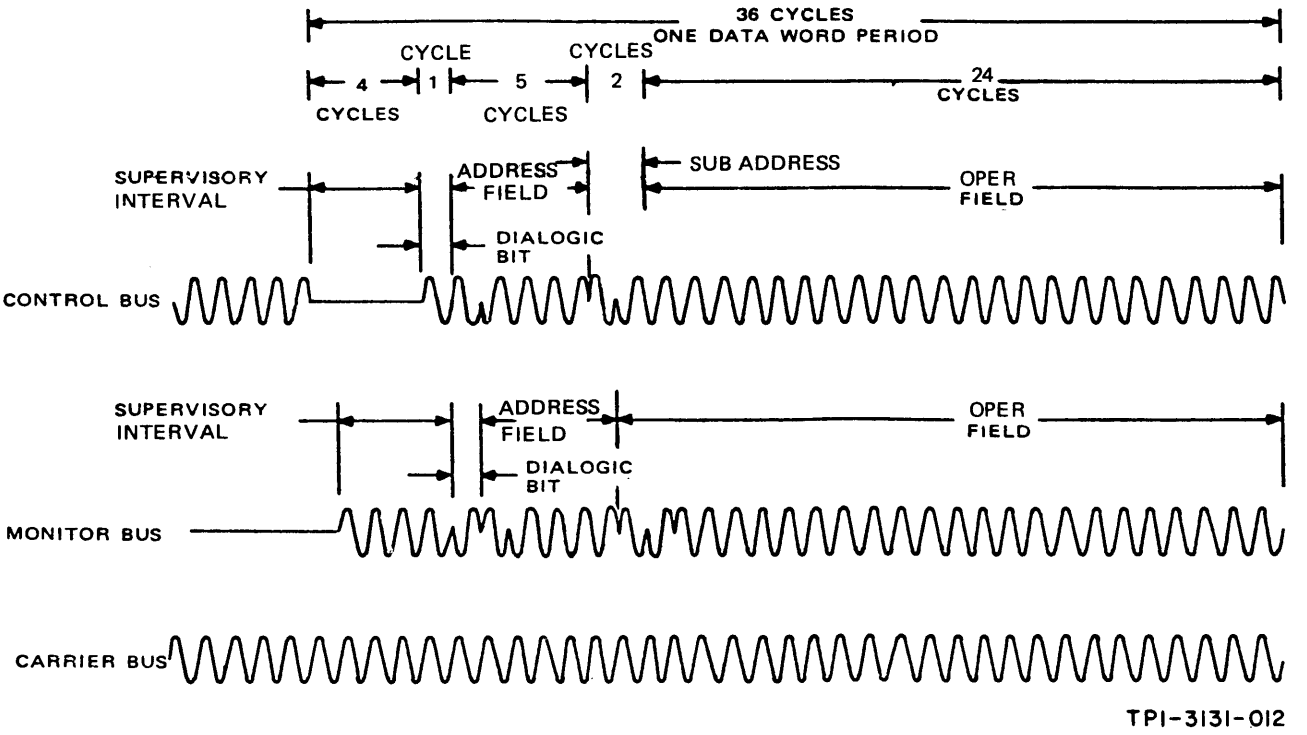
pulses from U404B during each bit cycle. The pulses are applied to flip-flops U402A and U402B and the positions of the pulses are decoded by U401A and U401D. U402A and U402B are clocked by the sampling clock and its inverse. (The sampling clock is shifted 90 degrees from the bit clock.)

If a positive pulse occurs early in a bit cycle, a logic 1 appears at U402B-Q and a logic 0 appears at U402A-Q. U401A detects this combination and applies a logic 1 to flip-flop U301B for data detection. Any other output combination from U402 results in a logic 0 output from U401A. The detected data is loaded into flip-flop U301B at the end of each bit clock period and U301B provides detected control data and detected control data outputs.

If no positive pulse occurs during a bit cycle, logic 0's appear at U402B-Q and U402A-Q. This combination is detected by U401D, which in turn applies a logic 1 to flip-flop U301A for sync detection. Any other output combination results in a logic 0 from U401D. Flip-flop U301A is loaded with the detected sync data at the end of each bit clock period and it provides the detected sync and detected sync outputs.

The carrier bus input is used to synchronize the timing of the entire operation between the DCU, and DCFE, and line processor. The carrier bus signal is routed through DCU interface amplifier U801, split, and applied to demodulator U802 and amplifier-filter U903. Demodulator U802 converts the carrier signal to a sampling clock for the data detector circuits (U402).

The automatic level control circuit (U903, Q1, and Q2) maintains the constant carrier bus output level (for clocks) despite the variation of the carrier input signal. The output of U903 is applied to differential switch Q2B. If the negative peak of the sine wave of U903 drops below the switching level of Q2A (determined by resistors R30 and R31), Q2A switches on and discharges C26. This reduces the voltage on the gate of Q1 (used as a voltage-controlled



DCU Interface Signals, Timing Diagram
Figure 11

resistor) and reduces the resistance from the junction of R26 and R28 to ground. This attenuates the signal level. If the U903 output is low, Q1 conducts less and more resistance to signal ground is developed, providing less attenuation to the signal.

The sine-wave clock signal is routed, as the modulator clock, to the monitor modulator circuit (U904 and associated circuits). The sine-wave clock is also converted to a square-wave bit clock signal by bit clock amplifier U803 and bit clock gate U404A. This bit clock signal clocks the time base counter, the data detector circuit (U301), and the output control circuits. It is also routed to the DCFE for synchronization purposes.

At this point, the 36 cycles of the control bus word have been operated on by the DCU as follows: the first four cycles (carrier off) were used to produce the det sync and $\overline{\text{det sync}}$ signals to maintain word synchronization, while the remaining 32 cycles of the control bus word have been converted to 32 control data bits. These 32 bits are routed to address recognition circuit U201B. A preselected address, controlled by strapping DCU address bit lines 1 through 5 to either a logic 1 or a logic 0, is applied to address code generator U103. The preselected DCU address from the address code generator is also applied, in serial form, to address recognition circuit U201B. When the address code contained in bits 1 through 5 of the control data word matches the preselected DCU address code, a logic 1 is applied by U101A to the control gate line. This logic 1 on the control gate line notifies the DCFE that a data word containing the correct address for this device (receiver) has been received by the DCU. At this time the DCFE circuits are enabled to process the remaining data bits (bits 6 through 31) that are present on the control data line.

4.2.15.3 Time Base and Output Control Circuits

The time base circuit generates all the timing signals required by the DCU. This circuit consists of an address code generator and a 36-counter circuit. The output control circuit controls the transfer of control and monitor information between the radio control unit, the DCU, and the DCFE. This circuit consists of sync detecting, address recognition, decoding, serial data gating, control and monitor gating, and modulator enabling circuits. Refer to figure 12 for the timing of the DCU.

The 36 counter circuit generates weight 1, 2, 4, 16, and 32 signals and $\overline{\text{weight 1, 2, 4,}}$ and $\overline{32}$ signals. The weight 32 and $\overline{\text{weight 32}}$ signals are applied to sync comparison circuit U201A and are compared by U201A to the det sync and $\overline{\text{det sync}}$ signals during the supervisory interval and during the dialogic and address bit intervals. If the det sync and weight 32 signals are not identical, the DCU is out of sync and flip-flop U102A applies a logic 0 set signal to counter flip-flops U203B, U203A, U204B, U204A, U304A, and U104. This set signal stops the counter and presets the counter flip-flops. When the weight 32 and det sync signals become identical, the set signal is removed and the counter resumes counting.

The last four flip-flops in the 36 counter (U204B, U204A, U304A, and U104) are disabled during the 4-bit supervisory interval. At the end of each 36-bit word period, the logic 0 output (supervisory interval) from U104-Q ($\overline{\text{weight 32}}$) is applied to the K input of counter flip-flop U204B. This logic 0 prevents any output change from U204B with the first 1 to 0 weight 2 transition on the clock input of U204B. The weight 2 clock pulse is also applied to the clock input of U104. The first 1 to 0 weight 2 transition changes the output states of U104, applying a logic 1 to the K input of U204B. The second 1 to 0 weight 2 transition then initiates the 32 count by clocking flip-flop U204B. This, in effect, expands the 32 counter to a 36 counter for use with the 36-bit word format.

The $\overline{\text{weight 32}}$ output is also applied to the set input of U304B. This set input to U304B is logic 0 during the supervisory interval, causing the output from U304B-Q to remain logic 1 during that period. At the end of the supervisory interval, the set input to U304B is changed to logic 1. The outputs from U304B do not change state, however, until the K input (WT 4) is logic 1 (the fourth bit after the end of the supervisory interval) and there is a logic 1 to 0 transition on the clock ($\overline{\text{WT 2}}$) input (the sixth bit after the end of the supervisory interval).

The logic 1 output from U304B-Q allows the bit clock signal to be routed through U304D. The bit clock signal is then applied to the clock input of flip-flop U102B during the first six bits after the supervisory interval (bits 0 through 5, the dialogic bit, and the address bits).

Address code generator U103 produces the dialogic bit (logic 0 in the DCU) and converts the strapped preset address (bit lines 1 through 5) to serial digital data. The dialogic bit and this serial coded address is applied to address recognition circuit U201B. (Strapping a DCU address bit line to ground produces a logic 0 in that bit position of the serial address format, and strapping an address bit line to +3 Vdc produces a logic 1 in that serial bit position.) Detected control data and $\overline{\text{detected control data}}$ signals are also applied to address recognition circuit U201B. If the address code contained in bits 1 through 5 of the control data signal matches the preset coded address from the address code generator, a logic 0 is applied to the K input of U102B. A logic 0 is then applied by U102B-$\overline{Q}$ to control gate U101A.

Six bits after the end of the supervisory interval, the outputs from U304B change states and a logic 0 appears at the U304B-Q output. This logic 0 prevents the bit clock signal from being routed through U403D to flip-flop U102B. If, during the dialogic bit period and the address bit period (bits 0 through 5), address recognition circuit U201B indicated that the DCU was correctly addressed, the logic 0 will remain at the input of control gate U101A.

The logic 0 output from U304B-Q is also applied to control gate U101A. Control gate U101A then applies a logic 1 to the control gate line. This logic 1 enables the proper DCFE circuits and the remaining control data bits (bits 6 through 31) are processed by the DCFE.

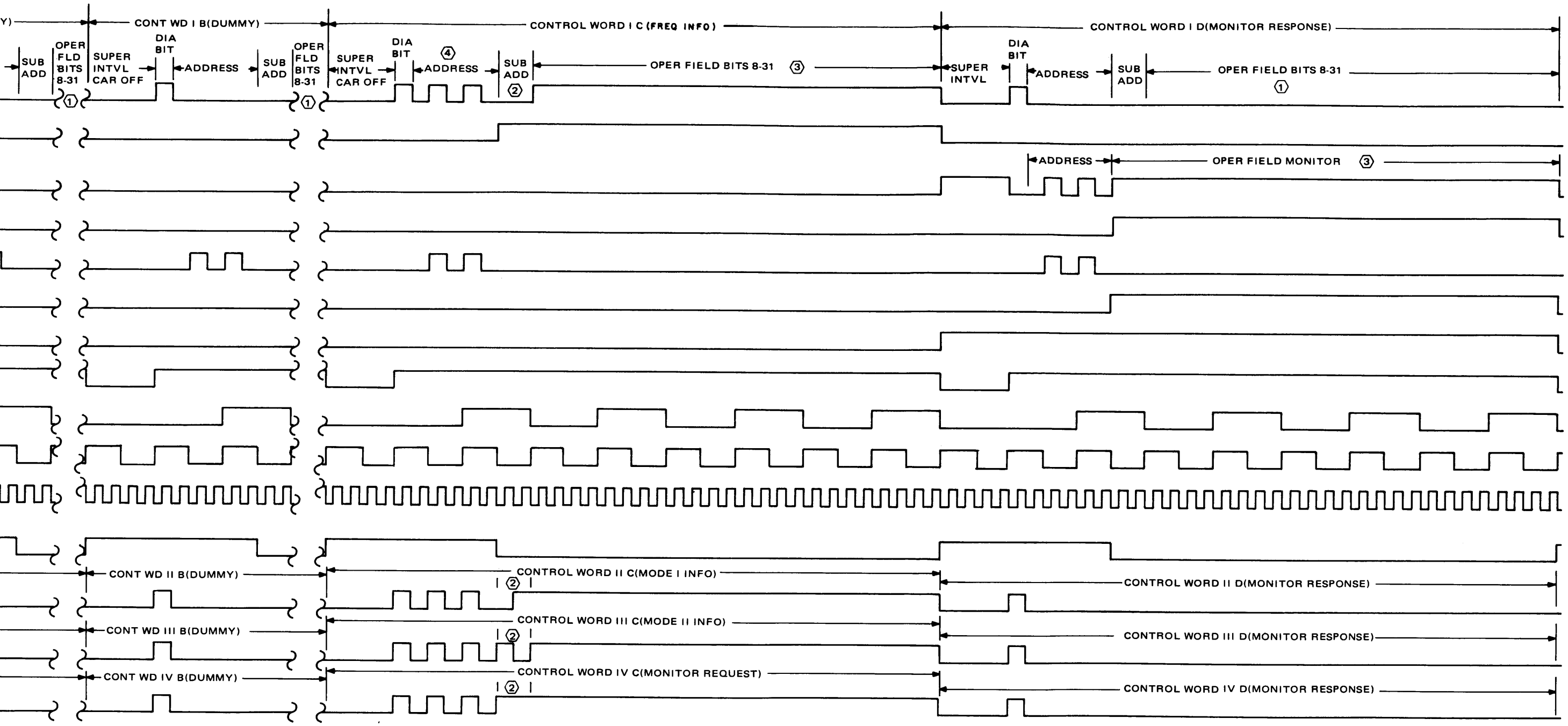
The logic 1 to 0 transition from U304B-Q is also applied to the clock input of U202A. This clock signal enables the transfer of information from flip-flop U102B to flip-flop U202B. If a correctly addressed control word was received by the DCU, a logic 1 is stored at U202A-13. The Q output of U202B, however, was preset to a logic 1 and the $\overline{Q}$ output was preset to a logic 0. These outputs will not change states until the next 1 to 0 transition of the $\overline{\text{weight 32}}$ output from U104-$\overline{Q}$ is applied to the U202B clock input. This transition occurs immediately at the end of the control word when the $\overline{\text{weight 32}}$ signal changes from 1 to 0, and flip-flop U202B is clocked. The outputs from U202B change states and a logic 0 is applied to the input of monitor gate U101D and a logic 1 is applied to modulator enable gates U403B and U403C.

The $\overline{\text{weight 32}}$ logic 0 is also applied to the set inputs of flip-flops U304B and U102B. At the end of the supervisory interval, $\overline{\text{weight 32}}$ changes to logic 1, removing the set inputs to these flip-flops. During the next six bits, U304B applies a logic 1 to monitor gate U101D. Gate U304B also allows the bit clock signal to clock U102B. Since there is no address on the detected control data and $\overline{\text{detected control data}}$ lines, address recognition circuit U201B applies a logic 1 to U102B, resulting in a logic 1 input to control gate U101A. This logic 1 disables the control gate.

The dialogic bit and serial address bits produced by address code generator U103 are applied to serial data gating circuit U303A. This serial address data is then routed through U303B for insertion into the monitor word.

Six bits after the supervisory interval, the output from U304B-Q changes to a logic 0, enabling monitor gate U101D. The monitor gate then applies a logic 1 to the monitor gate line. This logic 1 enables the monitor circuits in the DCFE, and the DCFE provides serial monitor data on the monitor data input to the DCU. This monitor data is gated through serial data gate U403A to U303B where it is combined with the serial address data to form a complete monitor word. Serial data gates U403B and U403C then pass the monitor word to the monitor modulation circuits.

The logic 1 to 0 transition from U304B-Q also clocks U202A and the information at the outputs of U102B is transferred by U202A to the inputs of U202B. A logic 1 is applied to the J input of U202B and a logic 0 is applied to the K input. When the next $\overline{\text{weight 32}}$ transition from logic 1 to 0 occurs, the outputs from U202B change states and a logic 1 is applied to the input of monitor gate U101D. This logic 1 disables the monitor gate. A logic 0 is applied by U202B-Q to serial data gates U403B and U403C. This logic 0 disables the serial data gates.



TOR RESPONSE CONTROL WORD OPER FIELD ALL 0'S.

CONT WD I = 00, CONT WD II = 01, CONT WD III = 10, CONT WD IV = 11.

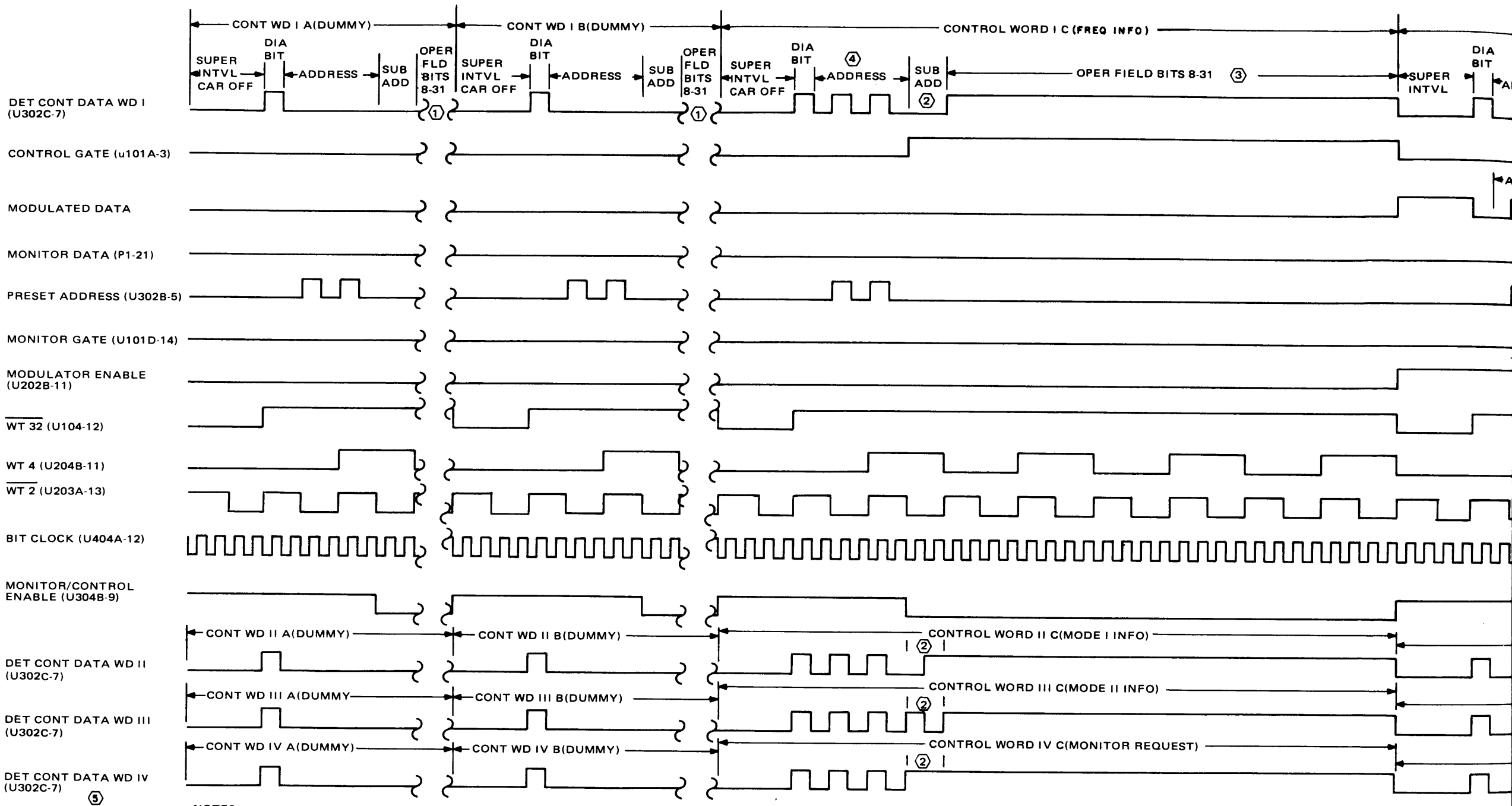
LL 1'S THIS EXAMPLE.

ET ADDRESS = 01010 THIS EXAMPLE.

OUSLY TRANSMITTED (AFTER WORDS I, II, AND III ARE ACCEPTED) TO
T STATUS.

TP2-5889-013

DCU Operation, Timing Diagram
Figure 12



NOTES:

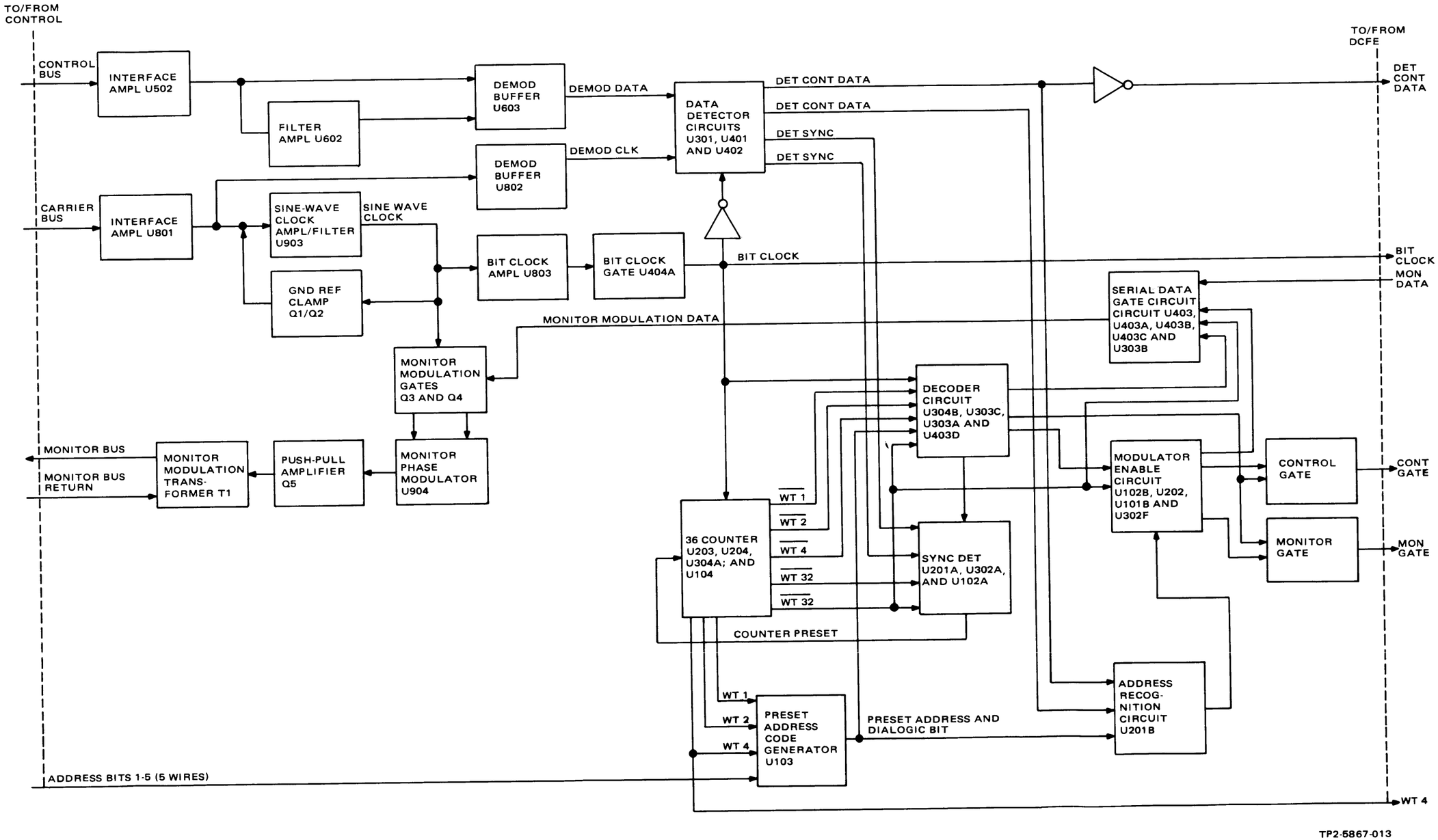
① DUMMY AND MONITOR RESPONSE CONTROL WORD OPER FIELD ALL 0'S.

② SUBADDRESS FOR CONT WD I = 00, CONT WD II = 01, CONT WD III = 10, CONT WD IV = 11.

③ OPER FIELD BITS ALL 1'S THIS EXAMPLE.

④ ADDRESS AND PRESET ADDRESS = 01010 THIS EXAMPLE.

⑤ CONT WD IV CONTINOUSLY TRANSMITTED (AFTER WORDS I, II, AND III ARE ACCEPTED) TO MONITOR EQUIPMENT STATUS.



DCU A9, Functional Diagram
Figure 13

When the weight 32 returns to logic 1, the DCU is ready to receive a new control word (or a repeat of the previous control word if the monitor response was incorrect). The DCU time base and output control circuits repeat the above sequencing each time a correctly addressed control word is received by the DCU.

4.2.15.4 Modulator Circuit

The serial monitor data from serial data gates U403B and U403C is routed through transistor gates Q3 and Q4 and is biphase modulated with the sine-wave clock by modulator amplifier U904. This biphase modulated data then passes through push-pull amplifier Q5 and is coupled through transformer T1 to the monitor bus. Table 9 in the DCFE theory lists the monitor word format.

4.2.15.5 DCU Card 624-5781-001

Refer to the schematic in the diagrams section. Functionally, this card is identical to the CPN 793-9414-001 version; however, thin-film circuits have been replaced with discrete flatpacks and components. For example, interface amplifier U502 is replaced by U61; filter amplifier U602 and demodulator buffer U603 are replaced by U51.

4.2.15.6 DCU Card 774-7842-001

Refer to the schematic in the diagrams section. Functionally the same as CPN 624-5781-001, except it operates at a much higher speed (carrier frequency). Discrete, flatpacks and components changed to accomplish high-speed operation, 76.8 kHz (bits per second).

4.2.16 TCU Card A9 (Optional)

Refer to figure 14 and to the schematic in the diagrams section. The TCU (teletypewriter converter unit) is a device that accepts standard ASCII TTY - coded control data at a 110-b/s data rate from a 514S-1 Remote Control Unit. The unit is addressable for multiunit use and control data can be either six characters of frequency data, eight characters of mode data, or characters for slewing the frequency of the receiver. Each character consists of eleven bits, a start bit, seven data bits, a parity bit, and two stop bits. The main functional elements of the TCU are the timing circuits, TTY character receiver, address control circuits, a down counter, DCFE interfacing circuits, error detector circuits, and scan control circuits.

4.2.16.1 Timing Circuits

The source of timing signals in the TCU is a free-running multivibrator containing transistors Q1 and Q2. Potentiometer R3 is adjusted for a 3521-Hz operating frequency. This master clock output is routed through pulse amplifier Q3 and inverters U103C and U103D to J-K flip-flop U112B, where it is divided by 2 to produce a 1760.5-Hz timing signal, WT1. J-K flip-flop U112A divides WT1 by 2, producing an 880.25-Hz timing signal, WT2. These three signals, master clock, WT1, and WT2, along with their complements, are distributed throughout the TCU for timing purposes.

Another main timing signal is the clock used in the TTY-character receiver portion of the TCU. This clock is enabled each time a start bit is received by the TCU. WT2F is applied through NOR gate U111D to the divide-by-8 portion of counter U101. The 110-Hz square-wave output from U101 The 110-Hz square-wave output from U101 is differentiated by C10 and R16 and routed through inverters U103A and U103F. The clock output from J103A is a short negative pulse, at a repetition rate of 100 p/s, and is used to clock the TTY-coded data bits into shift register U61.

4.2.16.2 TTY Character Receiver

TTY-coded characters are transmitted over the teletypewriter loop at 110 b/s using 20-mA mark/space signaling; that is, logic 1 is a 20-mA mark signal, and logic 0 is an absence of current or space signal. The TTY loop interface in the TCU is phototransistor U34 which conducts during mark signals and is cut off during space signals and produces an inverted output, DATAF.

Upon application of initial power to the board or the receipt of the stop bits at the end of a character, the TTY character receiver is enabled for the next character. DATAF, being a logic 0, is inverted by U103B and applied to J-K flip-flop U102A. The next time timing signal WT2 goes to logic 0, U102A is set. The T output, CHAR RCVR ENABLE (U102A-9), becomes logic 1 and removes the clear signal from shift register U61 and the reset signal from J-K flip-flop U73A. The F output (U102A-8) becomes logic 0, which enables the parity flip-flop and the divide-by-8 portions of counter U101 (paragraph 4.2.16.1).

During the start bit, DATAF becomes a logic 1. This signal is routed through U103B, U93D, and U93C and enables NOR gate U111D, which allows WT2F to be applied to the divide-by-8 portion of counter U101. DATAF is still a

logic 1 when the first clock pulse from U103A occurs, and is consequently clocked into shift register U61. This first clock also sets the F output of U73B to logic 0, which maintains the enabling of NOR gate U111D during the remaining bits of the character.

The next eight bits of the TTY character are clocked at a 110-b/s rate into shift register U61; and, simultaneously, routed through NOR gate U111A to the parity flip-flop portion of counter U101. The ninth clock pulse shifts the start bit, which has been shifted through shift register U61, into J-K flip-flop U73A. The strobe output of U73A, STB, enables NAND gate U13C, which is the parity check input to the error detection circuits. The other output of U73A, STBF, disables the divide-by-8 portion of U101 through NAND gate U93C and U111D, and prepares flip-flop U102A to be reset, through U111C, after the TTY-character has been processed. When U102A is reset, register U61 is cleared, U73A is reset, and all flip-flops in counter U101 are reset.

4.2.16.3 Address Processing

The first character to be received is the end of transmission (EOT) character. After being shifted into shift register U61, EOT is detected by the combinational logic of U71A, U83A, U81B, and U63C. The logic 0 output of U63C resets both U33A and U33B flip-flops and prepares them for the address character.

The next character to be received by the TCU is the address character. After being shifted into shift register U61, the four address bits are applied to exclusive OR gates U31A, U31B, U31C, and U31D. The other inputs to these exclusive OR gates are strapped to logic 1 or logic 0 to determine the address of the TCU. Because the address bits from U61 are inverted, the exclusive OR gates will have a logic 1 output only when the address character coincides with the strapped address. With a correct address received, the exclusive OR gate outputs are combined by NAND gates U32A and U32B, and cause NOR gate U42B to produce a logic 1 output, which is applied to the D input of flip-flop U33B. The clock signal to set U33B is produced by flip-flop U33A as STBF falls. If an incorrect address is received, U33B will not be set and will inhibit further characters from being processed. The address recognition circuit is normally disabled when a single radio is being controlled from a 514S-1 Remote Control Unit. This is accomplished by not strapping P1-26 (ALL CALL) to logic 0.

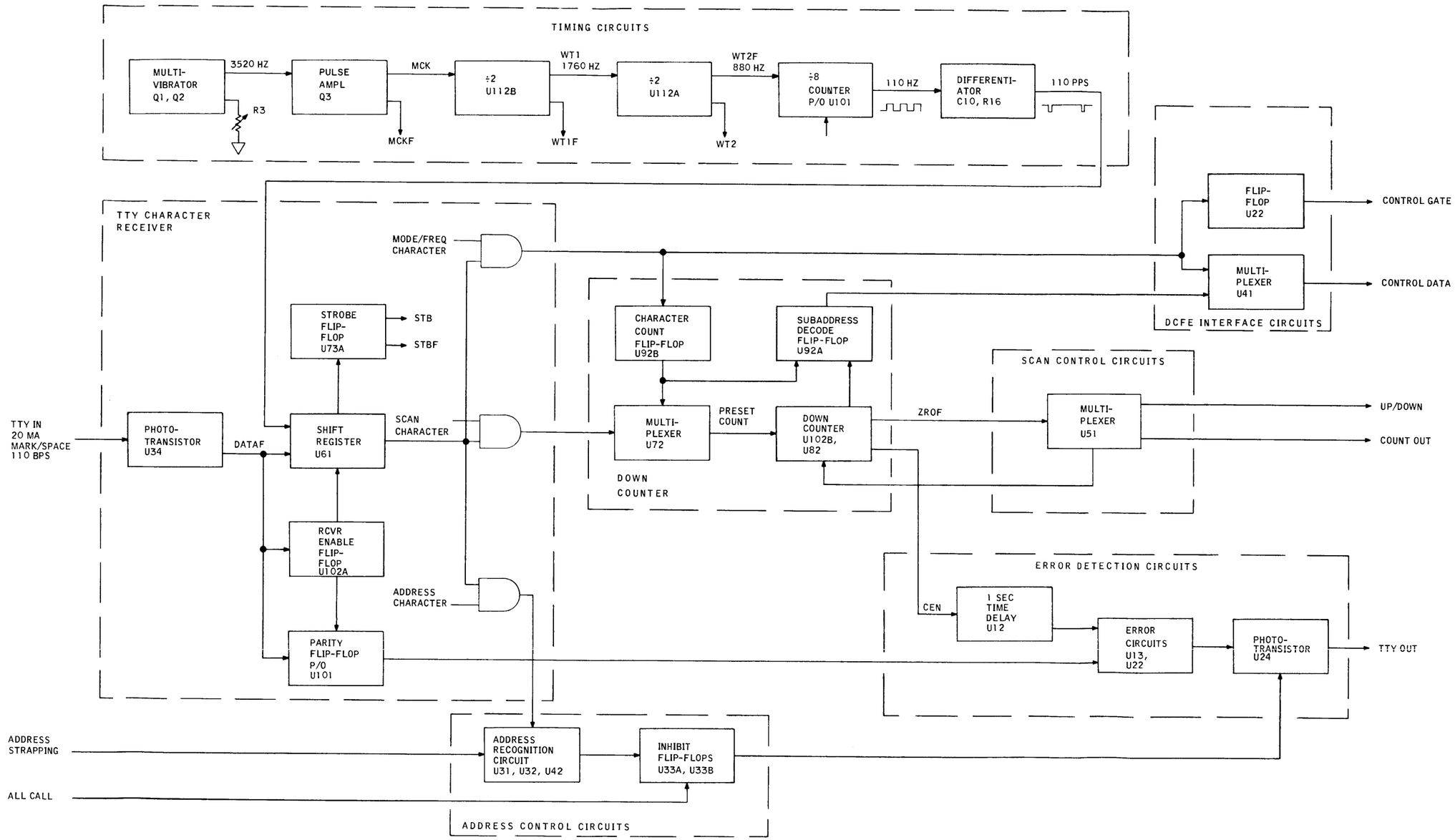
4.2.16.4 Mode and Frequency Words Processing

Mode and frequency data words are processed in almost the same manner; the main difference is that there are six characters of frequency data and eight characters of mode data.

For both types of words, a control gate and clock pulses must be applied to the DCFE. ASCII bit 7, out of shift register U61, is received as a logic 1 for these characters and is applied through NOR gate U62B and inverter U52E to NAND gate U13B. All other inputs to U13B are logic 1, which produces a logic 0 output that causes flip-flop circuit U22B and U22C to change to a state where the control gate, U22B-6, becomes logic 1. The control gate is applied to the DCFE and through U22D, which resets storage flip-flop U53B. STRF output, on U53B-12, becomes a logic 0 and disables AND gate U11D, which permits master clock MCKF to be applied through NOR gate U21B to the DCFE. Bits 5 and 7 of the first character for both words determine the subaddress used in the DCFE. Bit 7 is a logic 1 for both words to distinguish them from a scan word. Bit 5 distinguishes between a mode word (logic 0) and a frequency word (logic 1).

Bit 5 of the first mode/frequency character is used to preset counter U82 to either six (for frequency words) or eight (for mode words). Counter U82 counts each time a character is processed and determines when the appropriate number of characters for that type of word have been received. Bit 5, out of shift register U61, is applied to the D input of flip-flop U92B. If bit 5 is a logic 0, U92B remains unset; but if bit 5 is a logic 1, U92B is set. Both outputs of U92B are applied to the A inputs of multiplexer U72, and then to counter U82. Operation of counter U82 is described in paragraph 4.2.16.6.

The subaddress supplied to the DCFE is determined by the ASCII character received and how the character is processed by the subaddress decode circuit. The subaddress decode circuit consists of flip-flop U92A; NOR gates U81A, U81C, and U81D; NAND gates U91A and U91C; and inverter U52B. For frequency words, the



TP3-1436-014

TCU A9, Functional Diagram
Figure 14

subaddress is 00. For mode words, the subaddress is 10 for the first two characters, and 01 for the last six characters. The subaddress bits are applied to multiplexer U41 from inverter U52B and NAND gate U91C. These address bits are inverted and transferred to the DCFE by timing signals WT1 and WT2 during the period when the C input (U41-9) is a logic 0. After the subaddress has been shifted into DCFE, the first digit of mode/frequency data is shifted while the C input (U41-9) is a logic 1. Bits 1 through 4 contain the digit in the format (B1-B4) listed in tables 10 and 11. Subsequent characters are received and processed in a similar manner by the TCU.

Table 10. Control Data Format for Frequency Data.

ASCII BIT POSITION	CHARACTER 1	CHARACTER 2	CHARACTER 3	CHARACTER 4	CHARACTER 5	CHARACTER 6
B1	2^0 ┐ 10 MHz	2^0 ┐	2^0 ┐	2^0 ┐	2^0 ┐	2^0 ┐
B2	2^1 ┘	2^1	2^1	2^1	2^1	2^1
B3	0	2^2 1 MHz	2^2 100 kHz	2^2 10 kHz	2^2 1 kHz	2^2 100 Hz
B4	0	2^3 ┘	2^3 ┘	2^3 ┘	2^3 ┘	2^3 ┘
B5	1	1	1	1	1	1
B6	1	1	1	1	1	1
B7	0	0	0	0	0	0

1 = MARK SIGNAL
0 = SPACE SIGNAL

Table 11. Control Data Format for Mode Data.

ASCII BIT POSITION	CHARACTER 1	CHARACTER 2	CHARACTER 3	CHARACTER 4	CHARACTER 5	CHARACTER 6	CHARACTER 7	CHARACTER 8
B1	2^0 ┐	2^0 ┐	AM	VBFO	200 Hz	450 kHz BYPASS	10.35 MHz BYPASS	X
B2	2^1 VBFO	2^1 RF GAIN	NBFM	BFO	AGC SLOW	6 kHz	3 kHz	LOCAL
B3	2^2	2^2	0	ISB	0	LSB	1 kHz	OPERATE
B4	2^3 ┘	2^3 ┘	0	SSB/CW	INTER-POLATE	USB	500 Hz	AGC OFF
B5	0	0	0	0	0	0	0	0
B6	1	1	1	1	1	1	1	1
B7	0	0	0	0	0	0	0	0

1 = MARK SIGNAL
0 = SPACE SIGNAL

Thus, the control words specified in table 7 are transferred from the TCU to the DCFE in the following manner. For a frequency word, the first character processed contains data in bit positions 6 through 11 of control word I; the second character covers bits 12 through 15; the third covers 16 through 19; etc. For a mode word, the first character processed contains data in bit positions 6, 7, and 24 through 27 of control word III; the second character covers bits 28 through 31; the third covers bits 6 through 11 of control word II; the fourth covers bits 12 through 15; the fifth covers 16 through 19; etc.

4.2.16.5 Scan Word Processing

A scan word can be one character or a string of characters; with each character representing a number from 1 to 31. Scan characters will be received continuously as long as the 514S-1 manual tuning control is rotated.

The seven data bits of each scan character are identified in table 12. Bits 1 through 5 contain the number of scan pulses, up to a maximum of 31 pulses, that are required to slew the 651S-1 to the desired frequency. Each pulse represents a frequency change of 100 Hz. Bit 6 identifies whether the frequency should be slewed up or down. Bit 7 identifies a scan character and not a mode/frequency character.

Bits 1 through 5, from shift register U61, are applied to a 5-bit counter consisting of J-K flip-flop U102B and counter U82. Bit 1 is applied to U102B through NAND gate U43B and inverter U52D. Bits 2 through 5 are routed through multiplexer U72 and applied to counter U82. Detail operation of counter U82 is described in paragraph 4.2.16.6.

Multiplexer U51 has multiple applications: a scan control portion and a portion used with counter U82. In general, the input applied to S0 (U51-9) controls its operation. When S0 is a logic 0, the B0 through B3 inputs appear on the F0 through F3 outputs. When S0 is a logic 1, the A0 through A3 inputs appear inverted on the F0 through F3 outputs.

In the scan mode, bit 7 is a logic 1 and is applied to S0 input of multiplexer U51; thus enabling the A inputs. Timing signal WT1F is applied through NOR gate U42C to A2 input of U51. The inverted timing signal appearing at

Table 12. Control Data Format for Slew Control Data.

ASCII BIT POSITION	SLEW DOWN	SLEW UP
B1	2^0 ┐	2^0 ┐
B2	2^1 │	2^1 │
B3	2^2 COUNTDOWN VALUE	2^2 COUNT UP VALUE
B4	2^3 │	2^3 │
B5	2^4 ┘	2^4 ┘
B6	1	0
B7	1	1

1 = MARK SIGNAL
0 = SPACE SIGNAL

F2 output advances counter U82, and is routed back to the A0 input of U51. The inverted output, F0 on U51-3, is the count out signal used to slew the 651S-1. Bit 6, which determines slew up or slew down, is routed from shift register U61 through inverter U52C to the A1 input of U51. Both the up/down out signal at F1 (U51-4) and the count out signal are applied to frequency control card A14. When all the slew pulses have been processed, as determined by counter U82, the scan operation is complete.

4.2.16.6 Down Counter Operation

The down counter is a 5-bit counter that consists of J-K flip-flop U102B, counter U82, and various combinational logic elements. The down counter has two purposes: first, to count the number of characters received for mode/frequency words; and secondly, to count the number of slew pulses received in a scan word.

In a quiescent state, down counter contains a 1 in all five flip-flops (U102B, and four in U82). The five outputs are combined in NAND gate U71B, which causes ZROF (U71B-8) to be a logic 0. ZROF is inverted by U103 and applied to NOR gate U83C. The logic 0 from U83C is applied to the J-K inputs of U102B and inhibit any further counting.

Counter U82 is preset to other counts by multiplexer U72, which has two different applications. In general, the input applied to S0

(U72-9) controls its operation. When S0 is a logic 0, the B0 through B3 inputs appear on the F0 through F3 outputs. When S0 is a logic 1, the A0 through A3 inputs appear inverted on the F0 through F3 outputs. S0 is a logic 0 during scan characters, and permits the number of scan pulses stored in shift register U61 to be transferred to counter U82. During mode/frequency words, S0 is a logic 1 and permits the number of characters to be received (6 for frequency, 8 for mode) to be transferred from flip-flop U92B to counter U82.

The output of counter U82 and U102 is always the 1's complement of the number desired. For example, if a count of 8 (01000) is desired, its 1's complement, 23 (10111), is set into counter U82 and U102. Then, when the counter had advanced 8 counts to 31, the counter reaches its quiescent state.

The 1's complement of the desired count is determined by multiplexer U72 and U102, with the output of U72 being transferred to counter U82 by load signal LODF from a flip-flop circuit consisting of U63B and U63C. This load signal is produced by strobe signal STB at the end of the first mode/frequency/scan character.

With the counter preset, its counting action is now enabled through NAND gate U71B, inverter U103, and NOR gate U83C. Additionally, logic gates U81A, U91A, and U91D set flip-flop U92A to enable the subaddress decode circuit if a mode/frequency word is received. The output from U92A is routed through both NOR gates U81C and U81D to NOR gate U83C, which maintains the counter enable.

Once the counter has been preset and enabled, the counter can be advanced to its quiescent state by clocking flip-flop U102B, through NAND gate U93B, in one of three ways. The fastest clocking occurs when an error has been detected; then 3521-Hz MCK signal is routed through NAND gate U93A to U93B. The second fastest way is during a scan character; then 1760.5-Hz WT1F is routed through NOR gate U42C and multiplexer U51 to U93B. The slowest clocking of counter U82 occurs during mode/frequency word processing. During this time, the strobe signal STB, at the rate of 10 Hz, is routed through NOR gates U62A and U21A, NAND gate U63A, and multiplexer U51 to U93B.

4.2.16.7 Error Detection Circuit

Two types of errors can be detected: parity and word execution time. NAND gate U13C checks for odd parity during strobe signal STB; and delay AND gate U12A checks for mode/frequency word completion within 1 second. If either fault occurs, flip-flop circuit U22A and U13B is set so that phototransistor U24 is cut off; thus producing a space or error (no current) condition on the teletypewriter loop. The no-fault condition is maintained when the TCU has not been addressed in the all-call mode.

4.2.17 Auto Scan Card A9 (Optional)

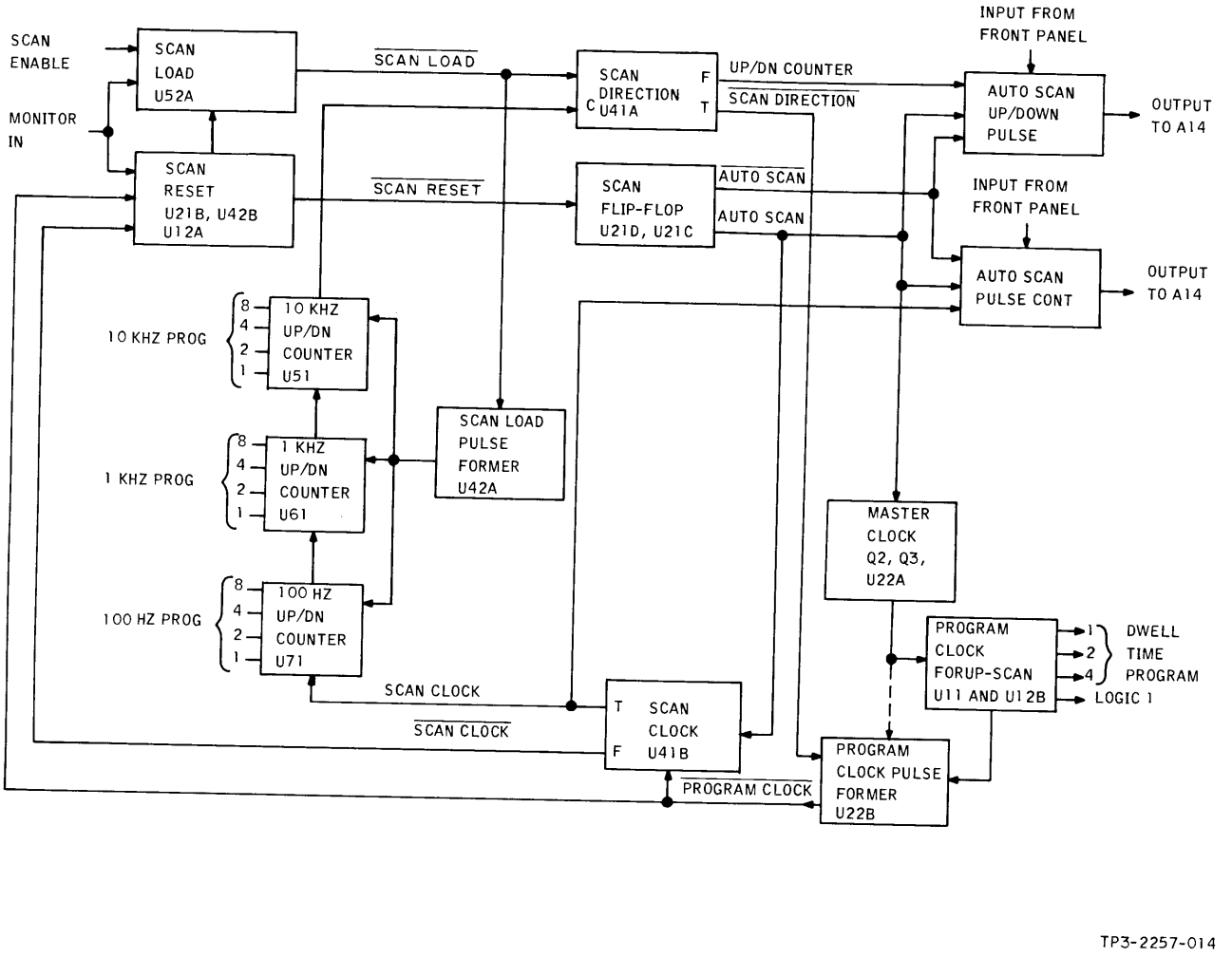
Refer to figure 15 and the schematic in the diagrams section. Auto scan card A9 receives frequency information from the front panel frequency controls and converts it into frequency scan data and applies this data to frequency control card A14. The two outputs are a frequency-count pulse (clock pulse) and a scan-up (logic 1) or scan-down (logic 0) signal.

4.2.17.1 Timing Signals (Figure 16)

The source of timing signals in the auto scan card is an RC controlled master clock consisting of Q2, Q3, and their associated components. A logic 0 input (scan-up operation) is inverted by U62E and applied to the base of Q2. When Q2 is enabled, C4 is added to the master clock RC network and the clock output pulse rate decreases. The master clock pulse is divided (countdown) by U11, the division ratio is determined by the dwell-time programmed into U11. The output of U11 is the program clock signal. The program clock pulses are divided (by 2) by JK flip-flop U41B to produce the scan clock signal.

4.2.17.2 Scan-up Operation

An enable signal (logic 1) from the REMOTE/LOCAL switch on the front panel enables Q1. The logic 0 on the collector of Q1 is routed through inverters U62B and U62C to JK flip-flop U52A. The F-output (pin 4) of U52A goes to logic 0 and is applied back to K (pin 6) to reset U52A. However, the short logic 0 trigger is applied to the R-input (pin 12) of U41A and also through pulse former U42A to reset up/down counters U51, U61, and U71 to their programmed initial state.

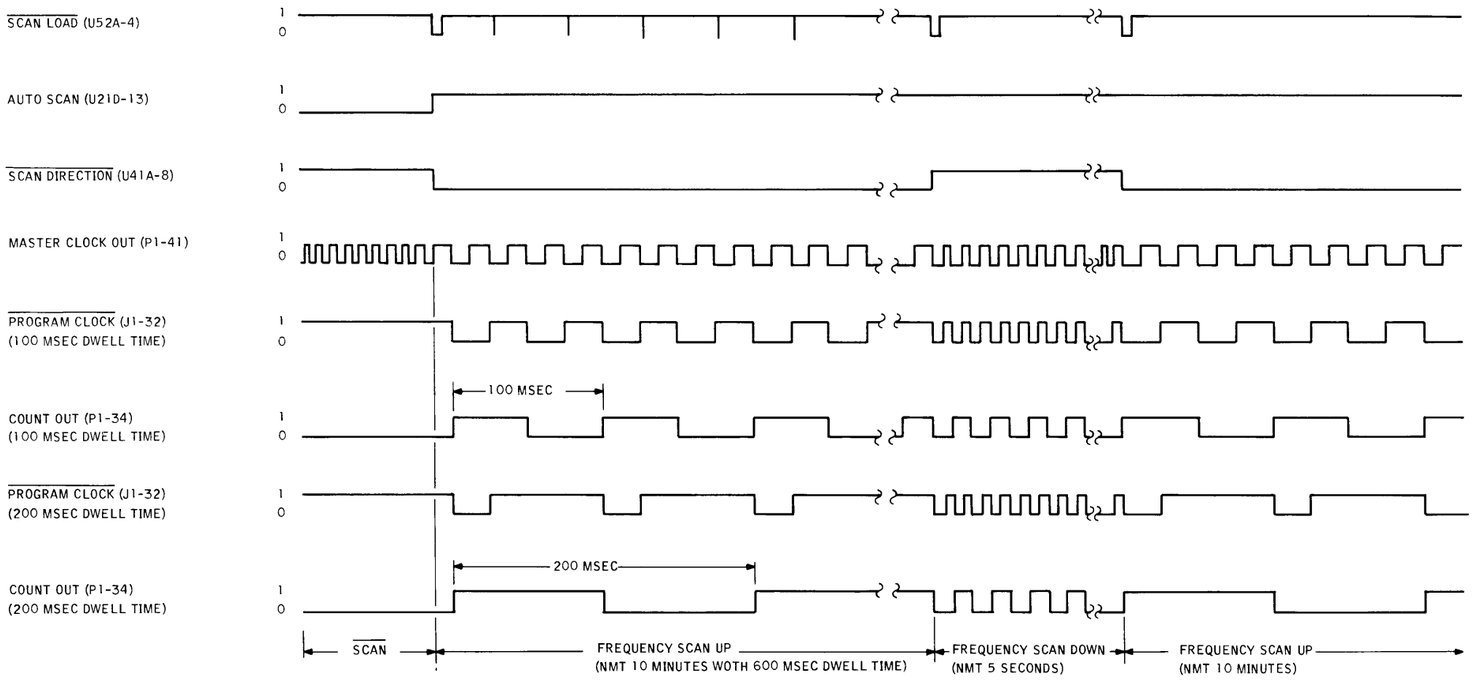


Auto Scan Control Card A9, Functional Diagram
Figure 15

The F-output of U41A (logic 1) is applied to the input of U31D in the auto scan circuit; the T-output (logic 0) is inverted by U62E and applied to the master clock circuit. The output of the master clock is inverted by U62D routed through pulse former U22A and applied to the program clock circuit U11 and U12B. The output of U12B (program clock) is routed through pulse former U22B and applied to the scan clock flip-flop U41B; simultaneously it is applied to U12A in the scan reset circuit.

The auto scan flip-flop U21D and U21C receives enabling signals (logic 1) from U12A and U24B (scan reset). The auto scan signal (logic 1) from U21D-13 is applied to U41B (scan clock) and to U31D and U32C in the auto scan circuit. The $\overline{\text{auto scan}}$ signal (logic 0) from U21C-10 is applied to U31C and U31B in the auto scan circuit.

The T-output (scan clock) of U41B triggers the frequency up/down counter U71 and is simultaneously



TP3-2256-014

Auto Scan Control Card A9, Timing Diagram
Figure 16

applied to U32C in the auto scan circuit; the F-output (scan clock) is applied to U21B in the scan reset circuit.

During scan-up operation (maximum of 10 minutes), the scan direction output (P1-31) will remain a logic 1; the frequency count output (P1-34) will be a clock pulse with the pulse rate determined by the scan clock which in turn is determined by the dwell time programmed into U11. This condition remains until up/down counters U71, U61, and U51 count up through the programmed frequency scan range. At the upper frequency limit, U51-12 applies a logic 1 to scan direction flip-flop U41A. This will cause U41A to reverse outputs and start the scan-down sequence.

4.2.17.3 Scan-Down Operation

A logic 1 from U51-12 causes U41A to reverse outputs, the F-output (logic 0) is routed through U31D and U31A to P1-31. A logic 0 output will cause frequency control card A14 to start scanning down in frequency. The T-output (logic 1) of U41A is inverted through U62E and applied as a disabling signal to Q2. With Q2 disabled, C4 is removed from the RC network of the master clock; shorter RC time will increase the master clock output pulse rate. Simultaneously the scan direction signal (logic 0) is applied to the input of U21A. The output of the master clock is routed through U62D and U22A and applied to the input of U21A. U21A is enabled bypassing dwell-time program clock U11 and U12B. The clock output of U22B will be the same pulse rate as the master clock.

The program clock signal is applied to U12A and in turn resets the scan-load flip-flop U52A, applying the scan-load trigger (logic 0) through U42A to reset the frequency up/down counters U51, U61, and U71 to their initial state. The F-output of U41B (scan clock) enables the scan-reset circuit (U21B and U42B) that in turn resets the auto scan flip-flop (U21D and U21C). Simultaneously, the T-output (scan clock) of U41B will start U71, U61, and U51 counting down. However, the scan down rate will be much faster than the scan-up rate. When the lower frequency limit is reached, a logic signal from U51-12 will cause U41A to reserve and the up-scan cycle will be repeated.

During scan-down operation (maximum of 5 seconds), the scan direction output (P1-31) will remain a logic 0; the frequency count output (P1-34) will be a clock pulse. However, the pulse rate will be much faster than in the scan-up sequence.

5. DIFFERENCE DATA

5.1 Configurations of 651S-1/1A

The following list explains the unique features of each configuration of the 651S-1/1A by part number identifier. Refer to table 1 for the complement of cards included in each.

5.1.1 651S-1

a. 522-4836-004: features local control; standard operating modes of FM, AM, SSB, and CW; bandwidths of 370 (offset 2 kHz) and 500 Hz, and 1.1 (offset 2 kHz), 2.7, 3, 6, and 16 kHz; has audio squelch.
b. 522-4836-102: features local control; standard operating modes of FM, AM, SSB, and CW; and bandwidths of 500 Hz and 2.7, 6, and 16 kHz.
c. 522-4836-103: features Collins 3-pair serial digital remote control, and standard operating modes and bandwidths listed in step b.
d. 522-4836-104: features local control; standard operating modes and bandwidths listed in step b, plus 370-Hz (offset 2 kHz) (narrow shift radioteletypewriter, NSRT) and 1.1-kHz (offset 2 kHz) (wide shift radioteletypewriter, WSRT) bandwidths.
e. 522-4836-106: features local control; standard operating modes and bandwidths listed in step b; plus independent sideband (ISB).
f. 522-4836-107: features Collins 3-pair serial digital remote control; standard operating modes and bandwidths listed in step b; ISB; and bandwidths of 0.2, 1.0, and 3.0 kHz.
g. 522-4836-108: features Collins 3-pair serial digital remote control; standard operating modes and bandwidths listed in step b; and bandwidths of 0.2, 1.0, and 3.0 kHz.
h. 522-4836-110: features local control; standard operating modes and bandwidths listed in step b; ISB; and bandwidths of 0.2, 1.0, and 3.0 kHz.
i. 522-4836-111: features local control; standard operating modes and bandwidths listed in step b; and bandwidths of 0.2, 1.0, and 3.0 kHz.

j. 522-4836-113: features Collins 3-pair serial digital remote control and standard operating modes and bandwidths listed in step b; bandwidths of 0.2, 1.0, and 3.0 kHz; and a special modification for fast external rf gain.
k. 522-4836-120: features local control, standard operating modes and bandwidths listed in step b; has vlf converter.
l. 522-4836-121: features local control; standard operating modes and bandwidths listed in step b; bandwidths of 0.2, 1.0, and 3.0 kHz; has audio squelch.
m. 522-4836-122: features local control; standard operating modes and bandwidths listed in step b; ISB; bandwidths of 0.2, 1.0, and 3.0 kHz; has audio squelch.
n. 522-4836-123: features remote teletypewriter coded control and standard operating modes and bandwidths listed in step b.
o. 522-4836-124: features local control; standard operating modes and bandwidths listed in step b; has audio squelch.
p. 522-4836-125: features Collins 3-pair serial digital remote control; standard operating modes and bandwidths listed in step b; has audio squelch.
q. 522-4826-126: features local control; standard operating modes and bandwidths; has a special gray front panel.
r. 522-4836-128: features Collins 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 1.1, 2, 2.7, 3, 4, 6, and 16 kHz.
s. 522-4836-129: features Collins 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 500 Hz and 1.1, 2.7, 3, 6, and 16 Hz.
t. 522-4836-131: features 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz and 1, 2.7, 3, 6, and 16 kHz plus ISB; has audio squelch.
u. 522-4836-132: features local control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz, and 1, 2.7, 3, 6, and 16 kHz; and vlf converter.
v. 522-4836-133: features local control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz, and 1, 2.7, 3, 6, and 16 kHz plus ISB; has vlf converter.
w. 522-4836-134: features local control; standard operating modes listed in step b; bandwidth of 370 Hz (offset +2 kHz) (narrow shift radioteletypewriter, NSRT) 500 Hz, 1.1 kHz, (offset +2 kHz) (wide shift radioteletypewriter, WSRT) and 2.7, 3, 6, and 16 kHz.
x. 522-4836-135: features 3-pair serial digital remote control; standard operating modes listed in step b; bandwidths of 200 Hz, 500 Hz and 1, 2.7, 3, 6, and 16 kHz plus ISB; has vlf converter and audio squelch.
y. 522-4836-152: features local control; standard operating modes AM, SSB, and CW; bandwidths of 2.7, 6, and 16 kHz.
z. 522-4836-153: functionally identical to part no -152, except has DCFE and DCU cards for remote control.
aa. 522-4836-154: features local control standard operating modes listed in step y; bandwidths of 320 Hz (NSRT) (offset +2 kHz), 500 Hz, 1.1 kHz (WSRT), (offset +2 kHz), and 2.7, 3, 6, and 16 kHz.
ab. 522-4836-156: functionally identical to part no -152, except has ISB card for ISB operation.
ac. 522-4836-173: functionally identical to part no -152, except has audio squelch.
ad. 522-4836-179: functionally identical to part no -153, except has a hi-speed DCU card (76.8 kHz).
ae. 522-4836-180: features local control; standard operating modes listed in step y; bandwidths of 500 Hz, 1.1 kHz (offset +2.55 kHz, WBTY), and 2.7, 3, 6, and 16 kHz.
af. 522-4836-181: functionally identical to part no -180, except has ISB card added.
ag. 522-4836-182: functionally identical to part no -180 except has vlf converter added.
ah. 522-4836-183: features Collins 3-pair serial digital remote control; standard operating modes listed in step y plus FM; bandwidths of 200 Hz, 500 Hz, and 1, 2.7, 3, 6, and 16 kHz; has FM detector, keep alive voltage, preselector control, and fast rf gain control.
ai. 522-4836-184: features Collins 3-pair serial digital remote control; standard operating modes listed in step y; bandwidths of 1.1 kHz (offset +2 kHz) and 2, 2.7, 3, 4, 6, and 16 kHz; has VBFO of 455.5 kHz and fast gain control.

5.1.2 651S-1A

622-1062-001: features local control; standard operating modes of AM, SSB, and CW; bandwidths of 370 Hz (narrow shift radioteletypewriter, NSRT), 500 Hz, 1.1 kHz (wide shift radioteletypewriter, WSRT), and 2.7, 3, 6, and 16 kHz; has audio squelch.

5.2 Card Configurations

The following list explains the unique features of the various cards, identified by part number.

a. A2, 778-2948-003 (old version): 600-ohm center tapped, 8-ohm speaker and 600-ohm headphone outputs; vbfo circuits that produce bfo variations in SSB of ±60 Hz in 10-Hz steps, and in CW of ±900 Hz.
b. A2, 778-2948-003 (current production model): functionally same as old version except operational amplifier U2, T1, and T2 in vbfo replaced with transistor Q6 and associated components.
c. A2, 778-2948-002: same as part no -003 old version, except with squelch operating an audio signal-to-noise ratio.
d. A2, 778-2948-004: same as part no -003 current production model, except with squelch operating on audio signal-to-noise ratio.
e. A2, 778-2948-005: same as part no -003 current production model, except Y1 is changed to 4.4555 MHz.
f. A4, 778-2951-001: standard if amplifier card with FM.
g. A4, 778-2951-003: same as part no -001, except with special modification for fast external rf gain.
h. A4, 778-2951-004: same as part no -001, except no FM.
i. A5A1, 797-3571-001, -006, -007, -010, -016, -012: only difference between each status is the bandwidth filters, see schematic in the diagrams section.
j. A5A2, 797-3585-002, -003, -004, -010, -011, -012: only difference between each status is the bandwidth filters, see schematic in the diagrams section.
k. A6, 790-1048-010, -021: the -010 differs from standard rf module A6 part no -008, and -021 differs from standard rf module part no -020 by providing a vlf up-converter for frequencies less than 560 kHz.
l. A6, 790-1048-008, -020: standard rf modules functionally the same, part no -020 is the current production model.
m. A7, 778-2928-003: standard 10-band decoder/driver card.
n. A7, 608-9087-001: standard 3-band decoder/driver card replaces the 778-2928-003 card.
o. A7, 608-9121-001: same as 608-9087-001, except has bcd outputs used with a 635U-2 external preselector.
p. A9, (DCU) 793-9414-001/624-5781-001/774-7342-001: functionally the same with discrete flatpacks on 624-5781-001 and 774-7843-001 replacing thin-film circuits on 793-9414-001. The 774-7843-001 is a hi-speed version (76.8 kHz/bits per second).
q. A10, 793-9334-001, -002: standard synthesizer divides cards functionally the same, with discrete flatpacks on part no -002 replacing thin-film circuits on part no -001.
r. A10, 793-9334-006: differs from standard synthesizer divider card part no -002 by providing injection frequencies 9.9 MHz above the incoming signals, for vlf operation below 560 kHz.
s. A11, 793-9333-001, -002: standard synthesizer reference cards functionally the same, with discrete flatpacks on part no -002 replacing thin-film circuits on part no -001.
t. A12, 793-9332-001, -002: standard synthesizer mixer cards functionally the same, with discrete flatpacks on part no -002 replacing thin-film circuits on part no -001.
u. A13, 793-9331-002, -003: standard synthesizer vco cards functionally the same, with discrete flatpacks on part no -003 replacing thin-film circuits on part no -002.

651S-1/1A General Purpose HF Receiver

installation

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NOTICE: This section replaces second edition dated 1 May 1972.

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[illegible]	15 Oct 72
*17	15 Oct 72
*18 Blank	15 Oct 72

Record of Revisions

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ON RECEIPT OF REVISIONS, INSERT REVISED PAGES IN THE MANUAL
AND ENTER DATE INSERTED AND INITIAL.

ASSIGNED TO (108 TITLE)

LOCATION

REV. NO.	REVISION DATE	INSERTION DATE	BY	REV. NO.	REVISION DATE	INSERTION DATE	BY
1st Ed	1 Oct 71						
2nd Ed	1 May 72						
1	1 Jul 72						
3rd Ed	15 Oct 72						

installation

1. UNPACKING AND PACKING

1.1 Unpacking

Carefully remove the 651S-1/1A from the packing material. If feasible, save the original carton and packing material for possible reshipment. Examine the unit for visible damage and check that all controls and switches operate freely. If the receiver has been damaged in shipment, notify the transportation company. Check each item received against the shipping invoice. Be sure the warranty card is included with the receiver.

1.2 Storage

Store the 651S-1/1A in the original carton and packing material, if available. Brace and pad the unit as in the original shipment. Include a dehydrating agent in the packing material to prevent damage from condensation. Be sure to store the unit in an environment that does not exceed the equipment specifications listed in the description and principles of operation section of this instruction book.

1.3 Preparation For Reshipment

Carefully pack the 651S-1/1A in the original carton and packing material, if available. Brace and pad the unit as in the original shipment. Include a dehydrating agent in the packing material to prevent damage from condensation.

2. MOUNTING (699J-1 SPEAKER PANEL)

The 651S-1/1A can be table-top installed or rack mounted in the 699J-1 Speaker Panel. Figure 1 shows outline and mounting dimensions for the 651S-1/1A and figure 3 shows the same for the 699J-1. Mount the receiver in the 699J-1 Speaker Panel as follows:

a. Remove the two feet and dust cover clips from the bottom front of the receiver. Refer to figure 2, detail C. Retain feet, clips, and hardware for future table-top installation if desired.
b. Remove the two bumper pads from the bottom rear corners of the receiver dust cover. Refer to figure 2, detail B. Retain the pads for future table-top installation if desired.
c. Remove the two screws that secure the dust cover. Do not remove the dust cover.
d. Slide the receiver through the speaker panel hole from the rear. Slide the receiver forward until it touches the speaker panel at point B in figure 2. When sliding the receiver, lift the rear slightly above horizontal to clear the rubber pad (point C, figure 2).
e. When the receiver is completely forward, lower it into place and secure it to the speaker panel using the hardware supplied (items 1 and 2, figure 2). Insert the tips of the bosses (part of item 1, figure 2) into the holes (point A, figure 2) that the dust cover mounting screws were removed from.
f. Connect the pendant cable from the speaker to the SPKR 8 OHM jack on the rear panel of the receiver.
g. Mount the completed assembly in a standard 19-inch rack.

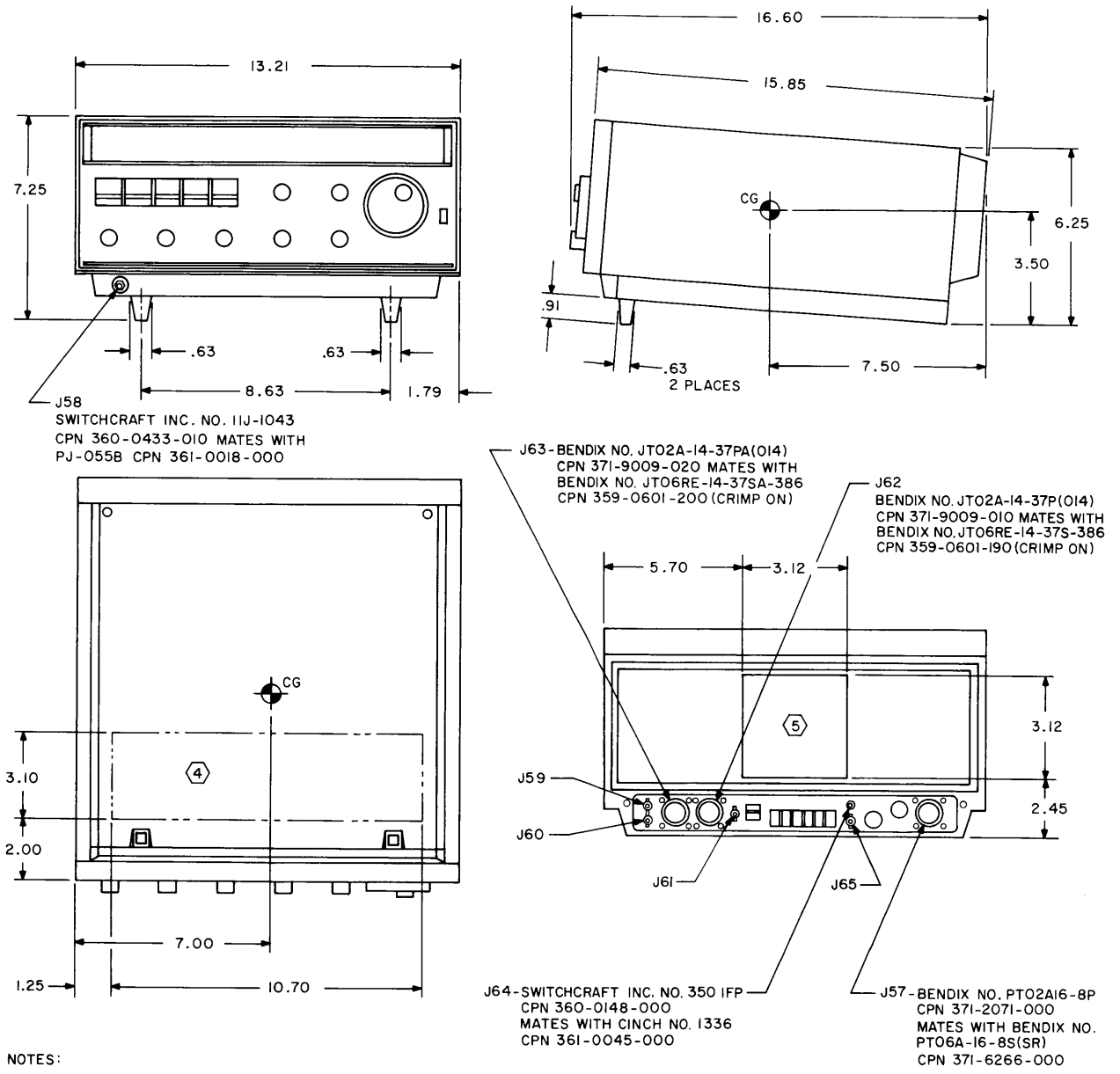
3. CABLING

Connect the 651S-1/1A Receiver as shown in figure 5.

3.1 Power Cable and Fuses

The 651S-1/1A is supplied with 1.5-ampere fuses for 115-volt operation. Replace with 0.75-ampere fuses for 230-volt operation.

Two power cables are available for the 651S-1/1A: 115-volt cable Collins part number 609-0507-001, and 230-volt cable Collins part number 618-3339-001. Connect the desired power cable to multipin PWR connector J57 on the rear panel of the receiver. Plug the power cable into an ac outlet. If the outlet does not have a mating receptacle for the power cable, use a power cable adapter and ground the green wire of the adapter.

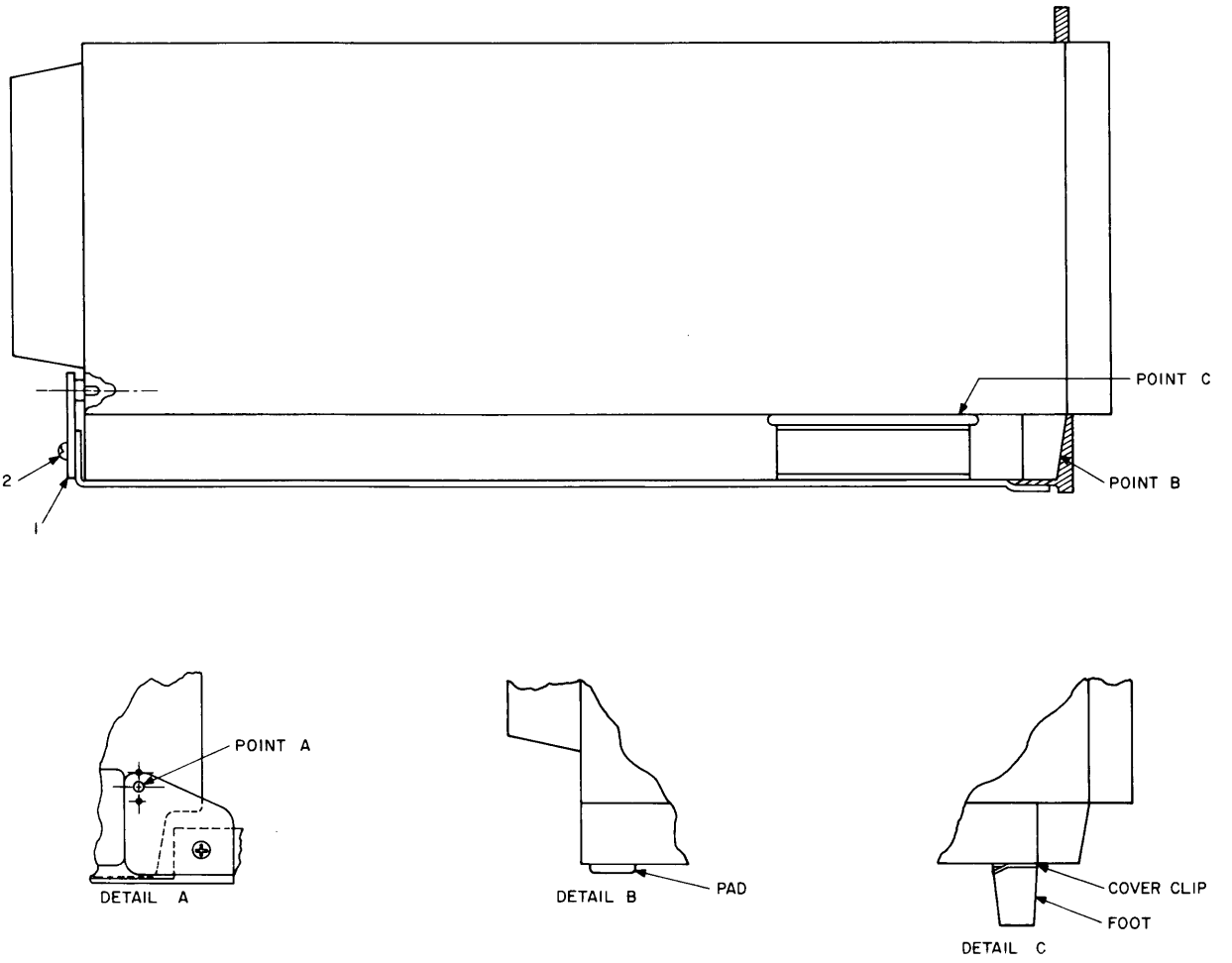


NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. THIS DRAWING APPLIES TO ALL 651S-1 (CPN 522-4836-XXX)
3. UNIT WEIGHT IS APPROXIMATELY 30 LBS.
4. AIR INLET AREA, MUST BE UNOBSTRUCTED.
5. AIR DISCHARGE AREA, MUST BE UNOBSTRUCTED.

TP2-7212-014

651S-1/1A Outline and Mounting Dimensions
Figure 1



651S-1/1A Mounting in 699J-1 Speaker Panel, Installation Details
Figure 2

Caution

Be sure to use 1.5-ampere fuses for 115-volt operation and 0.75-ampere fuses for 230-volt operation.

3.2 Audio Outputs

An 8-ohm speaker may be connected to the SPKR 8 OHM jack (J64) on the rear panel of the receiver. A phone-type plug on the speaker leads is required. ISB and standard audio (both 600 ohms, center tapped) are also available at the AUDIO LINES terminal strip (TB101) on the rear panel of the receiver, if desired.

High-impedance headphones, having a phone-type plug, may be plugged into the phone jack (J58) on the front panel of the receiver. Plugging in headphones automatically disables the output from the SPKR 8 OHM jack on the rear panel. The 600-ohm, center-tapped ISB and standard audio outputs are not disabled by plugging headphones into the front-panel phone jack.

3.3 Antenna

Connect an antenna to the 50-ohm BNC coaxial connector (J61) on the rear panel of the receiver.

Note

If the receiver is to be operated primarily below 150-kHz, better sensitivity will probably be obtained by changing to the 1000-ohm input impedance tap on the input of the vlf converter in rf module A6 (paragraph 4.5).

3.4 External Battery (For 651S-1/1A With Optional Keep-Alive Circuit).

An external 6-volt battery may be connected to the BATT-6V terminal block (TB106) on the rear panel of the receiver. If an external battery is used, the operating frequency will be retained in storage and not have to be reselected in the event of a momentary line power interruption. However, if operating power is turned off by the front panel POWER switch, the frequency must be reselected, even through an external battery is used.

3.5 Remote Control Interconnect

3.5.1 Processor Version

For remote control operation, connect a serial digital line processor unit to the multipin REMOTE CONTROL INPUT connector (J62) on the rear panel of the receiver. Refer to the chassis schematic in the diagrams section for pin function information. The connector of the rear panel is a type JT02A-14-37P(014), and the mating connector is a type JT06RE-14-37S-386. The three pairs of control, carrier, and monitor function wires in the interconnecting cable should be shielded twisted pairs (typically type 407L). The cable length should not exceed 1,000 feet. Refer to the operation section for address strapping information.

If using Collins 8311A-1 or 8311B-1 processors, three 90-ohm resistors must be added to the interface. At the processor end, connect one resistor between the monitor and monitor return lines. At the 651S-1/1A end, connect one resistor between the control and control return lines, and one between the carrier and carrier return lines. If more than one receiver is being controlled, connect them all in parallel with respect to the control information from the processor, and connect resistors across the control and carrier lines to the last receiver in the group. Only three resistors are necessary no matter how many receivers are being controlled by the processor. Refer to the operation section for remote control operating procedures.

3.5.2 Teletypewriter Signal Version (514S-1 Remote Control Unit)

Note

Refer to paragraph 4.7 for 651S-1/1A strapping and to the 514S-1 instruction book, Collins part number 523-0764187, for 514S-1 strapping.

For remote control operation, connect a 514S-1 Remote Control Unit to the multipin REMOTE CONTROL INPUT connector (J62) on the rear panel of the receiver. A typical 514S-1/651S-1/1A interconnect diagram is shown in figure 4. Refer to the chassis schematic in the diagrams section for pin function information. The connector of the rear panel is a type JT02A-14-37P(014), and the mating connector is a type JT06RE-14-37S-386. The two pairs of TTY receive and transmit wires in the interconnecting cable should be the standard 20-mA TTY loop, and the cable length should not exceed 1,000 feet.

Note

A single pair of standard 20-mA teletypewriter wires may be used by jumpering pin 5 to pin 1 on connector J62 of the 651S-1/1A and jumpering pin 2 to pin 4 on connector J62 of the 514S-1.

Refer to the operation section for address strapping information and remote control operating procedures.

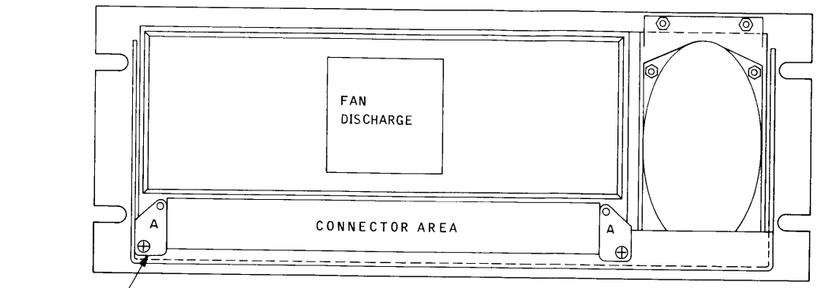
4. SUPPLEMENTARY INSTALLATION DATA

4.1 IF Outputs

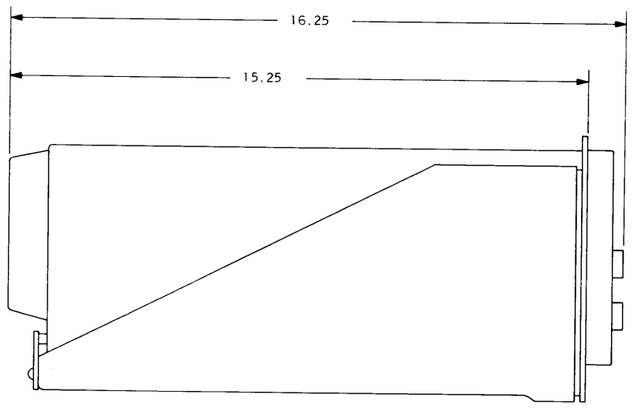
The 651S-1/1A contains a standard if output jack (J59) and an ISB if output jack (J60) on the rear panel. These 450-kHz, 50-ohm BNC coaxial outputs may be connected to any RTTY converter, an oscilloscope, or any other device requiring a 450-kHz signal. The if outputs may be used to monitor the standard and ISB if signals.

NOTES:

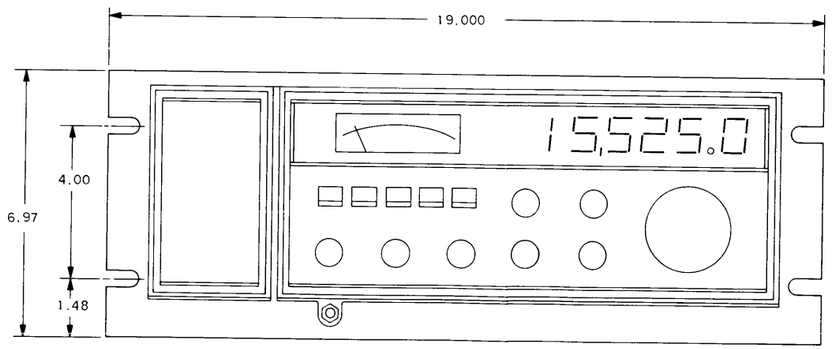
1. DIMENSIONS ARE IN INCHES.
2. UNLESS OTHERWISE SPECIFIED - TOLERANCES ON:
   DECIMAL DIMENSIONS - .XX = ± .02, .XXX = ± .008
   HOLE DIAMETERS - UNDER .251 DIA = + .005 - .005
   .251 TO .500 DIA = + .006 - .005
   OVER .500 DIA = + .008 - .005
   ANGLES = ± 1.0°
3. ECCENTRICITY BETWEEN DIAMETER ON AN AXIS NOT TO EXCEED .010 DIA.
4. REMOVE TWO FRONT FEET AND TWO REAR RUBBER PADS FROM RECEIVER. SLIDE RECEIVER, WITH DUST COVER IN PLACE, INTO ADAPTER PANEL AS SHOWN, AND SECURE WITH TWO RETAINER PLATES "A". PINS ON RETAINERS MATE WITH HOLES IN COVER, ON SOME STATUSES OF THE RADIO, PINS ON THE RETAINERS MATE WITH HOLES FOR COVER MOUNTING SCREWS FROM WHICH SCREWS HAVE BEEN REMOVED.
5. 699J-1 COLLINS PART NUMBER 792-6980-001 IS SHOWN. PART NUMBER 792-6980-002 IS ALSO AVAILABLE THAT HAS THE SPEAKER ON THE RIGHT HAND SIDE.



REAR VIEW



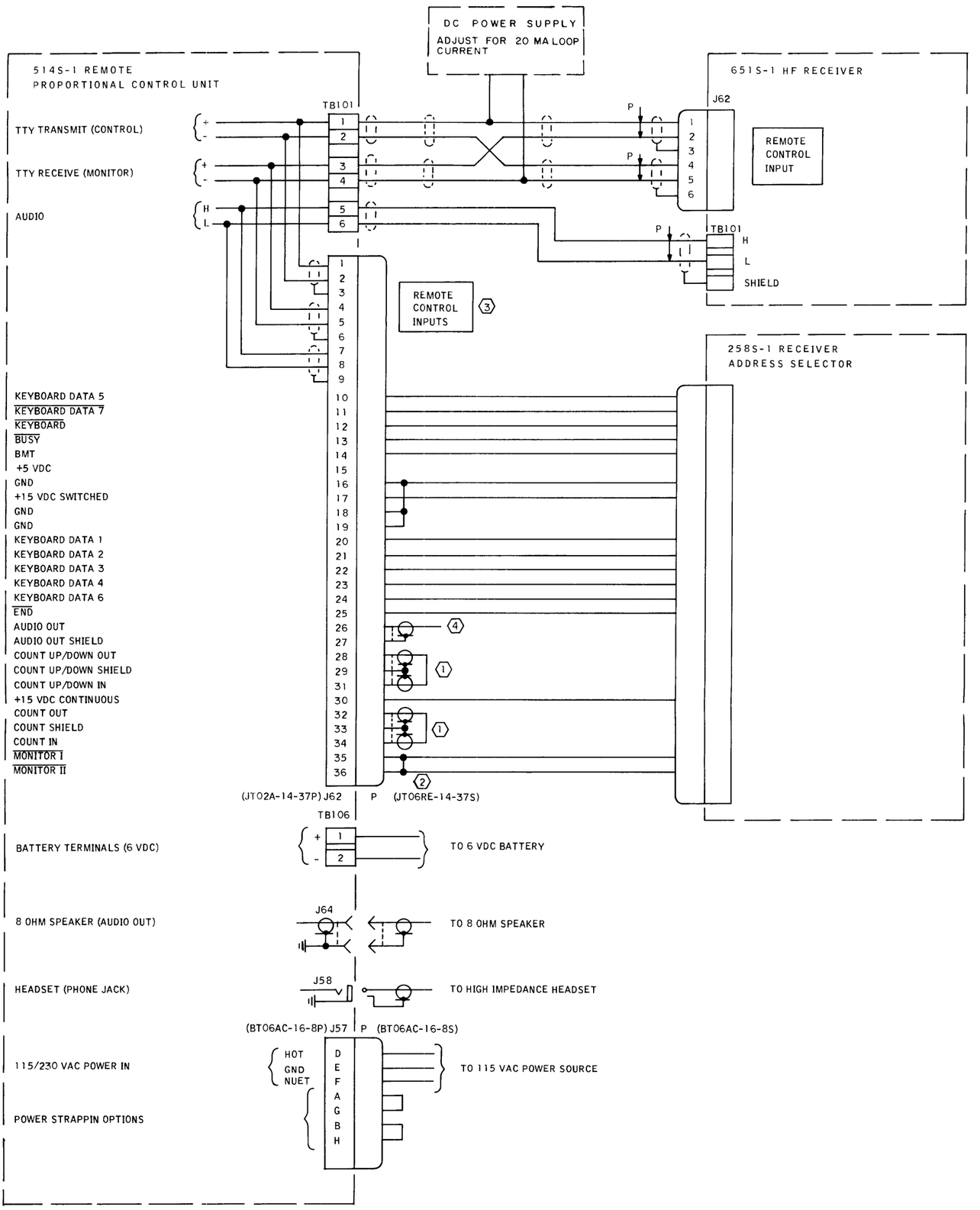
SIDE VIEW



FRONT VIEW

TP3-0333-014

651S-1/1A in 699J-1, Outline and Mounting Dimensions
Figure 3

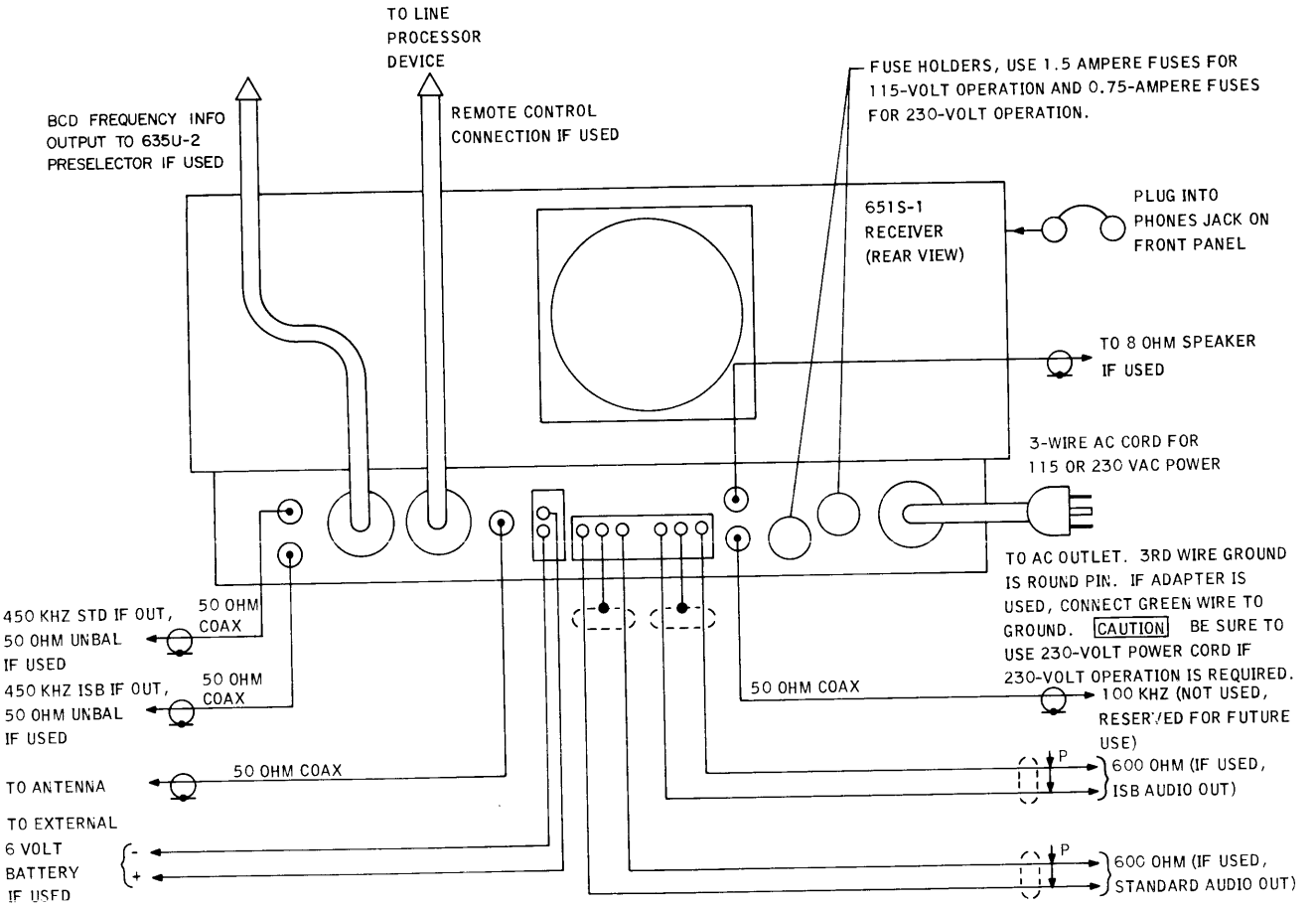


NOTES:

1. RESERVED FOR REMOTE FREQUENCY CONTROL. MUST BE STRAPPED AS SHOWN FOR NORMAL OPERATION.
2. MUST BE STRAPPED AS SHOWN FOR NORMAL OPERATION.
3. REMOTE CONTROL LINES TO 651S-1 MAY BE CONNECTED TOJ62, PINS 1 THROUGH 9, OR TO TB106 AS SHOWN.
4. AUDIO OUT FUNCTIONS IN PARALLEL WITH J64.

514S-1/651S-1/1A Interconnect Diagram
Figure 4

TP3-2447-014



TP2-7213-014

External Connections to 651S-1/1A
Figure 5

4.2 Remote Control Output

The multipin REMOTE CONTROL OUTPUT connector (J63) on the rear panel of the receiver provides bcd frequency information for controlling the 635U-2 RF Preselector. Refer to the chassis schematic in the diagrams section for connector pin function information. The connector on the rear panel is type JT02A-14-37PA(014), and the mating connector is type JT06RE-14-37SA-386.

4.3 100-kHz Input/Output Connector

The 100-kHz BNC coaxial connector (J65) on the rear panel of the receiver is not used (reserved for future use).

4.4 Mute

The receiver may be muted by removing the strapping option from TB103 (refer to the chassis schematic in the diagrams section). The receiver is muted when J62-22 is open; reception is normal when J62-22 is jumpered to J62-24.

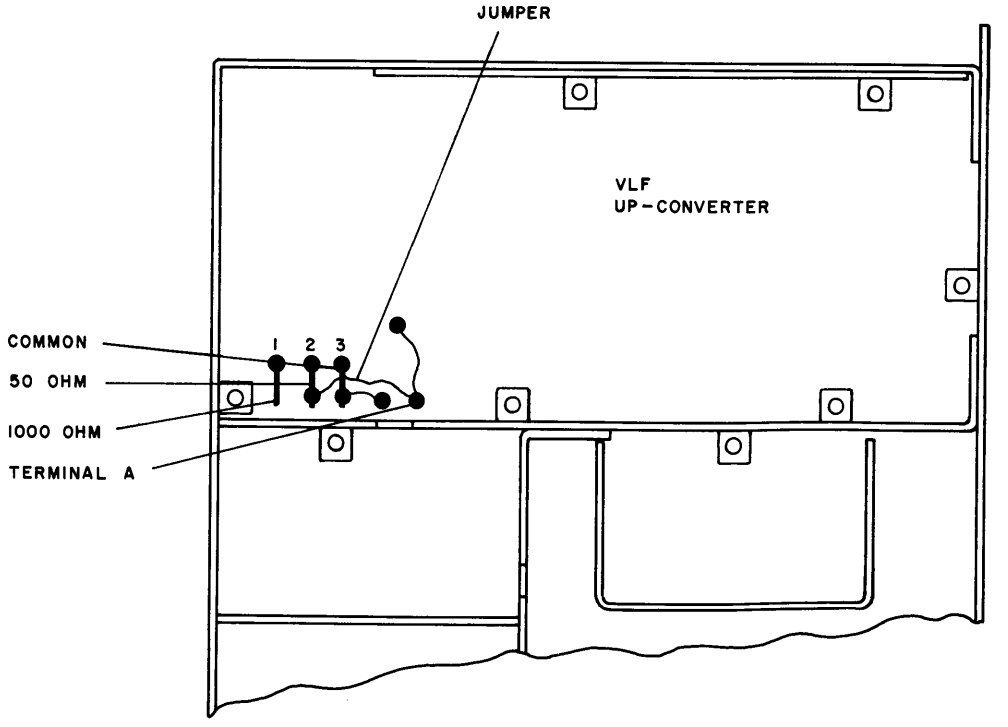
4.5 VLF Antenna Input Strapping (VLF Converter Only)

The input impedance of the receiver below 560 kHz may be changed from 50 ohms to 1000 ohms to obtain good performance from electrically very short antennas. In rf module A6 (790-1048-010), change jumper on terminal A from 50-ohm terminal to 1000-ohm terminal of filter FL601 (refer to figure 6).

4.6 Auto Scan Card A9, Installation and Strapping

4.6.1 Internal Strapping (Figure 7)

Strapping is accomplished by installing jumper clips (provided) in predetermined positions on the jackfield (J1) on the card. The odd-numbered pins of J1 are the programming input lines to the scan range dividers; even-numbered pins are ground. Jumper clips are used to ground the appropriate pins to set up the desired scan frequency and dwell time.



RF Module A6, VLF Version (790-1048-010, -021), Input Strapping Option
Figure 6

Note

An open input line is logic 1 and a grounded line is logic 0.

To program the scan range (frequency), subtract the desired scan range (in 100-Hz increments) from 1000 (100 kHz). Program the difference at J1 by installing grounding clips on the appropriate pins.

Example: A scan range of 9 kHz is desired.

1000 (100 kHz in 100-Hz increments)

-90 (9 kHz in 100-Hz increments)

910

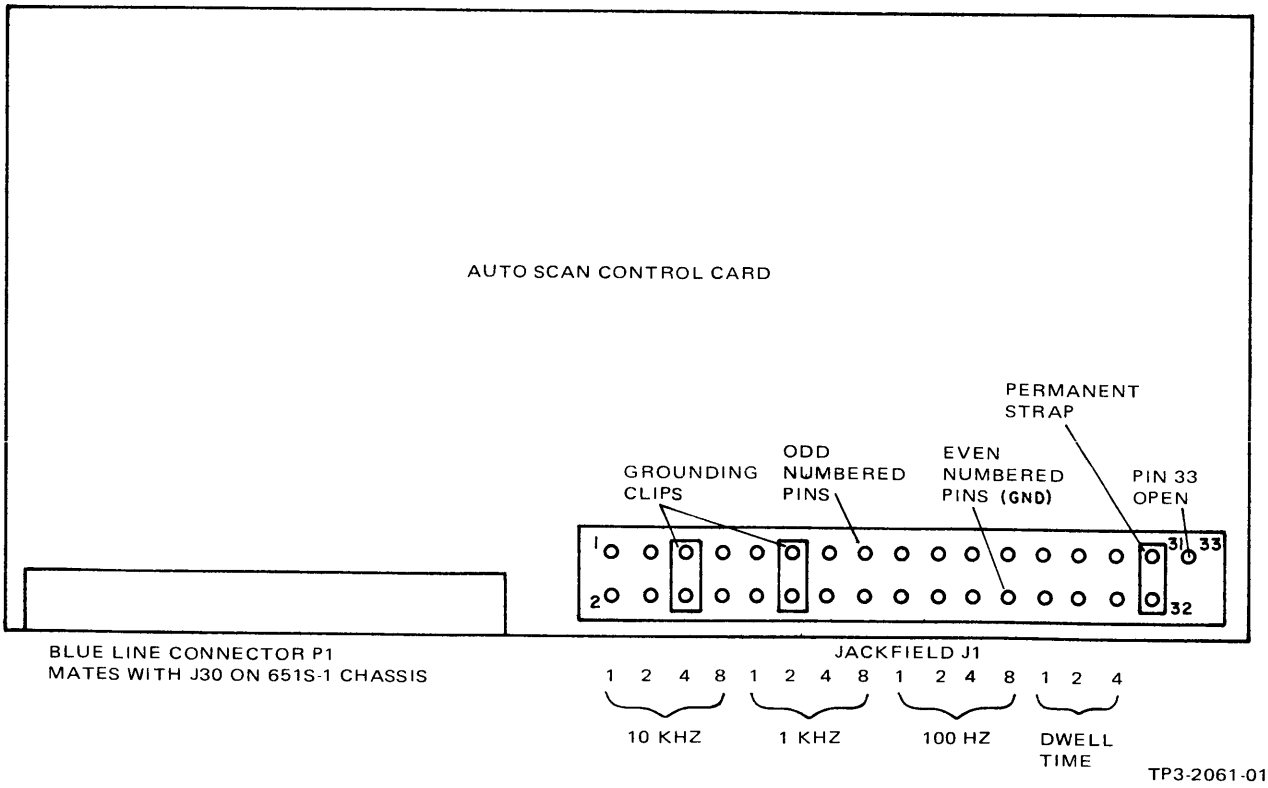
Program digits 9, 1, and 0 at the 10-kHz, 1-kHz and 100-Hz input lines respectively. (Refer to table 1 and figure 7.)

Table 1. Digit Code for 10-kHz, 1-kHz, 100-Hz, and Dwell-Time Inputs.

DIGIT	WT 1	2	4	8
0	X	X	X	X
1	-	X	X	X
2	X	-	X	X
3	-	-	X	X
4	X	X	-	X
5	-	X	-	X
6	X	-	-	X
7	-	-	-	X
8	X	X	X	-
9	-	X	X	-

- Indicates open line (logic 1)

X Indicates grounded by jumper clip (logic 0)



Auto Scan Control Card A9, Internal Strapping
Figure 7

To program dwell time (period in which the receiver remains on a discrete frequency), subtract the desired dwell time (in 100-millisecond increments) from 7 (700 milliseconds). Program the difference at J1 by installing grounding clips on the appropriate pins.

Example: A dwell time of 200 milliseconds is desired.

7 (700 milliseconds)

-2 (200 milliseconds)

5

Program the digit 5 at the dwell time program input lines (table 1 and figure 7).

The grounding clip on J1-31 to J1-32 must be installed and J1-33 must be open at all times for proper operation of the scan card.

4.6.2 External Strapping

External programming of the audio scan card is accomplished by using the 775L-1 Local Scan Control panel, Collins part number 620-9030-001, interfaced through rear connector J62 on the 651S-1/1A. External programming provides a variable frequency scan range and dwell time. Remove all grounding clips from J1 except put clips on the 100-Hz input lines; J1-17 to 18, J1-19 to 20, J1-21 to 22, J1-23 to 24, and the permanent clip J1-31 to 32.

4.6.3 Installation

4.6.3.1 Auto Scan Card Only

The auto scan card can be purchased as part of a modification kit or as an individual subassembly. To install card, perform the following:

a. Remove jumper straps from J30-29 to 31 and J30-32 to 34 on 651S-1/1A chassis sideboard.
b. Assure that card is properly strapped, refer to paragraph 4.6.1 or 4.6.2.
c. Insert card into 651S-1/1A chassis; make sure P1 on card mates properly with J30 on chassis.

4.6.3.2 Auto Scan Control Modification Kit

Installation Kit, Collins part number 609-1565-001, consists of an auto scan control card, a front panel switch plate, and an adapter card. To install, perform the following:

a. To install auto scan card, refer to paragraph 4.6.3.1.
b. Install switch plate on the REMOTE/LOCAL switch located on the 651S-1/1A front panel.
c. The adapter card permits normal operation of the 651S-1/1A when the auto scan card is removed without restrapping the chassis sideboard. To install, remove auto scan card from chassis and insert adapter card into J30.

4.7 TCU Card A9 Installation

Before installing the TCU card, remove the following jumpers from J30 on the 651S-1/1A sideboard:

a. J30-15 to -47
b. J30-29 to -31
c. J30-32 to -34
d. J30-42 to -43

On mating connector for J62 (from the 514S-1 control) jumper pin 2 to pin 4 (refer to paragraph 3.5.2). Ensure that a jumper is connected from J30-46 to J31-47 on the 651S-1/1A sideboard. Install TCU card by inserting it into J30 on the 651S-1/1A chassis.

651S-1/1A General Purpose HF Receiver

COLLINS

operation

Printed in USA

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3rd Edition, 15 October 1972

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NOTICE: This section replaces second edition dated 1 May 1972.

List of Effective Pages

*The asterisk indicates pages changed, added, or deleted by the current change.

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*Tab Divider	15 Oct 72
*Title	15 Oct 72
*A	15 Oct 72
*Rec of Rev	15 Oct 72
*1 thru 8	15 Oct 72

Record of Revisions

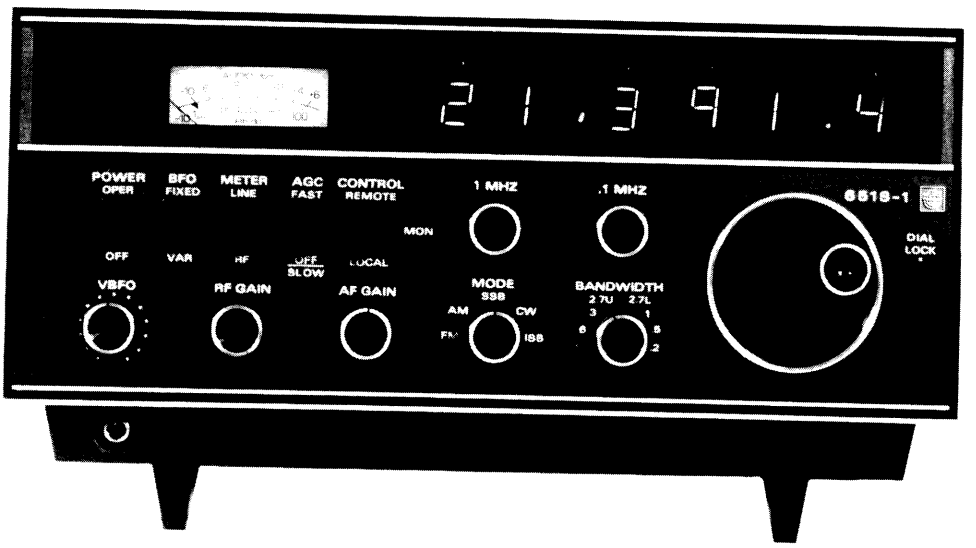
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1st Ed	1 Oct 71						
2nd Ed	1 May 72						
3rd Ed	15 Oct 72						

1. GENERAL

All the controls and indicators for manual control of the 651S-1/1A are located on the front panel. Table 1 lists the controls and indicators and briefly describes the function of each; figure 1 shows the controls and indicators on the front panel of the 651S-1/1A.



NOTE:
SILK-SCREEN ON BANDWIDTH SWITCH MAY VARY ON DIFFERENCE PART NUMBERS OF THE 651S-1/1A

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Operating Controls and Indicators
Figure 1

Table 1. Control or Indicator Function.

CONTROL OR INDICATOR	FUNCTION
Battery lamp	Red battery lamp lights when the external battery (if used) is providing keep-alive power to frequency memory circuits. Battery will supply power if the POWER switch is in OPER and a temporary power outage occurs. The lamp is just left of the front panel meter (not easily visible when not lit).

Table 1. Control or Indicator Function (Cont).

CONTROL OR INDICATOR	FUNCTION
AUDIO dbm/RF db meter	Indicates level of either 600-ohm audio output of rf signal depending on the position of the METER switch.
Frequency readout	Digitally indicates operating frequency selected.
POWER OPER-OFF switch	Applies switched and keep-alive voltages to circuits when in OPER position. All voltages are off when in OFF position.
BFO FIXED-VAR switch	Applies phase-locked fixed 450-kHz signal in SSB or CW mode when set to FIXED; applies 450-kHz variable bfo signal in SSB mode or CW mode when switch set to VAR.
METER LINE-RF switch	Controls front panel meter indications; audio signal level indicated when set to LINE or rf signal level indicated when set to RF.
AGC FAST-OFF-SLOW switch	Sets AGC release time; time is 100 ms at FAST and 1000 ms at SLOW. AGC is disabled in center position.
CONTROL REMOTE-MON-LOCAL switch	Allows manual control when set to LOCAL, remote control (optional cards required) when set to REMOTE, and signals status of receiver to remote control when set to MON.
1 MHZ control	Selects frequency in 1-MHz steps.
.1 MHZ control	Selects frequency in 0.1-MHz steps.
Tuning control	Selects frequency in 0.1-kHz steps.
DIAL LOCK switch	Disables tuning control in LOCK position.
VBFO control	Varies frequency of variable 450-kHz beat frequency oscillator when BFO switch is in VAR position; ±60 Hz in 10-Hz increments in SSB and ±900 Hz in 150-Hz steps in CW.
RF GAIN control	Controls rf gain.
AF GAIN control	Controls speaker audio level.
SQUELCH control (optional)	Controls squelch level and operating point; disables squelch circuits when in extreme counterclockwise position.
MODE selector	Selects operating modes of FM, AM, SSB, CW, and ISB.
BANDWIDTH selector	Selects if bandwidth (see table 2).

Table 2. IF Filters.

NOTES	BANDWIDTH SWITCH (pos)	MODE	IF FILTER 3-dB PASSBAND	FILTER ENABLED (*)
These positions are standard on all radios	16	AM or FM	16 kHz	ALL BYPASSED
	6	AM or FM	6 kHz	FL6
	3	AM	3 kHz	FL3
	2.7U	USB	2.7 kHz	FL5
	2.7L	LSB	2.7 kHz	FL7
The LSB filter is used in ISB operation	2.7L	ISB	2.7 kHz	FL7
Silk-screen for the last three clockwise positions of the BANDWIDTH SW may vary for various part no of the 651S-1	Top 1	CW	1.1 kHz	FL2
	Top 4	CW or AM	4 kHz	FL2
	Top WSRT	CW	1.1 kHz	FL2
	Top WBTY	CW	1.1 kHz	FL2
	Center .5	CW	500 Hz	FL1
	Center CW	CW	500 Hz	FL1
	Center 2	CW	2 kHz	FL1
	Bottom .2	CW	200 Hz	FL4
	Bottom NSRT	CW	370 Hz	FL4
	Bottom 1	CW	1.1 kHz	FL4

*See if filter cards A5A1 and A5A2 schematic diagram.

2. INPUT/OUTPUT CONNECTORS

The high-impedance headset audio connector is located on the lower left front panel and will accommodate a standard phone-jack type mating connector.

The rear panel (figure 2) contains the remaining input/output connectors and terminal strips. The functions of the connectors, listed from left to right, are as follows:

IF STD
connector ..... 450-kHz coaxial BNC if output that can be used to operate an RTTY converter, an oscilloscope, or for monitoring.

IF ISB
connector ..... 450-kHz coaxial BNC independent sideband if output point for monitoring (output from LSB filter when in ISB mode).

REMOTE CONTROL

OUTPUT
connector ..... Multipin output connector type JT02A-14-37PA (014) (mates with JT06RE-14-37SA-386) for bcd frequency information to 635U-2 Preselector.

INPUT
connector ..... Multipin input connector type JT02A-14-37P (014) (mates with JT06RE-14-37S-386) for all types of remote control.

ANT
connector ..... BNC coaxial input connector for receive signal.

BATT-6V
terminal block (Available option) ..... Connection point for external 6-volt battery.

AUDIO LINES
terminal block ..... Output points for standard and ISB audio at 600 ohms, center tapped (ISB audio is LSB audio when in ISB mode).

SPKR 8-OHM
jack (phono) ..... Output point for standard audio at 8 ohms.

100 KHZ
connector (BNC) ..... Input/output point for 100-kHz reference signal at 50 ohms. (Reserved for future use.)

PWR
connector ..... Multipin input connector type PT02A16-8P (mates with PT0-6A16-8S (SR) for 115/230-Vac input operating power.

3. MANUAL OPERATION

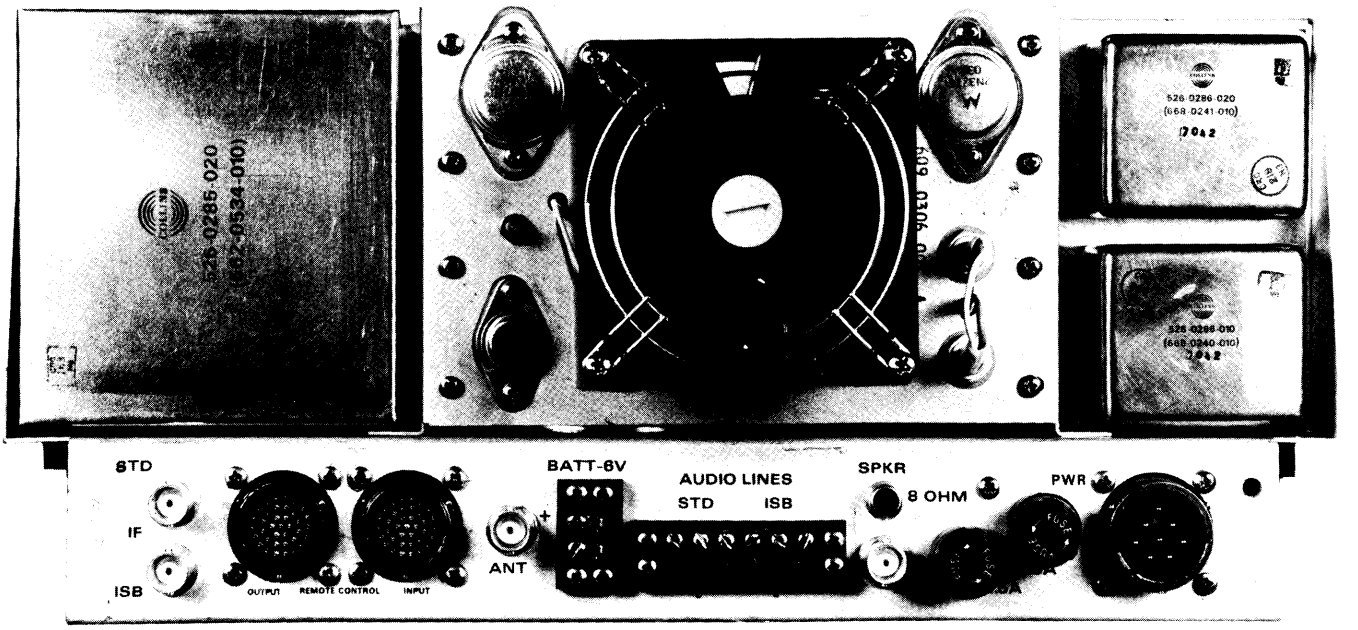
Note

MODE and BANDWIDTH switch settings are independent except as noted below for ISB mode operation.

3.1 Single-Sideband Reception

For proper single-sideband operation, perform the following steps:

a. Ensure primary power is connected properly.
b. Ensure rf antenna is connected to ANT jack.
c. Ensure speaker, headset, or power amplifier system is connected to appropriate audio output points.
d. Set POWER switch to OPER position.
e. Set BFO switch to desired position.
f. Set AGC switch to desired position.
g. Set CONTROL switch to LOCAL position.
h. Set frequency controls (1 MHZ, .1 MHZ, and large tuning knob) to desired frequency.



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Rear Panel Connectors, Cover Removed
Figure 2

i. Set METER switch to RF or LINE as necessary to read desired levels.
j. Set RF GAIN control fully clockwise (maximum signal strength).
k. Set AF GAIN control about midsetting.
l. Set mode selector to SSB.
m. Set BANDWIDTH switch to 2.7U or 2.7L.
n. Set SQUELCH control (optional) fully counterclockwise to OFF position.
o. Adjust the large tuning knob as necessary for best reception noted on meter.
p. After signal is received, set AF GAIN for desired listening level, set RF GAIN for best signal-to-noise ratio and, if BFO is set to VAR, set VBFO control for maximum intelligibility.
q. If squelch operation (optional) is desired, slowly turn SQUELCH control clockwise until background noise just drops out. Turning the control too far may result in blocking or reducing weak signals.

3.2 AM Reception

Operations for AM reception are the same as for sideband except for the following conditions:

a. Setting of BFO and VBFO controls does not affect AM reception.
b. Set MODE selector to AM.
c. Set BANDWIDTH switch to 3, 6, or 16.

3.3 CW Reception

Operations for CW reception are the same as for sideband except for the following conditions:

a. Set MODE selector to CW.
b. Set BANDWIDTH switch to desired bandwidth. (See table 2.)

3.4 FM Reception

Operations for FM reception are the same as for AM except for the following conditions:

a. Set MODE selector to FM.
b. Set BANDWIDTH switch to 6 or 16.

3.5 ISB Reception (Optional)

Operations for ISB reception are the same as for single sideband, except for the following conditions:

a. Optional ISB amplifier card A3 (778-2952-001) installed in radio.
b. Set MODE selector to ISB.
c. Set BANDWIDTH switch to 2.7U or 2.7L only.

Note

If it is necessary to adjust AGC or audio output controls on card A3, refer to maintenance section for adjustment procedure.

Note that the lower sideband audio and if outputs appear at the ISB audio and if output jacks at the rear of radio.

3.6 Frequency Scan Operation (Optional)

Frequency scan operation can be used with any type reception; operating procedures will be identical with the following exceptions:

a. Auto scan card A9 (793-9368-001) installed in radio.

Note

Ensure that 651S-1 chassis sideboard is properly strapped and card is programmed for the desired frequency scan range and dwell-time (refer to paragraph 4.6 in the installation section).

b. Set REMOTE/LOCAL switch to LOCAL.
c. Set the lower frequency limit by selecting the desired frequency on receiver.
d. Frequency scan is initiated by setting the REMOTE/LOCAL switch to REMOTE (SCAN) position.
e. A pause in frequency scanning is provided by setting switch to MONITOR; scanning will be resumed when switch is returned to REMOTE position.

Note

The receiver frequency display will follow the discrete frequency steps as scanning is being conducted.

4. REMOTE CONTROL OPERATION (OPTIONAL)

4.1 Processor Operation

For remote control operation, perform the following steps:

a. Ensure that optional DCFE card A8 (CPN 624-5744-001), and the appropriate optional DCU card A9 (CPN 793-9414-001, CPN 624-5781-001, or CPN 774-7842-001) are properly installed.

Note

If it is necessary to adjust rf gain controls on DCFE, refer to maintenance section for adjustment procedures.

b. Strap DCU address pins (pins 10, 11, 12, 13, and 14 on rear panel REMOTE CONTROL INPUT connector J62) to the desired address. For a logic 1 in an address position, strap that pin to pin 15 in connector J62; for a logic 0, strap to pin 18.

Note

An all 0 address will not properly control the receiver. An all 1 address is normally reserved for teletypewriter or crt control. Any one of the remaining 30 address possibilities is permissible and allows control of up to 30 separate receivers by one processor unit.

c. When DCU card 624-5781-001 or 774-7842-001 is installed, ensure that card is strapped for DCU address length of 5; the two clips (provided) should be installed on the two sets of posts marked 5 on the DCU card.
d. Ensure primary power is connected properly.
e. Ensure rf antenna is connected to ANT jack.
f. Ensure speaker, headset, or power amplifier system is connected to appropriate audio output points.
g. Connect processor unit to REMOTE CONTROL INPUT connector J62.
h. Set front panel CONTROL switch to REMOTE position.
i. Set front panel POWER switch to OPER position.
j. Send control words using control word content and format described in tables 7 and 8 of the description and principles of operation section of this instruction book. Monitor word content and format are described in tables 8 and 9 of the description and principles of operation section.

All functions in control word II are enabled by a logic 1 in that bit position of the control word. A logic 1 in local/remote bit position 30 of control word II places the receiver in local control without changing the front panel CONTROL switch from REMOTE to LOCAL.

The receiver may be returned to remote control by placing a logic 0 in bit position 30 of control work II.

Control word III provides vbfo and rf gain or squelch level control data to the receiver. The bcd code placed in vbfo bits 24, 25, 26, and 27 produces voltage levels that correspond directly to the voltage levels produced by front panel VBFO switch S112. The bcd code should, therefore, be limited to the 13 combinations from binary 0 to binary 12 to correspond to the 13 front panel switch positions. If interpolate enable bit 15 in control work II is a logic 1, the bfo variation is ± 60 Hz in 10-Hz steps. If vbfo enable bit 16 is a logic 1, the bfo variation is ± 900 Hz. The interpolate bfo frequency produced for each binary position is shown in table 3.

If DCFE card A8 is strapped for rf gain control, word III bits 28, 29, 30, and 31 provide bcd rf gain level information to the receiver. All 16 bcd combinations may be used with all 1's producing maximum rf gain (0-dB reduction) and all 0's producing minimum rf gain (90-dB reduction). Bit position 17 in control word II must be logic 0 to provide rf gain control.

Monitor word I is returned to the processor unit after the reception of control word I, III, or IV. Bits 10 through 31 of this monitor word contain bcd frequency information. A logic 1 in bit 9 indicates a power fault.

Monitor word II is returned to the processor unit after the reception of control word II.

A logic 1 in bit 9, 10, or 11 indicates a fault. If the front panel CONTROL switch is in REMOTE position, a logic 0 appears in bits 12 and 15. If the CONTROL switch is in LOCAL position, a logic 1 appears in bit 12 and a logic 0 in bit 15. If the CONTROL switch is in MON position, a logic 1 appears in bits 12 and 15. A logic 1 in bit 13 indicates the front panel POWER switch is in OPER

Table 3. Control Word III, Interpolate BFO Frequency Generation.

SWITCH STEPS	CONTROL WORD III BIT POSITION				INTERPOLATE FREQUENCY (kHz)
	24	25	26	27	
0	0	0	0	0	449.940
1	0	0	0	1	449.950
2	0	0	1	0	449.960
3	0	0	1	1	449.970
4	0	1	0	0	449.980
5	0	1	0	1	449.990
6	0	1	1	0	450.000
7	0	1	1	1	450.010
8	1	0	0	0	450.020
9	1	0	0	1	450.030
10	1	0	1	0	450.040
11	1	0	1	1	450.050
12	1	1	0	0	450.060

position. A logic 1 in bit 14 indicates no audio output. The mode of operation is indicated by coding of bits 16, 17, 18, and 19 (refer to table 10 in the description and principles of operation section). Bits 20, 21, 22, and 23 indicate the bcd vbfo control position and bits 24 through 31 repeat the 1-kHz and 100-Hz frequency information.

4.2 Operation With 514S-1 Remote Control Unit

Note

Refer to the 514S-1 instruction book (523-0764187) for interconnect information for the 514S-1 and 651S-1/1A.

For remote control TTY operation, perform the following steps:

a. Replace interconnect card A8 with optional DCFE card A8 (CPN 624-5744-001), and install optional TCU card A9 (CPN 783-9480-001). (Refer to paragraph 4.7 in the installation section for installation information for the TCU card.)

Note

If it is necessary to adjust rf gain controls on DCFE, refer to maintenance section for adjustment procedures.

b. Strap TCU address pins (pins 10, 11, 12, and 13 on rear panel REMOTE CONTROL INPUT connector J62) to the desired address in hexadecimal. For a logic 1 in an address position, strap that pin to pin 15 in connector J62; for a logic 0, strap to pin 18. Strap pin 14 (all call) to pin 18 in connector J62.

Note

No strapping is required for a single 651S-1 receiver controlled by a 514S-1 Remote Control Unit.

c. Ensure primary power is connected properly.
d. Ensure rf antenna is connected to ANT jack.
e. Ensure speaker, headset, or power amplifier system is connected to appropriate audio output points.
f. Connect 514S-1 Remote Control Unit to REMOTE CONTROL INPUT connector J62.

Note

If the receiver is to be remotely controlled over a greater distance then 1000 feet, TTY modems are required.

g. Set front panel CONTROL switch to REMOTE position.
h. Set front panel POWER switch to OPER position.
i. Operate the 514S-1 Remote Control Unit to control the receiver. Refer to 514S-1 instruction book for operation procedures.

651S-1/1A General Purpose HF Receiver

COLLINS

maintenance

Printed in USA

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3rd Edition, 15 October 1972

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NOTICE: This section replaces second edition dated 1 July 1972.

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Record of Revisions

RETAIN THIS RECORD IN THE FRONT OF MANUAL.
ON RECEIPT OF REVISIONS, INSERT REVISED PAGES IN THE MANUAL, AND ENTER DATE INSERTED AND INITIALS.

ASSIGNED TO (JOB TITLE)	LOCATION

REV. NO.	REVISION DATE	INSERTION DATE	BY	REV. NO.	REVISION DATE	INSERTION DATE	BY
1st Ed	1 Jan 72						
2nd Ed	1 Jul 72						
3rd Ed	15 Oct 72						

1. GENERAL

The 651S-1/1A General Purpose HF Receiver should be maintained with various levels of repair in mind. The simplest method of repair is card/module replacement. Procedures are included to isolate malfunctions to the card/module level. Overall test procedures are in table 2, and card/module test procedures are in tables 3 through 19. The next level of repair is chassis-mounted piece parts and wiring replacement. These parts include the front/rear panel parts, the power supply parts, the audio power amplifier parts, and the cabling. Also replacement of parts in rf module A6 is not too difficult.

The next level of repair is replacement of parts on all planar cards except the subcards on the four synthesizer cards (A10 through A13). Only technicians trained in repair of planar assemblies and replacement of microminiature packages should attempt this work. The last level of repair is replacement of parts on the synthesizer subcards. Many of the parts on these subcards are epoxied in place, or the whole subcard is epoxied, and replacement is very critical as well as difficult. Only Collins authorized repair facilities should attempt this work.

The intent of this maintenance section is to guide the technician to the probable cause of trouble (whatever level of repair is involved) and to recommend the method of repair.

Note

For ease of tuning the 651S-1/1A receiver and monitoring audio output, the audio output terminals should be terminated in a 600-ohm resistive load and an 8-ohm speaker connected to the SPKR jack for all tests except where noted.

2. TEST EQUIPMENT AND POWER REQUIREMENTS

Test equipment required to maintain the 651S-1/1A is listed in table 1. If the items listed are not available, equivalent test equipment may be used.

The power required to operate the 651S-1/1A during test is 115 or 230 volts ±10 percent, 47 to 63 Hz, 70 watts. An additional 40 watts is required if all the optional cards are installed. A source of 6 to 12 volts dc, 1 A unregulated, is required if the keep-alive function is to be checked.

Table 1. Test Equipment Required.

EQUIPMENT	MANUFACTURER TYPE NUMBER/ PART NUMBER	REQUIRED CHARACTERISTICS
Wave analyzer	HP 302A	Audio frequency, 2-tone analysis.
Signal generator (two required)	HP 606B	250 kHz to 30 MHz.
Two-tone generator	Collins 779-9878-001	Crystal accuracy; tones clear to 70 dB down. Frequencies required are 12.5, 10, 2, 1 MHz, and 450 kHz.
514S-1 Remote Control Unit	Collins 622-0370-102	Required to test TCU card A9.

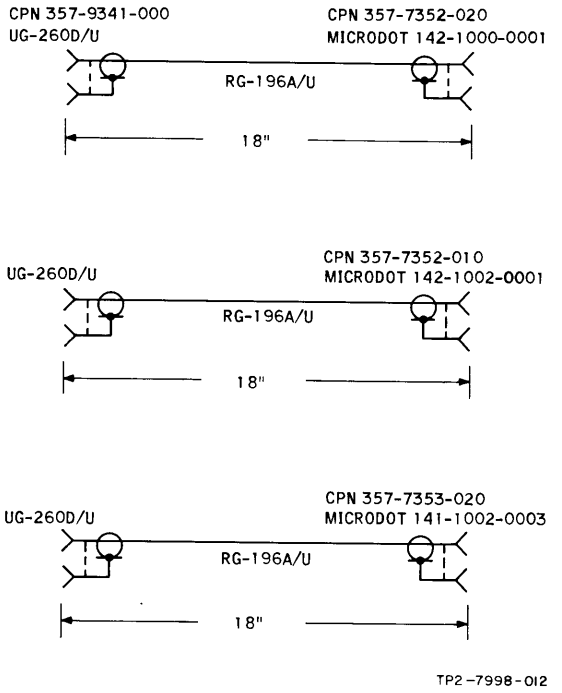
Table 1. Test Equipment Required (Cont).

EQUIPMENT	MANUFACTURER TYPE NUMBER/ PART NUMBER	REQUIRED CHARACTERISTICS
Signal generator	HP 608D	10 to 125 MHz.
Rf voltmeter	Boonton 91DA	0 to 10 Vrms rf, 400 kHz to 30 MHz.
Rf voltmeter adapter	Boonton 91-8B	50 ohms.
Distortion analyzer	HP 331A	0 to 15 Vrms, 0 to 30 percent distortion.
Oscilloscope	Tektronix 454	Measure 50-μs pulses.
Digital voltmeter	Fairchild 7000	Ac and dc measurements.
Variable rf pad	Daven RFB-543-5C	0 to 80 dB, 50 ohms.
Rf pad	Measurements 80-ZH3	6 dB, 50 ohms.
Pulse generator	HP 222A	5-V, 10-kHz, 50-μs pulses.
Frequency counter	HP 5245L	400 kHz to 109.35 MHz.
Frequency counter prescaler	HP 5252A	Increase range of HP 5245L.
FM signal generator	Marconi 1066B	400 kHz to 30 MHz.
Audio oscillator	HP 200CD	0 to 10 kHz, 600 ohms.
Serial digital word generator/ monitor	Collins 7404A-1	Generate/monitor biphase modulated 4800-Hz words.
Power meter	HP 432A	99 MHz, 0.05 to 5 mW.
Power meter thermistor mount	HP 478A	
Loudspeaker		8 ohms, 2 watts min.
Headphones		High impedance.
Dc power supply	Kepco ABC 40-0.5M	Variable 0 to 40 Vdc, 50 milliamperes.
Resistor	CPN 747-5418-000	8.2 ohms, 6.5 watts, 5%, with speaker cable attached.
Resistor	CPN 705-7042-000	75 ohms, 1/2 watt, 1%.
Resistor	CPN 705-3603-340	604 ohms, 1/4 watt, 1%.
Resistor	CPN 745-1352-000	1 kΩ, 1/2 watt, 10%.
Resistor	CPN 705-7068-000	261 ohms, 1/2 watt, 1%.
Resistor	CPN 745-1412-000	27 kΩ, 1/2 watt, 10%.
Resistor	CPN 745-1366-000	2.2 kΩ, 1/2 watt, 10%.
Resistor	CPN 745-1394-000	10 kΩ, 1/2 watt, 10%.
Resistor	CPN 745-1317-000	150 ohms, 1/2 watt, 10%.

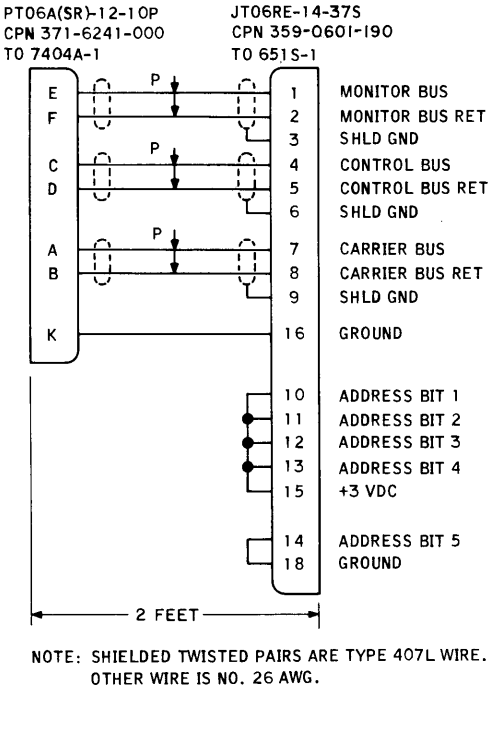
Table 1. Test Equipment Required (Cont).

EQUIPMENT	MANUFACTURER TYPE NUMBER/ PART NUMBER	REQUIRED CHARACTERISTICS
Resistor	CPN 705-3603-320	54.9 ohms, 1/4 watt, 1%.
Resistor	CPN 705-3602-260	549 ohms, 1/4 watt, 1%.
Resistor	CPN 705-6643-000	953 ohms, 1/4 watt, 1%.
Resistor	CPN 705-6536-000	56.2 ohms, 1/4 watt, 1%.
Resistor (four required)	CPN 705-3602-500	1810 ohms, 1/4 watt, 1%.
Resistor	CPN 705-6611-000	205 ohms, 1/4 watt, 1%.
Dc power source (power supply or battery)	Standard dc power supply	+6 to +12 Vdc.
Card extender	CPN 778-2953-001	Extend card A1.
Card extender	CPN 778-2954-001	Extend card A2.
Card extender	CPN 778-2959-001	Extend card A3.
Card extender	CPN 778-2955-001	Extend card A4.
Card extender	CPN 778-2956-001	Extend card A5.
Card extender	CPN 790-2667-001	Extend card A6.
Card extender	CPN 778-2957-001	Extend card A7.
Card extender	CPN 778-2958-001	*Extend card A8.
Card extender	CPN 778-2856-006	**Extend card A9.
Card extender	CPN 778-2856-004	Extend card A10.
Card extender	CPN 778-2856-010	Extend card A11.
Card extender	CPN 778-2856-009	Extend card A12.
Card extender	CPN 778-2856-008	Extend card A13.
Card extender	CPN 606-3397-001	Extend card A14.
Serial digital test adapter cable	Fabricate	Refer to figure 3.
Remote control cable	Fabricate	Refer to figure 11.
Two-tone mixer adapter	Fabricate	Refer to figure 2.
BNC to subminiax adapter cables	Fabricate	Refer to figure 1.
Power meter adapter cable	Fabricate	Refer to figure 4.

*Card A8 extender extends either the interconnect card or the DCFE card.
**Card A9 extender extends either the DCU card, TCU card, or scan control card.



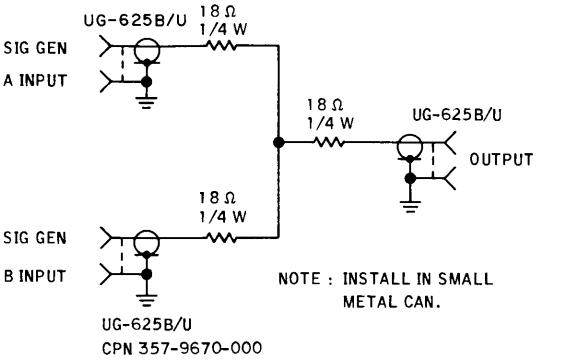
BNC to Subminiax Adapter Cables, Schematic Diagram
Figure 1



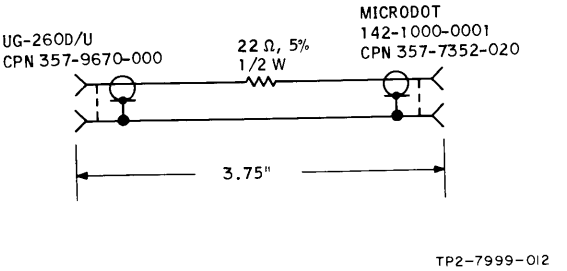
NOTE: SHIELDED TWISTED PAIRS ARE TYPE 407L WIRE.
OTHER WIRE IS NO. 26 AWG.

TP2-7996-012

Serial Digital Test Adapter Cables, Schematic Diagram
Figure 3



Two-Tone Mixer Adapter, Schematic Diagram
Figure 2



Power Meter Adapter Cable, Schematic Diagram
Figure 4

Table 2. Overall Performance Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Controls check	a. Set POWER switch to OFF. Connect the speaker. Be sure all assemblies are completely inserted and that all coax connectors are properly mated.		
	b. Set POWER switch to ON. Set BFO switch to FIXED. Set METER switch to RF. Set AGC switch to FAST. Set CONTROL switch to LOCAL. Set SQUELCH switch to OFF (optional). Set DIAL switch to unlock. Set MODE switch to SSB. Set AF GAIN control to midrange. Set BANDWIDTH switch to 2.7U.		
	c. Select 10.0000 MHz and adjust the RF GAIN control for a 40-dB meter indication.		
	d. Note status of comma in frequency readout.	Lit.	Check voltage to DS105 (+25 Vdc nominal). If voltage is normal, replace lamp.
	e. Rotate RF GAIN control and note meter level and background noise level. Reset for 1 μV on meter.	Affects meter and background noise level.	Check wiring. Replace control. Check METER switch.
	f. Rotate AF GAIN control and note audio level.	Affects audio level.	Check wiring. Replace control.
	g. Set DIAL switch to LOCK. Rotate large tuning knob.	Frequency does not change.	Check wiring to switch. Check switch (replace if necessary). Substitute card A14. If A14 faulty, test, using procedures in table 19.
	h. Set DIAL switch to unlock. Check all tuning controls to see that they can select all digits of frequency.	All controls operate properly.	Check wiring to switches. Substitute card A7. If A7 is faulty, test, using procedures in table 9. Substitute card A14. If faulty, test, using procedures in table 19. Replace faulty control(s).

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. AGC action	a. Connect the signal generator to the ANT jack through a 6-dB pad and set it for 1-μV output at 28.0000 MHz.		If this test does not meet standards, test the 651S-1/1A using test 18 of this table.
	b. Set the 651S-1/1A to 27.9990 MHz in SSB, BANDWIDTH to 2.7U, with the AGC switch in the off (center) position and with the RF GAIN control set to maximum cw position.		
	c. Connect a 600-ohm resistor and the distortion analyzer across the AUDIO LINES STD terminals. Set the analyzer to VOLTMETER.		
	d. Connect an rf voltmeter (with 50-ohm probe) to the STD IF output jack.		
	e. Tune the 651S-1/1A for maximum if output on rf voltmeter and check audio output level.	Audio level; NLT 0 dBm.	Perform test 7.
	f. Set AGC to FAST and check audio output level.	NLT -1 dBm.	Test card A4 using table 6.
	g. Check if output level.	40 to 70 mV.	
	h. Set signal generator for 0.1-V output. Check increase of audio level.	NMT 6 dB increase.	Same as step f.
	i. Repeat preceding steps if anything was adjusted because there is interaction between potentiometers.		
	j. Set the AGC switch to SLOW. Set the signal generator for 0.01-V output. Disconnect the signal generator. The audio tone should disappear, the speaker output should be relatively quiet for approximately 1 second, then background noise should be heard. Reconnect generator.	As in procedure.	If AGC is inactive completely, test card A2 using table 4. If slow or fast, repeat this entire test.
	k. Set the AGC switch to FAST. Disconnect the signal generator. The time between audio and background noise should be almost undetectable (approximately 0.1 second). Reconnect generator.	As in procedure.	Same as step j.
	l. Set the AGC switch to off (center). Audio level should increase appreciably.	As in procedure.	Same as step j.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Mode	a. With equipment connected as in test 2, set the 651S-1/1A and signal generator to 10.0000 MHz.		
	b. On 651S-1/1A, set AGC to ON, MODE to AM, and BANDWIDTH to 16. Set signal generator output level to 10 μV, modulated 30 percent at 400 Hz.		
	c. Check audio out with modulation on, then off.	Audio output with modulation on. No audio output with modulation off.	Perform test 7, then test card A2 using table 4.
	d. Adjust signal generator output to 1-μV and turn modulation off.		
	e. Set 651S-1/1A MODE to SSB. Sweep the signal generator frequency across the 651S-1/1A frequency and note audio output.	Audio output present when signal generator frequency is swept by the 651S-1/1A frequency and not present when the signal generator is 20 kHz or more from the 651S-1/1A frequency.	Same as step c.
	f. Set 651S-1/1A MODE to CW and repeat step e.	Same as step e.	Same as step c.
4. Selectivity (standard filters)	a. Connect a frequency counter to the UNCAL RF jack on the signal generator (to monitor frequency). Leave other equipment connected as in test 3.		
	b. Set 651S-1/1A MODE to SSB, BANDWIDTH to 2.7U, AGC off, and frequency to 1.1100 MHz.		
	c. Set signal generator for 1.1110 MHz at 1000-μV output.		
(Cont)	d. Adjust 651S-1/1A rf gain for a convenient if output level indicated on the rf voltmeter (30 to 100 mV). Slowly sweep the signal generator frequency across the passband of the 651S-1/1A to find the peak if output. Use this as a 0-dB reference.		

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	e. Slowly increase signal generator frequency until the if output drops 3 dB from peak response, note signal generator frequency.	Upper freq: NMT 1.1135 MHz.	Test filter card A5 using table 7.
	f. Slowly decrease signal generator frequency below the 651S-1/1A frequency until the if output again drops 3 dB from peak response, note signal generator frequency.	Lower freq: NLT 1.1102 MHz.	Same as step e.
	g. Compute the 3-dB bandwidth by subtracting the lower frequency limit from the upper frequency limit.	3-dB bw: 2.290 to 3.110 kHz.	Same as step e.
	h. Set signal generator to 1.1090 MHz and set the 651S-1/1A BANDWIDTH to 2.7L.		
	i. Repeat steps d through g for the LSB filter.	3-dB BANDWIDTH Upper freq: NMT 1.1098 MHz. Lower freq: NLT 1.1065 MHz. Bw: 2.290 to 3.110 kHz.	Same as step e.
	j. Set 651S-1/1A MODE to AM, BANDWIDTH to 6, AGC on, and frequency to 1.1100 MHz.		
	k. Set signal generator to 1.1100 MHz modulated 30 percent at 400 Hz.		
	l. Repeat steps c through g for the AM, 6-kHz filter, except measure the 6-dB points.	6-dB bw: From 5.100 to 6.900 kHz.	Same as step e.
	m. Set the 651S-1/1A MODE to 3, and repeat steps c through g for the AM, 3-kHz filter.	3-dB bw: From 2.550 to 3.450 kHz.	Same as step e.
5. Selectivity (optional filters) (Cont)	a. If the 500-Hz CW filter is installed in A5A1 or one of the optional A5A2 filter subcards is installed, determine which bandwidths are being used and check their filtering performance.		

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	b. Set the 651S-1/1A MODE to CW, BANDWIDTH to the appropriate position, and repeat steps 4.c through 4.g for the appropriate filters installed.	The total 3-dB bandwidth shall be within 50 percent of the nominal bandwidth.	If a failure occurs, test subcard(s) using procedures in table 7.
	BANDWIDTH SWITCH / FILTER / NOMINAL 3-dB BANDWIDTH		
	1st CW position (1, 4, WSRT, or WBTY): 1 kHz	1 kHz	
	1.1 kHz (offset +2 kHz)	1.1 kHz	
	1.1 kHz (offset +2.55 kHz)	1.1 kHz	
	4 kHz	4 kHz	
	2nd CW position (.5, 2, or CW): 500 Hz	500 Hz	
	2 kHz	2 kHz	
	3rd CW position (.2, 1, or NSRT): 200 Hz	200 Hz	
	370 Hz (offset +2 kHz)	370 Hz	
	1.1 kHz	1.1 kHz	
6. Sensitivity	a. Connect signal generator through a 6-dB pad to the ANT jack and set for 5 μV at 281 kHz. Set 651S-1/1A MODE to SSB, AGC off, BANDWIDTH to 2.7U at 280 kHz. Note audio output level (vary frequency slightly to peak audio out).	Audio out more positive than -8 dB. Use as reference only.	Perform test 7, (gain).
	b. Disconnect signal generator and note drop in audio level.	Snr: NLT 10 dB.	Test module A6 using table 8.
	Note Set signal generator 1 kHz higher than the 651S-1/1A for USB and 1-kHz lower for LSB.		
	c. Repeat steps a and b at 500 kHz and 1250 kHz with the signal generator set to 2.5-μV output.	Snr: NLT 10 dB.	Same as step b.
(Cont)	d. Repeat steps a and b at 2.05 MHz, 8.05 MHz, and 28.05 MHz with signal generator set to 0.7-μV output.	Snr: NLT 10 dB.	Same as step b.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	e. Set signal generator to 2.05 MHz, 3.5 μV modulated 30 percent at 400 Hz. Set 651S-1/1A MODE to AM, BANDWIDTH to 6, AGC on, and frequency to 2.05 MHz. Note audio output level. (Vary frequency slightly to peak audio out.)	Reference.	Test card A4 using table 6.
	f. Turn modulation off and note drop in audio output.	Snr: NLT 10 dB.	Same as step b.
7. Gain	a. Set 651S-1/1A MODE to SSB, BANDWIDTH to 2.7U, AGC on, and frequency to 280 kHz. Set signal generator to 281 kHz at 1 μV. (Vary frequency slightly to peak audio out.)		
	b. Measure audio output.	NLT 0 dBm.	Test card A2 using table 4.
	c. Repeat steps a and b at 500 kHz, 1.250 MHz, 2.05 MHz, 8.05 MHz, and 28.05 MHz.	NLT 0 dBm.	Same as step b.
	d. Set 651S-1/1A BANDWIDTH to 2.7L and frequency to 2.05 MHz. Set signal generator to 2.0490 MHz at 1 μV. (Vary frequency slightly to peak audio out.)		
	e. Measure audio output.	NLT 0 dBm.	Same as step b.
(Cont)	f. Set 651S-1/1A MODE to CW and BANDWIDTH to the applicable position. Turn modulation off on signal generator and set to 2.051 MHz at 3 μV. Vary frequency slightly to peak audio output.		

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. (Cont)	g. Measure audio output for appropriate filters installed. BANDWIDTH 2.7U 1 or WRST or 4 or WBTY .5 or CW or 2 .2 or NSRT or 1	 NLT -6 dBm NLT -6 dBm NLT -6 dBm NLT -6 dBm	Same as step b.
8. Meter calibration	a. Set signal generator to 28.0000 MHz unmodulated with 0.10 mV output. Set 651S-1/1A to 27.9990 MHz in SSB, BANDWIDTH to 2.7U, and AGC on. Tune the 651S-1/1A as necessary for a 1-kHz beat note.		
	b. Set the METER switch to RF. Set the RF GAIN control to maximum cw. Note meter indication.	80 ±3 dB.	Adjust A4R109.
	c. Set signal generator output to 1 μV. Set the METER switch to LINE. Note audio output.	0 ±1 dBm.	Adjust A2R70.
	d. Set the METER switch to RF. Vary generator output to set meter at 1 μV.	1 μV ±3 dB.	
9. ISB operation (optional)	a. Connect the 600-ohm load resistor and the distortion analyzer to the AUDIO LINES ISB 600-ohm audio output terminals. Connect the rf voltmeter (with 50-ohm probe) to the ISB IF jack.		
	b. Set signal generator to 10.0000-MHz output at 1 μV. Set the 651S-1/1A to 10.0010 MHz in the ISB mode, BANDWIDTH to 2.7U, with AGC set to off (center) position.		
	c. Check the audio level.	+1 dBm.	Adjust A3R92.
	d. Set 651S-1/1A AGC to SLOW. Check audio level.	More positive than -1 dBm.	Adjust A3R57.
	e. Check if output level.	35 to 70 mV.	
	f. Increase signal generator output to 0.1 V. Check that if and audio output levels increase.	NMT 6 dB increase.	Adjust A3R7.
	g. If any adjustments are made, repeat the entire test.		

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. FM operation (optional)	a. Connect FM signal generator to ANT jack through 6-dB pad.		
	b. Tune 651S-1/1A and FM generator to 10,000 MHz. Set generator output at 100 μV with 1-kHz deviation.		
	c. Set 651S-1/1A to CW mode, BANDWIDTH to .5, and set METER switch to RF. Peak 651S-1/1A meter indication by tuning the FM generator frequency (stay within 500 Hz of 10 MHz).		
	d. Set 651S-1/1A to FM mode and BANDWIDTH to 6.		
	e. Tune FM generator incremental frequency off frequency to 3 kHz above and below 10 MHz.	Audio does not degrade appreciably.	Test card using procedures in table 6.
	f. Repeat step e but go beyond 3-kHz limits.	Audio degrades after approximately 3-kHz deviation.	Test card using procedures in table 6.
	g. Repeat steps e and f with 651S-1/1A in FM mode, BANDWIDTH to 16, and using incremental frequency limits of ±8 kHz.	Same as steps e and f.	
11. Audio distortion	a. Ensure that the magnetic card cage covers are on. Actuate the 2-tone signal source (12.5 MHz is used in the following steps as a typical test frequency; any frequency between 5 and 15 MHz is satisfactory). Set one for 12.5006 MHz with 50-mV output and the other to 12.5016 MHz with 50-mV output. (Measure the 50-mV output with rf voltmeter and 50-ohm probe.) Connect the two generators through the 2-tone mixer adapter (figure 2) to the ANT jack.		
	b. Connect the wave analyzer across a 600-ohm resistor and connect both to the AUDIO LINES STD 600-ohm terminals.		
	c. Set 651S-1/1A to SSB, BANDWIDTH to 2.7U, at 12.5000 MHz, and AGC on. Record the dB level of the distortion products listed below with respect to F1. Note that the audio output signals are at 600 Hz (F1), and 1600 Hz (F2).		Test card A2 using procedures in table 4.
(Cont)			

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
11. (Cont)	F1 (600 Hz) F2 (1600 Hz) 2F2-F1 (2600 Hz)	0-dB reference. 0 ±1 dB. NLT 40 dB down.	
	d. Turn off the tone at 12.5006 MHz and disconnect the wave analyzer. Connect the distortion analyzer AF INPUT to the AUDIO LINES 600-ohm terminals. Set the distortion analyzer to SET LEVEL and set it for 0-dB reference (at 600 Hz). Set the distortion analyzer to DISTORTION and record total distortion (audio output signal is now 1600 Hz).	NLT 40 dB down.	
	e. (Optional) Repeat steps a, b, and c with 651S-1/1A in ISB mode, BANDWIDTH to 2.7U, at 12.5022 MHz with wave analyzer connected to AUDIO LINES ISB 600-ohm terminals.		Test card A3 using procedures in table 5.
	F1 (600 Hz) F2 (1600 Hz) 2F2-F1 (2600 Hz)	0-dB reference. 0 ±1 dB. NLT 40 dB down.	
12. Power output and distortion	a. Connect one tone of the 2-tone generator to the ANT jack. Connect the 8-ohm resistor (with speaker cable) to the SPKR jack.		
	b. Connect the distortion analyzer METER inputs to the 8-ohm resistor.		
(Cont)	c. Set tone generator for 0.1-V output. Set AF GAIN for 4-V audio. Move audio to AF INPUT terminals of distortion analyzer. Switch distortion analyzer to SET LEVEL. Set for 0 dB. Switch to DISTORTION and measure the total distortion.	NLT 33 dB down from 0-dB reference.	Check Q1, Q2, and U1 and associated components in chassis-mounted audio amplifier circuit. Replace faulty component.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. (Cont)	d. Plug high impedance headphones into front panel headphone jack and note that audio is transferred from speaker jack (audio meter indication at speaker jack disappears) to headphones.	Audio transfers.	Check wiring to J58 (headphone jack). Replace jack if wiring checks out.
13. Vbfo operation	a. Connect one tone of the 2-tone generator to the ANT jack. Set for 1-MHz output at 0.01 V.		
	b. Connect the frequency counter to the 8-ohm resistor (connected to SPKR jack).		
	c. Tune 651S-1/1A to 0.9990 MHz in SSB, BANDWIDTH to 2.7U, BFO to VAR.		
	d. Measure output frequency at each position of the VBFO control starting at extreme counterclockwise position.	Frequency changes in steps of approximately 10 Hz.	Test card A2 using table 4.
	e. Set 651S-1/1A to CW, BANDWIDTH to 2.7U or .5/CW/2 as appropriate and repeat step d. Readings between limits of VBFO control do not have to be linear.	Frequency changes in step of approximately 150 Hz.	Same as step d.
14. Squelch operation (optional)	a. Connect an hf signal generator through a 6-dB pad to the ANT jack. Connect a speaker to the SPKR jack. Set the signal generator to 10.0000 MHz with 3-μV output, unmodulated.		
(Cont)	b. Set 651S-1/1A to 10.0 MHz in AM mode, BANDWIDTH to 6. Set SQUELCH control at maximum ccw position against the switch, but do not operate the switch.	Circuit noise is audible.	

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. (Cont)	c. Modulate signal generator with 400 Hz at 15%. Slowly rotate SQUELCH control in cw direction until squelch circuit disables audio output.	SQUELCH control is 10 to 30° from ccw end when audio goes off.	Test card A2 using table 4.
	d. Increase modulation to 90%.	Audio comes on.	
	e. Rotate SQUELCH control to maximum cw position.	Audio stays on.	
	f. Turn SQUELCH control to OFF.	Audio stays on.	
	g. Disconnect signal generator.		
15. Battery keep-alive operation (optional)	a. Connect +6 to +12-Vdc source (power supply or battery) to BATT-6V terminals. Note frequency readout.		
	b. Disconnect power plug from ac source (651S-1/1A POWER switch in OPER). Leave disconnected for 30 seconds.	Red battery light comes on.	Ensure battery voltage is applied to DS101. Check Q501 through Q504 and associated parts.
	c. Reconnect line cord and check frequency readout.	Same frequency as step a.	Check that battery voltage (+5 Vdc) is getting to card A14. If it is, test A14, using table 19.
16. Optional remote control monitor operation (Collins DCU/ DCFE cards installed)	***Caution*** Assure that J30-46 is not jumpered to J31-47 on the 651S-1/1A sideboard.		
	a. Connect 651S-1/1A to primary power. Set POWER switch to OFF. Connect speaker. Connect signal generator through 6-dB pad to ANT jack. Connect frequency counter to UNCAL RF jack on signal generator. Connect 7404A-1 Source Generator/Display Unit LCU SINE WAVE connector to 651S-1/1A REMOTE INPUT connector using special cable (figure 3).		
(Cont)	b. Set signal generator to 10.0000 MHz at 100-μV output modulated 30% at 1 kHz.		

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. (Cont)	c. Set 651S-1/1A controls as follows: POWER OFF BFO FIXED METER RF AGC FAST CONTROL LOCAL VBFO MAX CCW RF GAIN MAX CW SQUELCH (optional) OFF MODE FM AF GAIN Midsetting BANDWIDTH 6 d. Set 7404A-1 front panel controls as follows: POWER ON PARITY MODE SENSED RETRANSMIT OFF MODE FDX ADDRESS LENGTH 5 BIT PARITY ENCODE MANUAL e. Set 7404A-1 rear panel controls as follows: Function LCU Sine/logic SINE f. Set 7404A-1 control word switches 0 thru 4 to logic 1 (up) and switch 5 to logic 0 (down) for all tests.		
	g. Set 651S-1/1A POWER switch to ON. Press 7404A-1 CLEAR pushbutton and then set switch 7 up and the remaining switches (6, 8 thru 31) down. Press SEND/READY pushbutton. Note 7404A-1 lamps.	7404A-1 lamp 0 out. 1 thru 4 lit (logic 1); 5 and 6 out (logic 0); 7 lit; 8 out; 9 lit; 10 out; 12, 13, and 14 lit; 15 through 19 out; and disregard 11 and 20 through 31.	Repeat test. Test card A8 or A9 using table 11 or 12.
	h. Press 7404A-1 CLEAR pushbutton and set switch 7 down, 8 up, 9 and 10 down, 11 up, and 12 thru 31 down. Press SEND/READY pushbutton.	Disregard response. This is just to sync the 651S-1.	Same as step g.
(Cont)	i. Set 651S-1/1A to FM, BANDWIDTH to 16. Set BFO switch to VAR. Press 7404A-1 CLEAR button and set 7404A-1 switch 7 up and 8 thru 31 down. Press SEND/READY button.	Lamps 8 thru 11 out, 12 thru 14 lit, 15 thru 23 out, disregard others.	Same as step g.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. (Cont)	j. Set 651S-1/1A to AM, BANDWIDTH to 3, and set VBFO control one stop from extreme ccw. Press 7404A-1 CLEAR button, then press SEND READY button.	Lamps 8 thru 11 out, 12 and 13 lit, 14 and 15 out, 16 lit, 17 thru 22 out, 23 lit, disregard others.	Same as step g.
	k. Set 651S-1/1A to AM, BANDWIDTH to 6, with VBFO control in second stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, 14 and 15 out, 16 lit, 17 thru 21 out, 22 lit, 23 out, disregard others.	Same as step g.
	l. Set 651S-1/1A to AM, BANDWIDTH to 16, with VBFO control in third stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, 14 and 15 out, 16 lit, 17 thru 21 out, 22 and 23 lit, disregard others.	Same as step g.
	m. Set signal generator to CW. Set 651S-1/1A to 9.9991 MHz in SSB, BANDWIDTH to 2.7U, with VBFO control in fourth stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 thru 17 out, 18 lit, 19 and 20 out, 21 lit, 22 and 23 out, 24 lit, 25 and 26 out, 27 lit, 28 thru 30 out, 31 lit.	Same as step g.
	n. Set 651S-1/1A to 10.0009 MHz in SSB, BANDWIDTH to 2.7L, with VBFO control in fifth stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 thru 18 out, 19 lit, 20 out, 21 lit, 22 out, 23 lit, 24 thru 27 out, 28 lit, 29 and 30 out, 31 lit.	Same as step g.
	o. Set 651S-1/1A to CW, BANDWIDTH to .2/1, with VBFO control in sixth stop and CONTROL switch in MON. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 out, 17 lit, 18 thru 20 out, 21 and 22 lit, 23 thru 27 out, 28 lit, 29 and 30 out, 31 lit.	Same as step g.
(Cont)	p. Set 651S-1/1A to CW, BANDWIDTH to .5/2, with VBFO control in seventh stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 out, 17 lit, 18 thru 20 out, 21 thru 23 lit, 24 thru 27 out, 28 lit, 29 and 30 out, 31 lit.	Same as step g.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. (Cont)	q. Set 651S-1/1A to CW, BANDWIDTH to 1/4, with VBFO control in eighth stop. Set 7404A-1 switches 7, 8 and 29 up (others as they were) and press the CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 out, 17 lit, 18 and 19 out, 20 lit, 21 thru 27 out, 28 lit, 29 and 30 out, 31 lit.	Same as step g.
	r. Set 651S-1/1A to ISB, BANDWIDTH to 2.7L, with VBFO control in ninth stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 and 17 out, 18 lit, 19 out, 20 lit, 21 and 22 out, 23 lit, disregard others.	Same as step g.
	s. Set 651S-1/1A VBFO control to tenth stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 and 17 out, 18 lit, 19 out, 20 lit, 21 out, 22 lit, 23 out, disregard others.	Same as step g.
	t. Set 651S-1/1A VBFO control to eleventh stop. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 and 17 out, 18 lit, 19 out, 20 lit, 21 out, 22 and 23 lit, disregard others.	Same as step g.
	u. Set 651S-1/1A VBFO control to twelfth stop (max cw). Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 11 out, 12 and 13 lit, disregard 14, 15 lit, 16 and 17 out, 18 lit, 19 out, 20 and 21 lit, 22 and 23 out, disregard others.	Same as step g.
(Cont)	v. Set 651S-1/1A CONTROL switch to REMOTE. Press 7404A-1 CLEAR and SEND/READY buttons.	Lamps 8 thru 10 out, disregard 11, 12 out, 13 lit, disregard 14, 15 thru 17 out, 18 lit, 19 out, disregard others.	Same as step g.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. (Cont)	w. Set 7404A-1 switches 11, 14, 18, 19, 21, 25, 27, 29, and 30 up; and set the others (between 6 and 31) down. Press SEND/READY button.	651S-1/1A frequency should go to 12.3456 MHz. 7404A-1 lamp 8 lit, 9 and 10 out, 11 lit, 12 and 13 out, 14 lit, 15 thru 17 out, 18 and 19 lit, 20 out, 21 lit, 22 thru 24 out, 25 lit, 26 out, 27 lit, 28 out, 29 and 30 lit, and 31 out.	Same as step g.
	x. Set 7404A-1 switches 6 through 31 down except for 7, 8, and 29. Press SEND/READY pushbuttons.	Lamps 8 thru 12 out, 13 lit, disregard 14, 15 thru 17 out, 18 lit, 19 out, 20 and 21 lit, 22 thru 24 out, 25 lit, 26 out, 27 lit, 28 out, 29 and 30 lit, and 31 out.	Same as step g.
17. Optional remote control, control operation (Cont)	a. Connect FM signal generator through an 80-dB pad plus the 6-dB pad to one-half of T-connector, connect frequency counter to other half of T-connector, and connect T-connector to ANT jack. b. Leave 7404A-1 and speaker connected as in test 16, step a. c. Set FM generator for 10.0000 MHz with 1.0-volt output. Set for nominal deviation to produce audio. d. Set 651S-1/1A controls as follows: POWER ON BFO FIXED METER RF AGC FAST CONTROL REMOTE VBFO Center RF GAIN Max cw AF GAIN 1/4 full SQUELCH (optional) OFF		

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	e. Set 7404A-1 front panel controls as follows: POWER ON PARITY MODE SENSED RETRANSMIT OFF MODE FDX ADDRESS LENGTH 5 BIT PARITY ENCODE MANUAL		
	f. Set the 7404A-1 rear panel controls as follows: Function LCU Sine/logic SINE		
	g. Set 7404A-1 control word switches 0 thru 4 to logic 1 (up) and switch 5 to logic 0 (down) for all tests.		
	h. Press 7404A-1 CLEAR pushbuttons and set switch 11 up. Set all others (6 thru 31) down. Press SEND/READY button. Set switch 11 down and set switches 7, 10, 22, 27, and 29 up only. Press SEND/READY button. Set switches 7, 10, 22, 27, and 29 down. Set switches 6, 28, 29, 30, and 31 up only. Press SEND/READY button. Determine that 651S-1/1A is functioning in FM mode at 10 MHz, with a bandwidth of 6 kHz.	Functioning properly.	Repeat test. Test card A8 or A9 using table 11 or 12.
	i. Set 7404A-1 switches 6 thru 31 down, and set switch 11 back up. Press SEND/READY pushbutton. Set switch 11 down and set switches 7, 10, 23, 27, and 29 up only. Press SEND/READY button. Determine that 651S-1/1A is functioning in FM mode at 10 MHz with a bandwidth of 16 kHz.	Functioning properly.	Same as step h.
	j. Connect an hf signal generator through a 6-dB pad to the ANT jack. Set it for 10.0000-MHz output at 100 μV modulated 30% at 1 kHz.		
(Cont)	k. (Perform only if optional filter card that provides 3-kHz bandwidth is installed.) Set 7404A-1 switches 6 thru 31 down, and set switch 11 back up. Press SEND/READY button. Set switch 11 down, and set switches 7, 11,	Functioning properly.	Same as step h.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	22, 26, and 29 up only. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in AM mode at 10 MHz, with a bandwidth of 3 kHz.		
	l. Set 7404A-1 switches 6 thru 31 down. Set switch 11 back up. Press SEND/READY button. Set switches 7, 11, 22, 27, and 29 up only. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in the AM mode at 10 MHz, with a bandwidth of 6 kHz.	Functioning properly.	Same as step h.
	m. Set 7404A-1 switches 6 thru 31 down. Set switch 11 back up. Press SEND/READY button. Set switches 7, 11, 23, 27, and 29 up only. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in the AM mode at 10 MHz, with a bandwidth of 16 kHz.	Functioning properly.	Same as step h.
	n. Turn off signal generator modulation. Set the 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 14, 20, 27 and 29 up. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in the USB mode at 9.9990 MHz. 1000-Hz tone should be heard.	Functioning properly.	Same as step h.
	o. Set 7404A-1 switches 6 thru 31 down. Set switches 11 and 27 up. Press SEND/READY button. Set 11 and 27 down. Set switches 7, 12, 14, 21, 27, and 29 up. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in LSB at 10.0010 MHz. 1000-Hz tone should be heard.	Functioning properly.	Same as step h.
(Cont)	p. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 13, 14, 20, 27, and 29 up. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in ISB (upper channel) at 9.9990 MHz. A 1000-Hz tone should be heard.	Functioning properly.	Same as step h.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	q. Connect distortion analyzer to ISB 600-ohm terminals with a 600-ohm resistor in parallel. Set analyzer to voltmeter function. Set 7404A-1 switches 6 thru 31 down. Set switches 11 and 27 up. Press SEND/READY button. Set 11 and 27 down. Set switches 7, 12, 13, 14, 20, 27, and 29 up. Press SEND/READY button. Determine that 651S-1/1A is functioning properly in ISB (low channel) at 10.0010 MHz. Analyzer should indicate +2 to +4-dBm audio level. Disconnect analyzer.	Functioning properly.	Same as step h.
	r. (Perform this step only if optional CW bandwidth filter card A5A2 is installed.) Set 7404A-1 switches 6 thru 31 down. Set switch 11 up. Press SEND/READY button. Set 11 down. Set switches 7, 12, 15, 19, 24, and 29 up. Press SEND/READY button. Determine that 651S-1/1A is in CW at 10.0000 MHz.	A 500-Hz tone should be heard with a noise band as wide as the optional filter bandwidth.	Same as step h.
	s. Set 7404A-1 switches 6 thru 31 down. Set 11 back up. Press SEND/READY button. Set 11 down. Set switches 7, 12, 15, 22, 24, and 29 up. Press SEND/READY button. Determine that 651S-1/1A is in CW at 10.0000 MHz.	A 500-Hz tone should be heard with a noise band 500 Hz wide. Vbfo equivalent to position 4.	Same as step h.
	t. (Perform this step only if step r was performed.) Set 7404A-1 switches 6 thru 31 down. Set switch 11 up. Press SEND/READY button. Set 11 down. Set switches 7, 12, 15, 22, 25, and 29 up. Press SEND/READY button. Determine that 651S-1/1A is in CW at 10.0000 MHz.	A 500-Hz tone should be heard with a noise band as wide as the optional filter bandwidth.	Same as step h.
(Cont)	u. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 14, 18, 20, 27, and 29 up. Press SEND/READY button. Check for slow AGC release time (1 second) by disconnecting the hf signal generator. Reconnect generator.	Audio should disappear, there should be a 1-second quiet spot, and then background noise should be heard.	Same as step h.

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	v. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 14, 20, 27, and 29 up. Press SEND/READY button. Check for fast AGC release time (0.1 second) by disconnecting hf signal generator. Reconnect generator.	Audio should disappear and background noise should be present in 0.1 second.	Same as step h.
	w. Connect distortion analyzer to STD 600-ohm terminals with 600-ohm resistor in parallel. Set to voltmeter function. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 14, 20, 27, 28, and 29 up. Press SEND/READY button. Check for no AGC action by varying signal generator output level from 0 to 20 μV.	Audio output should rise linearly. If AGC is operating, the audio would flatten out above approximately 1 μV.	Same as step h.
	x. VBFO Check		
	(1) Connect one tone of the 2-tone generator to the ANT jack. Set it to 10.0000 MHz at 1 μV. Connect frequency counter to the 651S-1/1A SPKR jack. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 16, 20, 27, and 29 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 6, 28, 29, 30, and 31 up. Press SEND/READY button. Check audio frequency.	1060 ±6 Hz.	Test DCFE A8 using table 11.
	(2) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 27, 28, 29, 30, and 31 up. Press SEND/READY button. Check audio frequency.	1050 ±5 Hz.	Same as step x.(1).
	(3) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 26, 28, 29, 30, and 31 up. Press SEND/READY button. Check audio frequency.	1040 ±5 Hz.	Same as step x.(1).
	(4) Set 7404A-1 switches 6 thru 31 down. Set switches 6 and 26 thru 31 up. Press SEND/READY button. Check audio frequency.	1030 ±4 Hz.	Same as step x.(1).

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	(5) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, and 28 thru 31 up. Press SEND/READY button. Check audio frequency.	1020 ±4 Hz.	Same as step x.(1).
	(6) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, and 27 thru 31 up. Press SEND/READY button. Check audio frequency.	1010 ±3 Hz.	Same as step x.(1).
	(7) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 28 thru 31 up. Press SEND/READY button. Check audio frequency.	1000 ±3 Hz.	Same as step x.(1).
	(8) Set 7404A-1 switches 6 thru 31 down. Set switches 6 and 25 thru 31 up. Press SEND/READY button. Check audio frequency.	990 ±3 Hz.	Same as step x.(1).
	(9) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 24, and 28 thru 31 up. Press SEND/READY button. Check audio frequency.	980 ±4 Hz.	Same as step x.(1).
	(10) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 24, and 27 thru 31 up. Press SEND/READY button. Check audio frequency.	970 ±4 Hz.	Same as step x.(1).
	(11) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 24, 26, and 28 thru 31 up. Press SEND/READY button. Check audio frequency.	960 ±5 Hz.	Same as step x.(1).
	(12) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 24, and 26 thru 31 up. Press SEND/READY button. Check audio frequency.	950 ±5 Hz.	Same as step x.(1).
(Cont)	(13) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 24, 25, and 28 thru 31 up. Press SEND/READY button. Check audio frequency.	940 ±6 Hz.	Same as step x.(1).

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	y. Perform the following steps only if DCFE card A8 is jumpered for rf gain:		
	(1) Set the signal generator for CW at 10.0000 MHz with 1-μV output. Monitor STD 600-ohm audio output level with distortion analyzer. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 14, 20, 27, 28, and 29 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 6, 25, 26, and 28 thru 31 up. Press SEND/READY button. Note audio output level for reference.	Reference audio level.	
	(2) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 28 thru 30 up. Press SEND/READY button. Vary signal generator level to produce audio reference. Record dB relationship to 1 μV.	+6 dB nom.	Test DCFE card A8 using table 11.
	(3) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, 29, and 31 up. Press SEND/READY button. Again produce audio reference. Record dB relationship.	+6 dB nom.	Same as step y.(2).
	(4) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, and 29 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(5) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, 30, and 31 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(6) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, and 30 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
(Cont)	(7) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, and 31 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).

Table 2. Overall Performance Test Procedures (Cont).

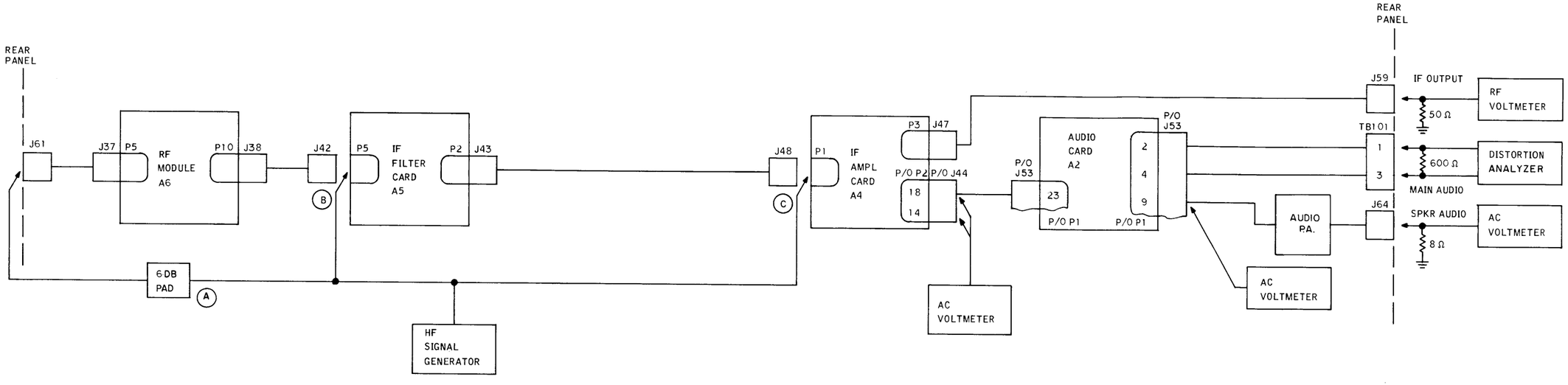
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	(8) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 28 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(9) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 29 thru 31 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(10) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 29, and 30 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(11) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 29, and 31 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(12) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 29 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(13) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 30, and 31 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(14) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 30 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
	(15) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 31 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).
(Cont)	(16) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, and 26 up. Press SEND/READY button. Record dB change to produce reference.	+6 dB nom.	Same as step y.(2).

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	z. Perform the following steps only if DCFE card A8 is jumpered for squelch:		
	(1) Set signal generator to CW at 10.0000 MHz. Connect speaker to 651S-1/1A. Set 7404A-1 switches 6 thru 31 down. Set switches 12, 15, 16, 19, 20, 23, 24, and 27 up. Press SEND/READY button. Set switches 6 thru 31 down. Set switches 7, 12, 14, 17, 20, 27, 28, and 29 up. Set switches 6 thru 31 down. Set switches 6, 25, 26, 28, 29, 30, and 31 up. Press SEND/READY button. Find signal generator output level that just breaks squelch to produce audio.	0 dB ref.	Test card A8. Normal setup for squelch operation is 1-dB increment. This can be varied by the program.
	(2) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, 29, and 30 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
	(3) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, 29, and 31 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
	(4) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, and 29 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
	(5) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, 30, and 31 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
	(6) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, and 30 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
(Cont)	(7) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, 28, and 31 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).

Table 2. Overall Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
17. (Cont)	(8) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 28 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
	(9) Set 7404A-1 switches 6 thru 31 down. Set switches 6, 25, 26, and 29 thru 31 up. Press SEND/READY button. Record level to break squelch.	+1 dB nom.	Same as step z.(1).
18. Abnormal SSB gain card isolation. (Do not perform this test unless some previous test has failed.)	a. If gain is abnormal, the defective subassembly can be isolated using the following steps. Refer to figure 5 for a block diagram of the procedure.		
	b. Extend card A5. Disconnect extender coaxial connector from A5P5. Connect the hf signal generator to A5P5 using BNC to subminiax adapter cable. Connect the distortion analyzer to the AUDIO LINES STD 600-ohm terminals with a 600-ohm resistor in parallel. Use distortion analyzer METER input.		
	c. Set 651S-1/1A to SSB, BANDWIDTH to 2.7U, at 9.9990 MHz (or 2.7L at 10.0010 MHz), fixed bfo, fast AGC, maximum RF GAIN, maximum AF GAIN.		
	d. Set the signal generator for 5-μV output, at 10.35 MHz. Peak the audio with the signal generator frequency.	Approx 0 dBm.	If abnormal, rf module A6 is good; proceed to next step. If normal, rf module is bad; proceed to table 8.
	e. Check level at STD IF output jack with rf voltmeter (using 50-ohm probe).	Approx 50 mV.	Same as step d.
	f. Connect the 8-ohm load resistor with speaker cable to the SPKR 8 OHM jack. Measure audio voltage with distortion analyzer.	Approx 2.85 V (1 watt).	Same as step d.
	g. Reinstall A5. Extend A4. Disconnect extender coax from A4P1. Connect signal generator to A4P1 and set it for 27-μV output at 450 kHz. Repeat measurements of steps d, e, and f.	Same as steps d, e, and f.	If abnormal, if filter card A5 is good; proceed to next step. If normal, if filter card A5 is bad; test using table 7.
	h. Measure audio level at A4P2-18 with digital voltmeter ac probe.	Approx 12 mVrms.	If abnormal, if ampl card A4 bad; proceed to table 6. If normal, proceed to step i.
	i. Measure audio level at A2P1-9 with digital voltmeter ac probe.	Approx 200 mVrms.	If abnormal, audio card A2 bad; proceed to table 4. If normal, and speaker audio level abnormal, audio power amplifier on chassis is bad; repair.



FOR GAIN CARD/ASSY ISOLATION, THE INJECTIONS TO EQUAL AGC THRESHOLD (1 UV, 10.0000 MHZ) AT POINT (A) ARE:

POINT (B) 5UV AT 10.35 MHZ

POINT (C) 30UV AT 450 KHZ

FOR SENSITIVITY CARD/ASSY ISOLATION, THE INJECTIONS TO EQUAL 0.4 UV AT 10 MHZ AT POINT (A) ARE:

POINT (B) 0.7 UV AT 10.35 MHZ

POINT (C) 0.32 UV AT 450 KHZ

FOR LARGE SIGNAL GAIN CARD/ASSY ISOLATION, THE INJECTIONS TO EQUAL 0.1 V AT 10 MHZ AT POINT (A) ARE:

POINT (B) 1.5 MV AT 10.35 MHZ

POINT (C) 5.8 MV AT 450 KHZ

REFER TO THE TEST PROCEDURE FOR THE OUTPUT LEVELS AT THE POINTS INDICATED.

TP2-8102-014

Card Isolation Tests, Test Setup Block Diagram
Figure 5

Table 8. Power Supply Regulator Card A1, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Output voltage measurements	a. Extend regulator card A1. Connect the 651S-1 to primary power and set the POWER switch to OPER.		
	b. Measure the dc level at the following pins of A1P1:		
	3, 4, 9, 10	+5.0 to +5.2 Vdc.	Select new A1R16. Check +5.1-Vdc regulator circuit. If pins 3 and 4 only are incorrect, check enable circuit from A1P1-38 to relay A1K2.
	5, 6, 13, 14	-14.7 to -15.3 Vdc.	Select new A1R6. Check -15-Vdc regulator circuit. If pins 13 and 14 only are incorrect, check enable circuit from A1P1-38 to relay A1K2.
	23, 24, 29, 30,	+14.7 to +15.3 Vdc.	Select new A1R4. Check +15-Vdc regulator circuit. If pins 23 and 24 only are incorrect, check enable circuit from A1P1-38 to relay A1K1.
	33, 35, 36	+23.0 to +25.0 Vdc.	Check +25-Vdc regulator circuit. Check enable circuit from A1P1-38 to relay A1K1.
2. Performance monitor	a. Measure the dc level at performance monitor output pin A1P1-48.	NMT +0.5 Vdc.	Check gates U4A and U4B and associated circuits.
3. Blanking circuit	a. Rapidly rotate the 100-Hz tuning knob and measure the dc level at the following pins on A1P1:		
	71	NMT +1.0 Vdc while tuning.	Check blanking circuit from A1P1-69 to outputs A1P1-71 and A1P1-73.
	73	NLT +4.5 Vdc while tuning.	
	b. Select any operating frequency and measure the dc level at the following pins on A1P1:		
	71	NLT +1.0 Vdc.	Check blanking circuits from A1P1-69 to outputs A1P1-71 and A1P1-73.
	73	NMT +0.5 Vdc.	

Table 4. Audio Card A2, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Dc voltages	a. Extend audio card A2. Connect the primary power and set the POWER switch to OPER. b. Measure the dc level at the following test points: ON 778-2948-002,-004 / ON 778-2948-003,-005 A2J6 / A2J1-2	+11 ±1 Vdc.	A2VR5 or A2R83.
	A2J1 / A2J1-3	-5 ±0.5 Vdc.	A2VR1 or A2R1.
2. Af gain	a. Remove if amplifier card A4. Set MODE switch to SSB. Jumper A2P1 pins 23, 30, and 44. Connect a 27-kΩ resistor to a 2.2-kΩ resistor. Connect the free end of the 27-kΩ resistor to the high side of the audio oscillator output and the free end of the 2.2-kΩ resistor to the low side of the audio oscillator output (grounded). b. Connect a 600-ohm load resistor across the AUDIO LINES STD terminals and ground one side. Connect the meter portion of the distortion analyzer to the same points (make sure the low side of the meter input is the grounded side on the terminals). c. Set the audio oscillator for 17-mV (at the junction of the two resistors) output at 1 kHz. Connect junction to A2P1-23. d. Note the audio output level.	0 dBm.	Adjust A2R70.
(Cont)	e. Set the MODE and BANDWIDTH switches to the positions listed below and measure the audio output at each: MODE / BANDWIDTH FM / 6	0 ±1 dBm.	A2Q7, Q8, Q13 and Q14, and associated circuits.
	FM / 16	-6 ±1 dBm.	
	AM / If installed, 3	0 ±1 dBm.	A2Q9, Q10, and associated circuits.
	AM / 6	0 ±1 dBm.	
	AM / 16	-6 ±1 dBm.	
	f. Connect a 10-kΩ resistor from A2P1 pin 9 to ground and connect the audio meter across the resistor.		

Table 4. Audio Card A2, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	g. Measure the audio level in dBm at each of the following modes. MODE — BANDWIDTH SSB — 2.7U CW — If installed, .2	 -10 ±1.5 dBm. -10 ±1.5 dBm.	
3. Performance and af level monitors	a. Return oscillator frequency to 1 kHz. Adjust the oscillator output level for 0 dBm on the audio voltmeter. b. Measure the dc level at audio performance monitor pin A2P1-12. c. Adjust the oscillator output level for -10 dBm on the audio voltmeter and measure the dc level at pin A2P1-12. d. Readjust the oscillator output level for 0 dBm on the audio voltmeter. Set front panel METER switch to LINE. Check indication on front panel meter.	 NMT +0.5 Vdc. NLT +4.0 Vdc. 0 dBm ±1.3 dB.	 Check A2Q16, Q17, Q19, and associated circuits. Check A2Q16, Q17, Q19, and associated circuits. Check A2R91 and wiring to A2P1-6.
4. Distortion	a. With oscillator at 1 kHz, adjust the output level for 0 dBm on the audio voltmeter. b. Connect the distortion portion of the distortion analyzer to the 600-ohm STD AUDIO LINES terminals. Measure and record the total harmonic distortion. c. Adjust oscillator output level for +6 dBm on the audio voltmeter. Measure and record the total harmonic distortion.	 NMT 1.0%. NMT 1.0%.	
5. Squelch (CPN 778-2948-002; -004 only) (Cont)	a. Adjust oscillator at 1 kHz for 0 dBm on audio voltmeter. Ensure SQUELCH switch is in OFF. b. Connect audio voltmeter to the squelch low-channel test point A2J2 and vary the oscillator frequency until the voltmeter reads a maximum. Record frequency and voltage. c. Connect the audio voltmeter to the squelch high-channel test point A2J3 and vary the oscillator frequency for a voltage maximum. Record the frequency and voltage.	 650 ±100 Hz at NLT 750 mV. 2700 ±300 Hz at one half the voltage for the low channel.	 Check low-channel circuits and A2U1A. Check high-channel circuits and A2U1B. Adjust A2R27 for voltage level.

Table 4. Audio Card A2, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	d. Connect the audio voltmeter to the 600-ohm STD AUDIO LINES terminals. Adjust the oscillator for 1 kHz and 0 dBm on the audio voltmeter.		
	e. Set the front panel SQUELCH switch to position 7 (OFF is position 0, position 1 is next step clockwise).		
	f. Increase the oscillator frequency until the audio output suddenly drops. Record the level on the audio voltmeter.	NMT -40 dBm.	Check squelch gate A2Q15. Check A2U2 and circuits to A2Q15.
	g. Decrease frequency slowly until the audio level jumps back to 0 dBm. Increase frequency quickly to beyond the squelching frequency and note the time delay before the audio drops out.	1 to 3 seconds.	Check A2C46, R97.
	h. Set front panel SQUELCH switch to OFF.	Audio output comes back up.	Check squelch control circuits from A2P1-32 to A2Q15.
	i. Rapidly rotate the 100-Hz tuning knob.	Audio output drops out while tuning.	Check audio blanking circuits from A2P1-11 A2Q15.
	j. Disconnect test equipment.		
6. Vbfo	a. Set POWER switch to OFF. Remove the cover from the vbfo subassembly. Terminate A2P2 with a 150-ohm load (resistor). Connect oscilloscope, counter, and rf voltmeter with high-impedance probe to bfo output jack A2P2. ***Note*** Steps b and c apply to -002 and -003 (effectivity up to CI-72353) only.		
	b. Set front panel BFO switch to VAR, MODE switch to CW, and BANDWIDTH to .5. Check waveform.	Clean sinusoid at approximately 450 kHz.	Check filter circuit A2A1T1, -T2, -C42, -C43, and -C44.
	c. Set MODE switch to SSB, BANDWIDTH to 2.7U, and check waveform.	Clean sinusoid at approximately 450 kHz.	Check filter circuit A2A1T1, -T2, -C42, -C43, and -C44.
(Cont)	d. Return MODE switch to CW, BANDWIDTH to desired bandwidth, and set VBFO switch to position 7 (center). Check output frequency.	450.000 ±.010 kHz.	Adjust A2R34.

Table 4. Audio Card A2, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. (Cont)	e. Check output level on rf voltmeter.	300 ±30 mV.	On -002 and -003 (effectivity up to CI-72353) adjust A2A1T1 and A2A1T2 for maximum level on rf voltmeter. If level is still not within specification, select new A2A1R32 (larger A2A1R32 decreases output level). On -004 and -003, -005 (effectivity CI-72373) select new A2A1R32.
	f. Set MODE switch to SSB, BANDWIDTH to 2.7U, and check rf voltmeter indication.	300 ±30 mV.	Same as step e.
	g. Set VBFO switch to 13 (cw). Set MODE switch to CW, and BANDWIDTH to desired bandwidth. Measure output frequency at A2P2.	451 kHz.	Check crystal oscillator circuits. Check mixer A2A1U1 and associated circuits.
	h. Set BFO switch to FIXED and measure output frequency at A2P2.	450,000 kHz.	Check diodes A2A1CR7 and -CR8.
	i. Reinstall cover on the vbfo subassembly. Set BFO switch to VAR and VBFO switch to position 7 (center). Measure output frequency.	450.000 ±.005 kHz.	Adjust A2R34.
	j. Measure output frequencies at the following VBFO switch positions: 1 (ccw) 13 (cw)	NMT 449.100 kHz. NLT 450.900 kHz.	Check crystal oscillator circuits and mixer A2A1U1 circuits.
	k. Set MODE switch to SSB, BANDWIDTH to 2.7U, and VBFO switch to position 7 (center). Measure output frequency.	450.000 kHz.	Adjust A2R43.
	l. Set VBFO switch to position 13 (cw). Measure output frequency.	450.047 to 450.063 kHz.	Adjust A2R41.
	m. Repeat step k and l until both frequencies are correct.		
	n. Set VBFO switch to position 1 (ccw). Measure output frequency.	449.937 to 449.943 kHz.	Select new A2C3 (larger A2C3 lowers minimum frequency).
	o. If capacitor A2C3 was changed in step m, repeat steps k through n.		

Table 5. ISB Amplifier Card A3, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. If gain adjust	a. Extend ISB amplifier card A3. Connect primary power and set the POWER switch to OPER. Set the RF GAIN control fully clockwise, the MODE switch to ISB, the AGC switch to FAST, the SQUELCH switch to OFF, and the BFO switch to FIXED.		
	b. Disconnect the extender coax from A3P1 and connect the hf signal generator (no 6-dB pad) to A3P1 using a BNC to subminiax adapter cable (figure 1). Set it to 451 kHz at 27 μV.		
	c. Connect the rf voltmeter to the ISB IF output jack, set A3R57 fully clockwise, and peak the output with A3T1. Note the rf voltmeter indication.	50 mV.	Adjust A3R7.
2. ISB audio output	a. Connect a 600-ohm load resistor and the meter portion of the distortion analyzer to the AUDIO LINES ISB 600-ohm terminals.		
	b. Peak the audio indication using A3T2. Note the final level.	0 ±1 dBm.	Adjust A3R92.
	c. Increase the signal generator output level to 10 mV and note the rise in audio output.	4 to 5-dB rise over step b.	Adjust A3R57.
3. AGC operation	a. Set the signal generator output level to 0. Slowly increase the level to 27 μV and monitor the audio. Continue to increase the output up to 10 mV.	Audio level increases rapidly with up to 27 μV in; then the increase slows considerably. Final level at 10 mV is NMT 5 dB above that for 27 μV in.	Repeat steps 1, 2, and 3 until the following requirements are met: AGC threshold, 25 to 30 μV; audio rise, 5 to 6 dB; and if output, 40 to 60 mV.
4. If gain reduction	a. Set the signal generator for 27 μV out. Note the rf voltmeter indication for reference.		
	b. Set the AGC switch to off (center position) and set the RF GAIN control fully counterclockwise.		
	c. Increase the signal input until the reference rf voltmeter indication is reached, and note the increase required.	85 to 95 dB.	

Table 5. ISB Amplifier Card A3, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Audio distortion	a. Connect the 2-tone generator to the 2-tone adapter (figure 2). Set the tones for 450.6 and 451.6 kHz, each at 2.5 mV (at the adapter output). Connect the adapter to A3P1. b. Connect the wave analyzer to the 600-ohm AUDIO LINES ISB terminals (with 600-ohm load) and measure the distortion products at the following frequencies: F1 (600 Hz) 2F2-F1 (2600 Hz)	 0-dB reference. NLT 40 dB down.	

Table 6. IF Amplifier Card A4, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. If gain adjust	a. Extend if amplifier card A4. Connect the 651S-1/1A to primary power and set the POWER switch to OPER. Set the RF GAIN control fully clockwise, the MODE switch to SSB, BANDWIDTH to 2.7U, and the AGC switch to off (center) position.		
	b. Disconnect the extender coax from A4P1 and connect the signal generator (no 6-dB pad) at 451 kHz, 27 μV to A4P1 using a BNC to subminiax adapter cable (figure 1). Connect an rf voltmeter (with 50-ohm probe) to the STD IF output jack.		
	c. Set A4R61 fully clockwise. Adjust A4T1 for maximum output. Note the rf voltmeter indication.	57 mV.	Adjust A4R6.
	d. Set AGC switch to FAST. Note rf voltmeter indication.	50 mV.	Adjust A4R61.
	e. Repeat procedure as necessary so rf voltmeter indication is 57 ±1 mV with no AGC and 50 ±1 mV with AGC.		
2. AGC control	a. Set AGC switch to FAST. Set the signal generator to 27 μV and note the rf voltmeter indication.	0-dB reference.	Check AGC amplifier circuits.
	b. Set the signal generator to 5-mV output and note the rf voltmeter indication increase.	NMT 5-dB rise.	
3. SSB audio output	a. Set the BFO switch to FIXED. Set the signal generator for 27 μV.		
	b. Connect the meter portion of the distortion analyzer to A4P2-18. Note the indication.	15 to 22 mV.	Adjust A4T3 for maximum output.
4. SSB audio distortion	a. Connect the 2-tone generator through the adapter shown in figure 2. Set the tones for 450.6 kHz and 451.6 kHz, each at 2.5 mV (at the adapter output). Connect the adapter to A4P1, connect the wave analyzer to A4P2-18, and measure the following distortion products: F1 (600 Hz) 2F2-F1 (2600 Hz)	 0-dB reference. NLT 40 dB down.	

Table 6. IF Amplifier Card A4, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. AM audio output	a. Connect the signal generator to A4P1 and set it for 450 kHz at 5-mV modulated 30% at 1000 Hz.		
	b. Set 651S-1/1A to AM mode with a bandwidth of 6 kHz. Measure audio output at A4P2-4.	15 to 25 mV.	Check audio amplifier.
6. FM audio output (-001, -003 only)	a. Set the audio oscillator for 1-V output at 1000 Hz. Connect it to the signal generator external modulation input. Set the signal generator for 450 kHz at 5 mV.		
	b. Set the 651S-1/1A to FM mode with a bandwidth of 6 kHz; measure the audio output at A4P2-21.	2 to 6 mV.	Adjust A4L8 for maximum output.
7. Meter output	a. Set the 651S-1/1A METER switch to RF. Disconnect the audio oscillator. Set the signal generator to 450 kHz at 5 mV. Connect a 205-ohm resistor to A4P2-12 and ground, and measure the dc level.	0.15 V.	Adjust A4R109.
8. If gain reduction	a. Set the signal generator to 450 kHz at 27 μV. Connect the rf voltmeter (with 50-ohm probe) to the STD IF output jack. Set the 651S-1/1A RF GAIN control fully clockwise.		
	b. Note the rf voltmeter indication.	0-dB reference.	
	c. Set the RF GAIN control fully counterclockwise and note the increase of signal generator output necessary to produce the 0-dB reference on the rf voltmeter.	85 to 95 dB.	

Table 7. IF Filter Card A5, Test Procedures.

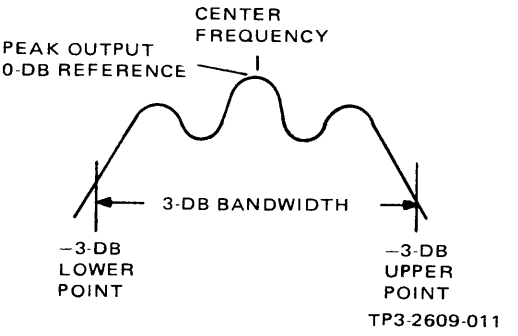
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Gain, standard modes	a. Extend if filter card A5. Connect the primary power and set the 651S-1/1A POWER switch to OPER, BFO switch to FIXED, MODE switch to FM, BANDWIDTH switch to 6, at any frequency. Set the RF GAIN control fully clockwise.		
	b. Connect one tone of the 2-tone generator at 9.9 MHz, 0.6 Vrms to A5P4 using a BNC to subminiax adapter cable. Connect an hf signal generator to A5P5 and set it for 10.35 MHz at 3.0-mV output. Connect an rf voltmeter (with 50-ohm probe) to A5P2.		
	c. Vary the signal generator frequency for a maximum indication on the rf voltmeter indication.	14 to 20 mV.	Adjust A5T1 and A5T2 for maximum output.
	d. Repeat step c for the following modes:		Same as step c.
	MODE / BANDWIDTH		
	FM 16	14 to 20 mV.	
	AM 6	20 to 30 mV.	
	AM 16	15 to 25 mV.	
	SSB 2.7U	15 to 23 mV.	
	SSB 2.7L	15 to 23 mV.	
2. Gain, optional modes	a. Repeat the procedures of step 1 for the following optional modes, if applicable:		Same as step 1.c.
	MODE / BANDWIDTH		
	AM 3	20 to 30 mV.	
	CW 1, 4, WSRT, or WBTV	20 to 30 mV.	
	CW .5, 2, or CW	20 to 30 mV.	
	CW .2, 1, or NSRT	20 to 30 mV.	
	b. Connect the rf voltmeter to A5P1 (ISB if output). Set the MODE switch to ISB and vary the signal generator frequency to obtain the maximum rf voltmeter indication. Note the indication.	17 to 24 mV.	Same as step 1.c.
3. Filter responses, AM, USB, and LSB (Cont)	a. Set the 651S-1/1A to SSB mode with BANDWIDTH at 2.7U and frequency at 450 kHz. Set the signal generator to 451 kHz. Vary frequency slightly to peak output. Increase signal to produce 10 mV at A5P2. Note as 0-dB reference.		

Table 7. IF FILTER Card A5, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	b. Decrease signal generator frequency until output decreases 2-dB from reference bandpass point, lower). Note the frequency.	NMT 450.6 kHz.	
	c. Slowly increase the frequency (starting at 451 kHz) to find upper bandpass as in step b.	NLT 453.05 kHz for upper 2-dB point.	
	d. Refer to figure 6 for bandwidth definitions.		
	e. Set the 651S-1/1A to SSB mode, BANDWIDTH to 2.7L, and repeat steps a through d using the 449 kHz as the 0-dB reference.	NMT 446.95 kHz for the lower bandpass 2-dB point, NLT 449.4 kHz for the upper bandpass 2-dB point.	
	f. Set the 651S-1/1A to AM mode with a 6-kHz bandwidth. Set the signal generator to 450 kHz and record the output level as 0-dB reference.		
	g. Find the 6-dB drop points above and below 450 kHz. Note the frequency at each point. Subtract the frequencies and record the result.	5.25 to 6.75 kHz.	
	h. Refer to figure 6 for AM bandwidth definitions.		
4. Filter responses, AM and CW	a. With the same setup as in step 3, set the signal generator to 10.35 MHz with output to produce 12 mV at the rf voltmeter.		
	b. Set the 651S-1/1A to AM mode and BANDWIDTH to 3 (if AM 3 is installed). Also two bandwidths of AM 3 are possible, 3 or 4 kHz. Sweep the signal generator around 10.35 MHz to find the upper and lower 3-dB down points (bandwidth). Refer to figure 6 for bandwidth definitions.	Bandwidth, 2.7 to 3.3 kHz. Bandwidth, 3.8 to 4.2 kHz.	
	c. Set the 651S-1/1A to CW BANDWIDTH to the appropriate position and sweep the signal generator frequency to find the 3-dB bandwidth as in step b for all CW modes installed. Refer to figure 6. Use enough signal to produce 12-mV out.	***Note*** The total 3-dB bandwidth shall be within 50 percent of the nominal bandwidth. For example, the 500-Hz filter shall have a 3-dB bandwidth of 500 Hz ±250 Hz or from 250 to 750 Hz.	Check appropriate filter.
(Cont)			

Table 7. IF Filter Card A5, Test Procedures (Cont).

TEST	PROCEDURE		NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	BANDWIDTH SWITCH	FILTER	NOMINAL 3-dB BANDWIDTH	
	1st CW position (1, 4, WSRT, or WBTY)	1 kHz	1 kHz	
		1.1 kHz (offset +2 kHz)	1.1 kHz	
		1.1 kHz (offset +2.55 kHz)	1.1 kHz	
		4 kHz	4 kHz	
	2nd CW position (.5, 2, or CW)	500 Hz	500 Hz	
		2 kHz	2 kHz	
	3rd CW position (.2, 1, or NSRT)	200 Hz	200 Hz	
		370 Hz (offset +2 kHz)	370 Hz	
		1.1 kHz	1.1 kHz	



IF Filter Card A5, Filter Response
Figure 6

Table 8. RF Module A6, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Passband variations	a. Extend rf module A6 on its module extender. Connect the 651S-1/1A to primary power and set POWER switch to OPER. Set 651S-1/1A MODE switch to SSB, BANDWIDTH switch to 2.7U, AGC switch to off (center) position, and RF GAIN control fully clockwise. Tune the 651S-1/1A to 10.0 MHz. b. Connect the rf voltmeter (with 50-ohm probe) to the IF OUTPUT jack (J59). Connect the signal generator (through a 6-dB pad) to ANT jack (J61); set it for 10.0 MHz at 2 μV and tune for zero beat. c. Set 651S-1/1A MODE switch to AM, BANDWIDTH to 16, and note if output level. d. Tune the 651S-1/1A ±3 kHz and measure the if output variation in dB.	NMT 1 dB.	Perform voltage checks and adjustment procedures, steps 6 through 11.
2. Sensitivity (Cont)	***Note*** The 651S-1/1A 600-ohm audio output (TB101, terminals 1 and 3) must be terminated in a 600-ohm resistive load when performing tests on rf module A6. a. Connect an audio vtvm to the 600-ohm audio output (TB101, terminals 1 and 3) on the 651S-1/1A. b. Set 651S-1/1A MODE to SSB and BANDWIDTH to 2.7U. c. Measure sensitivity (snr) at the following frequencies and input signal levels:		Perform voltage checks adjustment procedures, steps 6 through 11.

FREQ		INPUT SIG LVL	SNR
100 kHz	(790-1048-010, -021 only)	2.5 μV	NLT 10 dB
300 kHz	(790-1048-010, -021 only)	2.5 μV	NLT 10 dB
550 kHz	(790-1048-010, -021 only)	2.5 μV	NLT 10 dB
350 kHz	(790-1048-008, -020 only)	2.5 μV	NLT 10 dB
1350 kHz		2.5 μV	NLT 10 dB
2.0 MHz		0.7 μV	NLT 10 dB
3.0 MHz		0.7 μV	NLT 10 dB
4.0 MHz		0.7 μV	NLT 10 dB
6.0 MHz		0.7 μV	NLT 10 dB

Table 8. RF Module A6, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	FREQ / INPUT SIG LVL / SNR 8.0 MHz / 0.7 μV / NLT 10 dB 12 MHz / 0.7 μV / NLT 10 dB 16 MHz / 0.7 μV / NLT 10 dB 24 MHz / 0.7 μV / NLT 10 dB 29.999 MHz / 0.7 μV / NLT 10 dB d. For rf module A6 790-1048-010 or -021, connect equipment as shown in figure 7. **Note** Assure that the jumper on vlf filter FL601 is connected for 50-ohm input (terminals 2 and 3). e. Measure sensitivity at the following frequencies and input signal levels: FREQ / INPUT SIG LVL / SNR 12 kHz / 2.5 μV / NLT 10 dB 50 kHz / 2.5 μV / NLT 10 dB f. Connect the jumper on FL601 for 1000-ohm input (terminals 1 and 3) and connect the 1000-ohm resistor as shown with dashed lines in figure 7. g. Measure sensitivity at 12 kHz with signal generator output level at 6 volts.	Snr: NLT 10 dB.	Perform voltage checks and adjustment procedures, steps 6 through 11.
	Note Restrap FL601 for 50-ohm input (normal).		
3. Internal spurious level	a. Connect rf signal generator (through a 6-dB pad) to the ANT jack and an audio vtvm to the 600-ohm audio output on the 651S-1/1A. b. Set signal generator output level to zero, the 651S-1/1A to 20.7005 MHz, MODE to SSB, and BANDWIDTH to 2.7U. c. Note audio output for reference. Detune the 651S-1/1A to 20.6005, set the signal generator to 20.6005 MHz, and increase output level to produce the same audio output as noted for reference. Note signal generator output level.	Signal generator output level NMT 10 μV.	Perform voltage checks and adjustment procedures, steps 6 through 11.

Table 8. RF Module A6, Test Procedures (Cont).

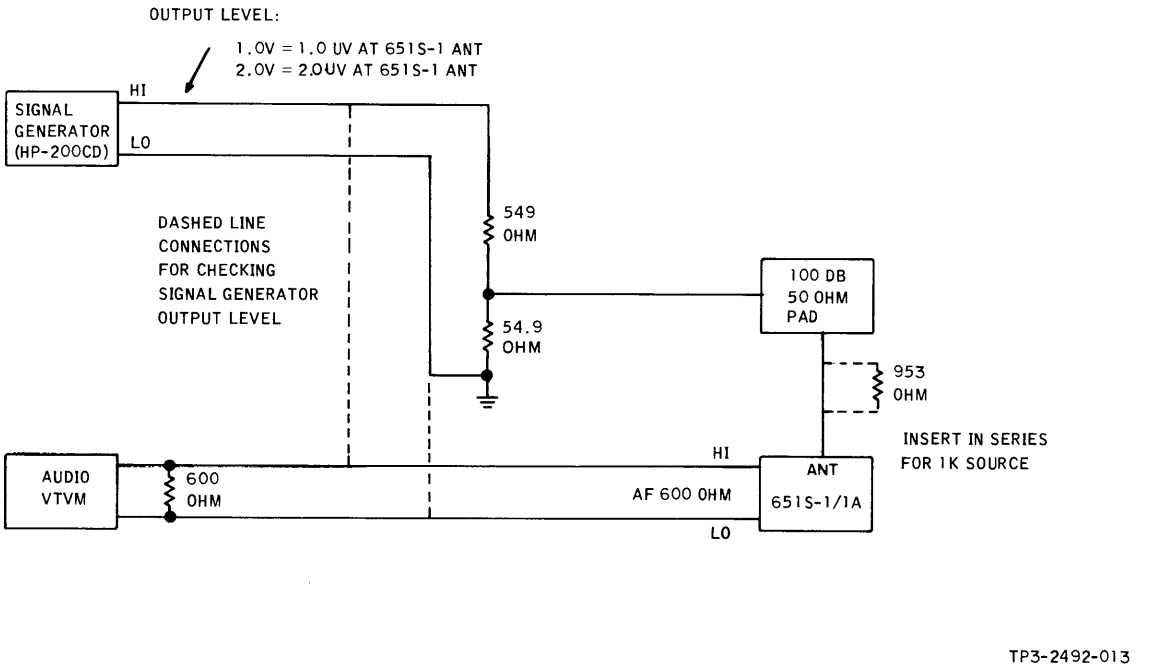
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Gain	a. Set signal generator for 28.0000 MHz at 1 μV.		
	b. Set 651S-1/1A to 28.0000 MHz. Vary frequency for peak audio out and measure audio output.	790-1048-008, -010: +0.5 to -0.5 dBm. 790-1048-020,-021: +2.5 to +3.5 dBm.	Adjust A6R31 (figure 8).
	c. For rf module A6 790-1048-010, set signal generator to 250 kHz at 1 μV and 651S-1/1A to 250 kHz. Vary frequency to peak audio out and measure audio output.	-2 to +2 dBm.	Perform voltage checks and adjustment procedures, steps 6 through 11.
5. AGC	a. Set the 651S-1/1A and the signal generator to 10.0 MHz. Vary frequency slightly to peak audio, and adjust signal generator output level to produce 0-dBm audio output.		
	b. Connect a variable dc source to the AGC lead (green) on the rf module, (figure 8), and adjust for +2.2 Vdc.		
	c. Readjust signal generator output level for a 0-dBm audio output and note the increase in dB.	45 to 55 dB.	Check AGC diodes A6CR1 through A6CR4.
	d. For rf module A6 790-1048-010 or -021, repeat steps a, b, and c with signal generator and 651S-1/1A set to 250 kHz.	45 to 55 dB.	Check AGC diodes A6CR1 through A6CR4.
6. Injection voltage (figure 8)	***Note*** Tests (adjustments) 6 through 11 not required if 651S-1/1A successfully passed tests 1 through 5.		
	a. Set the 651S-1/1A MODE to SSB, BANDWIDTH to 2.7U, and frequency to 10.0 MHz.		
	Note Do steps b and c for A6 790-1048-008 and -010. Do only step c for A6 790-1048-020 and -021.		
	b. With rf voltmeter (use hi-z probe with a very short ground lead), measure injection voltage at the source lead of U1 (figure 8).	2.25 to 2.50 Vac.	Change test select resistor A6R20.
	c. Measure injection voltage at the source of Q1 or Q2.	1.80 to 2.50 Vac.	Change test select resistor A6R25.

Table 8. RF Module A6, Test Procedures (Cont).

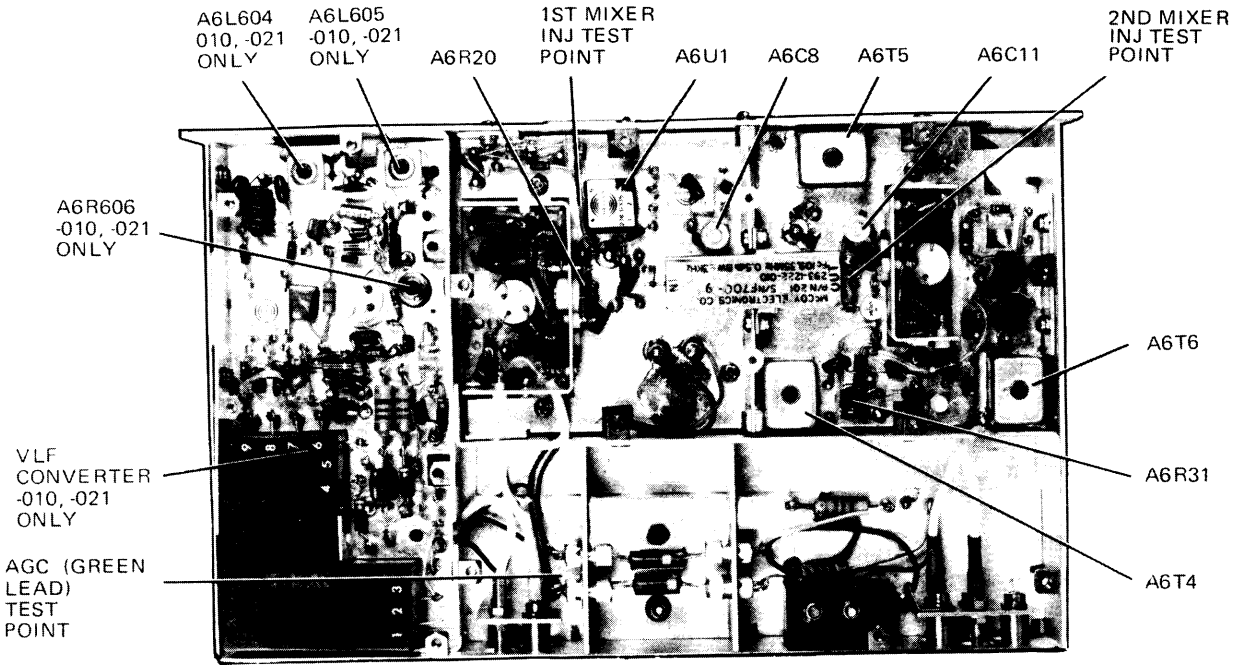
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
7. Initial adjustments (figure 8)	a. Set A6R31 fully cw. Set 651S-1/1A to 10 MHz and signal generator to 9.9990 MHz at 1 μV. (Vary frequency slightly to peak audio out.)		
	b. Adjust A6C8, A6C11, and A6T4 for maximum audio output.	Peak adjustment possible.	Peak adjustment not possible. Check Q1, Q2, Q3, U1, and associated circuits.
8. 9.45-MHz trap adjustment (figure 8) (All -008 and -010 part numbers and the -020 part number if T6 is installed.)	a. Set 651S-1/1A to 9.1 MHz. Set signal generator output level for 1 μV and frequency to 9.1 MHz. Adjust slightly to peak audio output.		
	b. Set 651S-1/1A to 10 MHz. Increase signal generator output level to 0.1 volt and adjust frequency slightly to peak audio output.		
	c. Adjust A6T6 for a null in the audio output.	Null possible.	Null not possible. Check Q3, T6, and associated components.
	d. Return 651S-1/1A to 9.1 MHz. Set signal generator output level to 1 μV and adjust frequency to peak audio output.		
	e. Adjust A6T4 and A6T5 for maximum audio output.		
	f. Repeat steps b through e until no further improvement is possible.		
	g. Note the audio output with the 651S-1/1A and signal generator at 9.1 MHz. Note signal generator output level in dB.	0-dB reference.	
	h. Set the 651S-1/1A to 10 MHz and increase the signal generator output level until audio output is the same as 0-dB reference in step g. Compute the dB change in the signal generator output level from step g.	dB change in the signal generator output level; NLT 85 dB.	
9. Gain adjustment (figure 8)	a. Set 651S-1/1A to 28.0000 MHz. Set signal generator for 28.0000 MHz at 1 μV. Vary frequency slightly for peak audio output.		
	b. Adjust A6R31 as follows:		
	For 790-1048-008, -010: 0-dBm audio output.	0 dBm	
	For 790-1048-020, -021: +3 dBm audio output.	+3 dBm.	

Table 8. RF Module A6, Test Procedures (Cont).

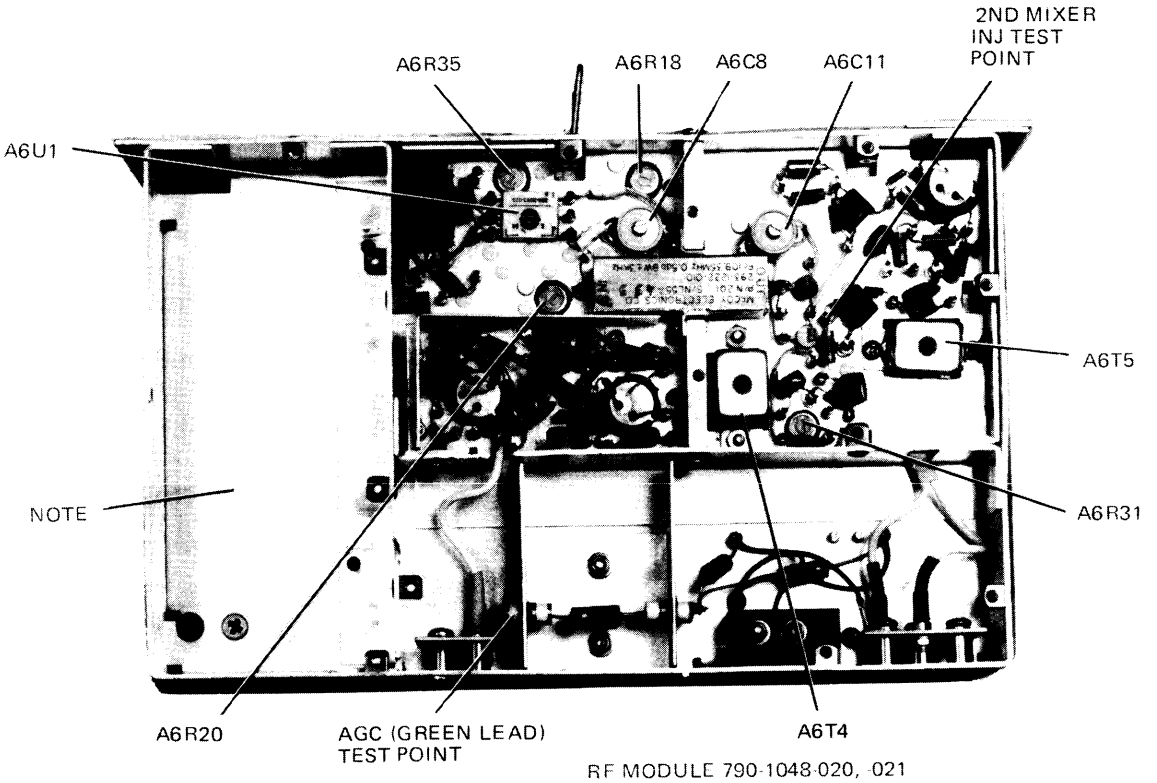
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
10. Vlf converter adjustment (790-1048-010, -021) (figure 8)	a. Set the 651S-1/1A and signal generator to 250 kHz. Vary frequency slightly to peak audio output. Assure that AGC is off. Adjust the signal generator output level to produce 0-dBm audio output. b. Peak audio output by adjusting A6L604 and A6L605; readjust signal generator output level as necessary to maintain a 0-dBm audio output. c. Set the 651S-1/1A only to 12 kHz. Note audio output noise level. d. Adjust A6R606 for minimum noise output.		
11. First mixer adjustments (790-1048-020, -021) (figure 8)	a. Connect equipment as shown in figure 9. Set 651S-1/1A to 2.0 MHz, and set AGC off. Set signal generator A to 2.026 MHz and signal generator B to 4.027 MHz. b. Adjust A6R18, A6R20, and A6R35 for a minimum in 2nd order distortion level as indicated on the audio output vtvm. c. Set 651S-1/1A to 24.2 MHz, generator A to 8.2 MHz, and generator B to 16.001 MHz. d. Adjust A6R20 for a minimum audio output level. e. Set 651S-1/1A to 7.8 MHz and adjust A6R18 for minimum audio output. f. Set 651S-1/1A to 2.0 MHz, generator A to 2.026 MHz, generator B to 4.027 MHz, and adjust A6R35 for minimum audio output. g. Repeat steps c through f until no further improvement is possible.		
12. Final test	After completion of adjustments, repeat applicable tests (1 through 5).		



RF Module A6 Sensitivity (12-50 kHz), Test Setup
Figure 7



RF MODULE 790-1048-010



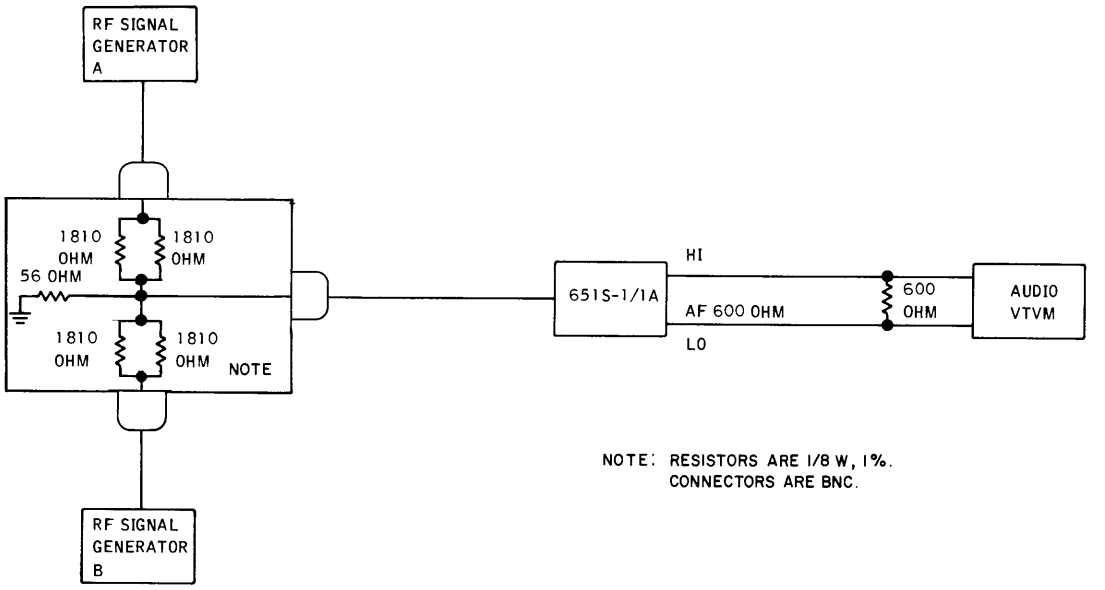
RF MODULE 790-1048-020, -021

NOTE:

REFER TO THE -010 VIEW FOR COMPONENTS LOCATION OF THE VLF CIRCUITS IN THE -021.

TP3-2485-017

RF Module A6, Location of Test Points and Adjustments
Figure 8



RF Module A6 (790-1048-020, -021), Distortion Test Setup
Figure 9

Table 9. Decoder/Driver Card A7, Performance Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Band outputs (778-2928-003 only)	a. Extend card A7 on appropriate card extender. Connect 651S-1/1A to primary power. Set POWER switch to OPER. Measure dc levels at the following pins of A7P1 with the 651S-1/1A set to 400 kHz.		
	62	-15 Vdc nom.	Check Q2 and assoc drivers.
	45	-15 Vdc nom.	Check Q4 and assoc drivers.
	64	-15 Vdc nom.	Check Q6 and assoc drivers.
	72	-15 Vdc nom.	Check Q8 and assoc drivers.
	43	-15 Vdc nom.	Check Q9 and assoc drivers.
	60	-15 Vdc nom.	Check Q10 and assoc drivers.
	44	-15 Vdc nom.	Check Q11 and assoc drivers.
	56	-15 Vdc nom.	Check Q12 and assoc drivers.
	84	-15 Vdc nom.	Check Q13 and assoc drivers.
	86	+5 Vdc nom.	Check Q14 and assoc drivers.
	b. Increase frequency in 20-kHz steps to 540 kHz and measure as in step a at each increment.	Same as step a.	Same as step a.
	c. Set 651S-1/1A to 560 kHz and repeat step a.	All pins in step a -15 Vdc, except 84 is +5 Vdc.	Same as step a.
	d. Measure same points with 20-kHz incremental frequency increase up to 1.980 MHz.	Same as step c.	Same as step a.
	e. Set 651S-1/1A to 2 MHz and repeat step a.	All pins in step a -15 Vdc, except 56 is +5 Vdc.	Same as step a.
	f. Measure same points with 20-kHz incremental frequency increase up to 2.980 MHz.	Same as step e.	Same as step a.
	g. Set 651S-1/1A to 3 MHz and repeat step a.	All pins in step a -15 Vdc, except 44 is +5 Vdc.	Same as step a.
	h. Measure same points with 20-kHz incremental frequency increase up to 3.980 MHz.	Same as step g.	Same as step a.
(Cont)	i. Set 651S-1/1A to 4 MHz and repeat step a.	All pins in step a -15 Vdc, except 60 is +5 Vdc.	Same as step a.

Table 9. Decoder/Driver Card A7, Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	j. Measure same points with 20-kHz incremental frequency increase up to 5.980 MHz.	Same as step i.	Same as step a.
	k. Set 651S-1/1A to 6 MHz and repeat step a.	All pins in step a -15 Vdc, except 43 is +5 Vdc.	Same as step a.
	l. Measure same points with 20-kHz incremental frequency increase up to 7.980 MHz.	Same as step k.	Same as step a.
	m. Set 651S-1/1A to 8 MHz and repeat step a.	All pins in step a -15 Vdc, except 72 is +5 Vdc.	Same as step a.
	n. Measure same points with 20-kHz incremental frequency increase up to 11.980 MHz.	Same as step m.	Same as step a.
	o. Set 651S-1/1A to 12 MHz and repeat step a.	All pins in step a -15 Vdc, except 64 is +5 Vdc.	Same as step a.
	p. Measure same points with 20-kHz incremental frequency increase up to 15.980 MHz.	Same as step o.	Same as step a.
	q. Set 651S-1/1A to 16 MHz and repeat step a.	All pins in step a -15 Vdc, except 45 is +5 Vdc.	Same as step a.
	r. Measure same points with 20-kHz incremental frequency increase up to 23.980 MHz.	Same as step q.	Same as step a.
	s. Set 651S-1/1A to 24 MHz and repeat step a.	All pins in step a -15 Vdc, except 62 is +5 Vdc.	Same as step a.
	t. Measure same points with 20-kHz incremental frequency increase up to 29.980 MHz and at 29.9999 MHz.	Same as step s.	Same as step a.
2. Band outputs (608-9087-001 or 608-9121-001)	a. Extend card A7 on appropriate card extender. Connect 651S-1/1A to primary power. Set POWER switch to OPER. Measure dc levels at the following pins of A7P1 with 651S-1/1A set to 260 kHz:		
	56	-15 Vdc nom.	Check Q2 and assoc drivers.
	84	-15 Vdc nom.	Check Q4 and assoc drivers.
(Cont)	86	+5 Vdc nom.	Check Q3 and assoc drivers.

Table 9. Decoder/Driver Card A7, Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	b. Increase frequency in 20-kHz steps to 540 kHz and measure dc levels, as in step a, at each increment.	Same as step a.	Same as step a.
	c. Set 651S-1/1A to 560 kHz and repeat the dc level measurements in step a.	Pins 56 and 86 at -15-Vdc. Pin 84 at +5 Vdc.	Same as step a.
	d. Increase frequency in 20-kHz steps to 1.980 MHz and repeat dc level measurements at each increment.	Same as step c.	Same as step a.
	e. Set 651S-1/1A to 2.0 MHz and repeat the dc level measurements in step a.	Pins 84 and 86 at -15 Vdc. Pin 56 at +5 Vdc.	Same as step a.
	f. Increase frequency in 20-kHz steps to 29.980 MHz and repeat the dc level measurements at each increment.	Same as step e.	Same as step a.
3. Bcd output (778-2928-003 or 608-9121-001)	a. Set the 651S-1/1A to 20 MHz. Check dc level at A7P1 pins listed:		
	6	+3.2 Vdc nom.	Check flatpacks U1D and U1E, or U4B and U4C.
	4	0 Vdc nom.	Check flatpacks U1A and U1B or U4A and U4F.
	20	0 Vdc nom.	Check flatpacks U3D and U3E or U4D and U4E.
	18	0 Vdc nom.	Check flatpacks U3A and U3B or U5B and U5C.
	10	0 Vdc nom.	Check flatpacks U2A and U2B or U5A and U5F.
	14	0 Vdc nom.	Check flatpacks U2D and U2E or U5D and U5E.
	32	0 Vdc nom.	Check flatpacks U4D and U4E or U8A and U8F.
	23	0 Vdc nom.	Check flatpacks U4A and U4B or U6A and U6F.
	38	0 Vdc nom.	Check flatpacks U5D and U5E or U6D and U6E.
	25	0 Vdc nom.	Check flatpacks U5A and U5B or U8B and U8C.
	36	0 Vdc nom.	Check flatpacks U10D and U10E or U9B and U9C.
	26	0 Vdc nom.	Check flatpacks U10A and U10B or U9A and U9F.
	30	0 Vdc nom.	Check flatpacks U4C and U5C or U9D and U9E.
	b. Set 651S-1/1A to 10 MHz and repeat step a.	All pins in step a 0 Vdc, except 4 is +3.2 Vdc.	Same as step a.
(Cont)	c. Set 651S-1/1A to 8 MHz and repeat step a.	All pins in step a 0 Vdc, except 20 is +3.2 Vdc.	Same as step a.

Table 9. Decoder/Driver Card A7, Performance Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	d. Set 651S-1/1A to 4 MHz and repeat step a.	All pins in step a 0 Vdc, except 18 is +3.2 Vdc.	Same as step a.
	e. Set 651S-1/1A to 2 MHz and repeat step a.	All pins in step a 0 Vdc, except 10 is +3.2 Vdc.	Same as step a.
	f. Set 651S-1/1A to 1 MHz and repeat step a.	All pins in step a 0 Vdc, except 14 is +3.2 Vdc.	Same as step a.
	g. Set 651S-1/1A to 800 kHz and repeat step a.	All pins in step a 0 Vdc, except 32 is +3.2 Vdc.	Same as step a.
	h. Set 651S-1/1A to 400 kHz and repeat step a.	All pins in step a 0 Vdc, except 23 is +3.2 Vdc.	Same as step a.
	i. Set 651S-1/1A to 10.2 MHz and repeat step a.	All pins in step a 0 Vdc, except 4 and 38 are +3.2 Vdc.	Same as step a.
	j. Set 651S-1/1A to 10.1 MHz and repeat step a.	All pins in step a 0 Vdc, except 4 and 25 are +3.2 Vdc.	Same as step a.
	k. Set 651S-1/1A to 10.08 MHz and repeat step a.	All pins in step a 0 Vdc, except 4 and 36 are +3.2 Vdc.	Same as step a.
	l. Set 651S-1/1A to 10.04 MHz and repeat step a.	All pins in step a 0 Vdc, except 4 and 26 are +3.2 Vdc.	Same as step a.
	m. Set 651S-1/1A to 10.02 MHz and repeat step a.	All pins in step a 0 Vdc, except 4 and 30 are +3.2 Vdc.	Same as step a.

Table 10. Interconnect Card A8, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Continuity	a. Remove interconnect card A8 from the 651S-1/1A and check for continuity between the following pins:		
	A8P1-10 to A8P1-12	0 ohm.	Check wiring between pins.
	A8P1-55 to A8P1-56	0 ohm.	
	A8P1-59 to A8P1-21	0 ohm.	
	A8P1-63 to A8P1-64	0 ohm.	
	A8P1-67 to A8P1-68	0 ohm.	
	A8P1-41 to A8P1-23	0 ohm.	
	A8P1-8 to A8P1-13	0 ohm.	

Table 10. Interconnect Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. (Cont)	b. Measure the resistance between pins A8P1-15 and A8P1-19.	8200 ohms ±10%.	Check A8R4. Check wiring to pins.
2. Mode enabling outputs	a. Connect interconnect card A8 to a card extender. Connect the 651S-1/1A to primary power and set the POWER switch to OPER.		
	b. Set BFO switch to FIXED. Change mode selector as shown in figure 10 and check the output pins on A8 for the indicated levels.	Refer to figure 10.	Check diodes and wiring associated with the chosen mode.
	c. Set BFO switch to VAR and switch mode selector switch through the mode positions. Check the output pins using figure 10. (The only pins affected by switching the BFO switch from FIXED to VAR are pins 35, 37, and 38.)	Refer to figure 10.	Check diodes, gates, and wiring associated with the chosen mode.

MODE AND BANDWIDTH SELECTORS		OUTPUT FROM CARD A8 PINS A8P1-( )																		
		FIXED BFO															VAR-BFO			
POSITION		1	2	3	4	21	23	25	35	37	38	77	79	81	83	84	85	35	37	38
FM 6				X		X							X							
FM 16				X		X											X			
AM 3		X					X						X							
AM 6				X			X						X							
AM 16				X			X										X			
SSB 2.7U				X				X		X				X						X
SSB 2.7L				X				X		X						X				X
CW A8 -004 only	1		X					X		X			X					X		
	.5				X			X		X			X					X		
	.2				X			X		X		X						X		
CW A8 -006 only	WRST		X					X		X			X					X		
	CW				X			X		X			X					X		
	NRST			X				X		X		X						X		
CW A8 -007 only	WBTY		X					X		X							X	X		
	.5				X			X		X			X					X		
	.2				X			X		X		X						X		
ISB				X						X				X	X					x

Note

An X indicates +5 Vdc at the pin in a given mode; a space indicates 0 Vdc.

Interconnect Card A8, Mode Output
Figure 10

Table 11. DCFE Card A8, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Operating voltages	***Note*** If required, remove the strip between J30-46 and J31-47 on the 651S-1/1A sideboard.		
	a. Using the appropriate card extender, extend DCFE card A8 from the 651S-1/1A. Install DCU card A9 in the 651S-1/1A (J30). Connect the 651S-1/1A to primary power. Set POWER switch to OPER and CONTROL switch to LOCAL. Measure the dc level at the following pins:		
	A8P1-28	+14.3 to +15.7 Vdc.	Check C10.
	A8P1-27	+4.7 to +5.3 Vdc.	Check C1 through C7, and C9.
	A8P1-20	-14.3 to -15.7 Vdc.	Check C11.
	A8P1-11, 72	Less than -10 Vdc. NMT 0.5-ohm resistance.	Check wiring.
	b. Check logic level at A8P1-10 and A8P1-60. Set CONTROL to REMOTE and recheck levels.	LOCAL: A8P1-10 NMT +1.0 Vdc. A8P4-60 +4.7 to +5.3 Vdc. REMOTE: A8P1-10 +4.7 to +5.3 Vdc.	
2. Control word II (mode I info) (Cont)	a. Set 651S-1/1A POWER to OFF. Connect 7404A-1 Source Generator/ Display Unit LCU/SINE WAVE connector to 651S-1/1A REMOTE INPUT connector using special cable (figure 3).		
	b. Set 651S-1/1A controls as follows: BFO — FIXED METER — RF AGC — FAST CONTROL — REMOTE VBFO — CCW RF GAIN — CW AF GAIN — Midrange MODE — FM BANDWIDTH — 6		

Table 11. DCFE Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	c. Set 7404A-1 front panel controls as follows: POWER ON PARITY MODE SENSED RETRANSMIT OFF MODE FDX ADDRESS LENGTH 5 BIT PARITY ENCODE MANUAL d. Set 7404A-1 rear panel controls as follows: Function LCU Sine/logic SINE e. Set 7404A-1 control word switches 0 through 4 to logic 1 (up) and switch 5 to logic 0 (down) for all tests. f. Set 651S-1A POWER to OPER. g. Press 7404A-1 CLEAR switch; set control word switches 7, 8, 10, 18, 22, 27, 29, and 30 to logic 1 (up). Assure that all other control word switches are at logic 0 (down). Press SEND/READY switch and observe indicators on the 7404A-1 for monitor word II response (refer to table 8 in the description and principles of operation section for content and format).	***Note*** Lamps 0 through 4 will be lit and 5 will be OFF for all tests.	
(Cont)	MONITOR WORD II FUNCTION Dialogic bit 5-bit DCU address DCFE subaddress	LAMP NO / STATUS 0 Lit 1 Lit 2 Lit 3 Lit 4 Lit 5 Off 6 Off 7 Lit	Check 7404A-1. Check address strapping on special cable (figure 3). Check DCU card A9.

FUNCTION / LAMP NO / STATUS
DCFE Address: 6 Off, 7 On

Table 11. DCFE Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	MONITOR WORD II FUNCTION	LAMP NO / STATUS	
	Parity	8 Lit	Check 7404A-1.
	Pwr interrupt	9 Lit	Check U5, U17, and associated circuits.
	Pwr supply perf	10 Off	Check U17 and U18.
	Synth lock	11 Off	
	Remote	12 Lit	Check Q5, U108, U23, U22, and U21.
	Operate	13 Lit	Check U35, U22, and U21.
	Audio perf	14 Lit	Check U22, U21, and U9.
	Freq storage	15 Off	Continue tests.
	Mode, FM	16 Off	Check CR2, CR23, U19, U25, and U26.
		17 Off	
		18 Off	
		19 Off	
	Vbfo	20 Off	Continue tests.
		21 Off	
		22 Off	
		23 Off	
	Freq	24 through 31 Off	Continue tests.
	h. Set 651S-1/1A MODE to AM. Press 7404A-1 CLEAR switch, set control word switches 10 down and 11 up, and press SEND/READY switch.	LAMP NO / STATUS	
	Mode, AM	16 Lit	Check CR3, U19, U25, and U31.
		17 Off	
		18 Off	
		19 Off	
	i. Set 651S-1/1A MODE to SSB, BANDWIDTH to 2.7U. Press 7404A-1 CLEAR switch; set control word switches 11 and 22 down; set 12, 14, and 20 up; and press SEND/READY switch.	LAMP NO / STATUS	
	Mode, USB; fixed bfo	16 Lit	Check CR5, CR17, U19, U25, U26, U27, and U31.
		17 Lit	
		18 Lit	
(Cont)		19 Off	

Table 11. DCFE Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	j. Set 651S-1/1A BFO switch to VAR. Press 7404A-1 CLEAR switch, set control word switches 14 down and 15 up, and press SEND/READY switch.		
	Mode, USB; vbfo	LAMP NO STATUS 16 Off 17 Lit 18 Lit 19 Off	Check U14 and U23.
	k. Set 651S-1/1A BFO to FIXED and BANDWIDTH to 2.7L. Press 7404A-1 CLEAR switch, set control word switches 20 down and 21 up, and press SEND/READY switch.		
	Mode, LSB; vbfo	LAMP NO STATUS 16 Off 17 Lit 18 Off 19 Lit	Check U14.
	l. Set 651S-1/1A BFO to FIXED, MODE to CW, and BANDWIDTH to .5/2. Press 7404A-1 CLEAR switch; set control word switches 15, 21, 27 down and 23, 24 up; and press SEND/READY switch.		
	Mode, CW; fixed bfo	LAMP NO STATUS 16 Lit 17 Lit 18 Off 19 Off	Check CR6, CR7, and U31.
	m. Set 651S-1/1A BFO to VAR. Press 7404A-1 CLEAR switch, set control word switches 14 down and 15 up, and press SEND/READY switch.		
(Cont)	Mode, CW; vbfo	LAMP NO STATUS 16 Off 17 Lit 18 Off 19 Off	Check CR9 and U14.

Table 11. DCFE Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	n. Set 651S-1/1A BFO to FIXED and MODE to ISB. Press 7404A-1 CLEAR switch, set control word switches 15 down and 14 up, and press SEND/ READY switch.	LAMP NO STATUS	
	Mode, ISB; fixed bfo	16 Lit 17 Lit 18 Lit 19 Lit	Check CR7 and CR43.
	o. Set 651S-1/1A BFO to VAR. Press 7404A-1 CLEAR switch, set control word switches 14 down and 15 up, and press SEND/READY switch.	LAMP NO STATUS	
	Mode, ISB; vbfo	16 Off 17 Lit 18 Lit 19 Lit	Check CR11 and U14.
	p. Assure that the 651S-1/1A VBFO switch is fully ccw. Press 7404A-1 CLEAR switch; then press SEND/ READY switch, and observe lamps 20 through 23. Measure dc voltage at P1-68 with dvm.	Lamps 20 through 23 off. P1-63 +3, ±0.2 Vdc.	Check U29 and U30.
	q. Observe lamps 20 through 23 and measure dc voltage at P1-68 for each position (step) cw of the VBFO switch. Press 7404A-1 CLEAR switch; then the SEND/READY switch for proper results in each step.		
	STEP	LAMPS VDC	
	1	20, 21, 22 out; 23 lit +3.8 ±0.2	Check U40, U29, U30, U34, Q4,and associated components.
	2	20, 21, 23 out; 22 lit +4.6 ±0.2	Check Q3 and associated components.
	3	20, 21 out; 22, 23 lit +5.4 ±0.2	Check Q3, Q4, and associated components.
(Cont)	4	20, 22, 23 out; 21 lit +6.2 ±0.2	Check Q2 and associated components.

Table 11. DCFE Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	STEP	LAMPS VDC	
	5	20, 22 out; 21, 23 lit +7 ±0.2	Check Q2, Q4, and associated components.
	6	20, 23 out; 21, lit +7.7 ±0.2	Check Q2, Q3, and associated components.
	7	20 out; 21, 22 23 lit +8.5 ±0.2	Check Q2, Q3, Q4, and associated components.
	8	21, 22, 23 out; 20 lit +9.2 ±0.2	Check Q1 and associated components.
	9	21, 22 out; 20, 23 lit +10 ±0.2	Check Q1, Q4, and associated components.
	10	21, 23 out; 20, 22 lit +10.7 ±0.2	Check Q1, Q3, and associated components.
	11	21 out; 20, 22 23 lit +11.5 ±0.2	Check Q1, Q3, Q4, and associated components.
	12	22, 23 out; 20 21 lit +12 ±0.2	Check Q1, Q2, and associated components.
3. Control word I (freq info)	a. Set 651S-1/1A MODE to AM, BANDWIDTH to 6, and BFO to FIXED. Press 7404A-1 CLEAR switch, set control word switches 7, 8, 11, 23, 27, and 29 up, and all other control word switches from 6 through 31 shall be down. Press SEND/READY switch.	Lamp 6 off, 7 lit, ignore other lamps.	
	b. Press 7404A-1 CLEAR switch; set control word switches 11, 15, 19, 23, 27, 31 up, and all others 6 through 31 shall be done. Press 7404A-1 SEND/READY switch. Observe frequency readout on 651S-1/1A and lamps 10 through 31 on 7404A-1.	651S-1/1A frequency reads 11.1111 MHz. Lamps 6 and 7 off. Ignore lamps 11, 15, 19, 23 and 27: and 31 shall be lit.	Check logic levels and appropriate pins of U16, U20, U24, U28, U32, U36, U33, and U37.
(Cont)	c. Press 7404A-1 CLEAR switch; set control word switches 10 up, 11 down, 15 down, 14 up, 19 down, 18 up, 23 down, 22 up, 27 down, 26 up, 31 down, 30 up. Press SEND/READY switch.	651S-1/1A freqquency reads 22.-2222 MHz. Lamps 10, 14, 18, 22, 26, and 30 lit.	Same as step b.

Table 11. DCFE Card A8, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	d. Press 7404A-1 CLEAR switch. Set control word switches 14, 18, 22, 26, and 30 down and 13, 17, 21, 25, and 29 up. Press SEND/READY switch.	651S-1/1A frequency reads 24.4444 MHz. Lamps 10, 13, 17, 21, 25, and 29 lit.	Same as step b.
	e. Press 7404A-1 CLEAR switch; set control word switches 13, 17, 21, 25, and 29 down and 12, 16, 20, 24, and 28 up. Press SEND/READY switch.	651S-1/1A frequency reads 28.8888 MHz. Lamps 10, 12, 16, 20, 24, and 28 lit.	Same as step b.
4. Control word II (mode II info)	a. Press 7404A-1 CLEAR switch, set control word switch 6 up, and press SEND/READY switch.	Lamp 6 lit, 7 off. 651S-1/1A frequency reads 28.8888 MHz.	Check word III load and gate circuits.
	b. Measure dc voltage at P1-64 and P1-60.	P1-64 +1.8 Vdc. P1-60 less than 0.1 Vdc.	Check U41, Q6, and associated components. Check U39B, and U38. Check Q7, Q8, and K1.
	c. Press 7404A-1 CLEAR switch, set control word switches 28 down and 29 up. Press SEND/READY switch and measure dc voltage at P1-64.	P1-64 +1.9 Vdc.	Same as step b.
	d. Repeat step c, except set control word switches 29 down and 30 up.	P1-64 +2.0 Vdc.	Same as step b.
	e. Repeat step c, except set control word switches 30 down and 31 up.	P1-64 +2.1 Vdc.	Same as step b.
	f. Repeat step c, except set control word switch 28 up.	P1-64 +1.7 Vdc.	Same as step b.
5. Control word IV (monitor request)	a. Press 7404A-1 CLEAR switch, set control word switches 7 up, 28 and 31 down. Press SEND/READY switch.	Lamps 6 and 7 lit. 651S-1/1A frequency reads 28.8888 MHz.	Check monitor gate circuits.
6. AGC	a. Press 7404A-1 CLEAR switch, set control word switches 6 down and 7, 8, 11, 18, 22, 27, 28, and 29 up. Set 651S-1/1A AGC to off (center). Press 7404A-1 SEND/READY switch.		
	b. Measure dc voltage at P1-24 with 651S-1/1A AGC switch in off, FAST, and SLOW position. Place AGC switch to FAST.	P1-24 0 Vdc in all positions.	Check Q9 and U35.
	c. Press 7404A-1 CLEAR switch and set control word switch 28 down.		
	d. Monitor the AGC voltage at P1-24 when the 7404A-1 SEND/READY switch is pressed.	Voltage counts up to +12 ±0.2 Vdc.	Same as step b.

Table 12. DCU Card A9, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Operating voltages, logic levels	a. Connect DCU card to a card extender. Connect 651S-1/1A to primary power and set POWER switch to OPER. Set CONTROL switch to LOCAL. Measure the dc level at the following pins:		
	A9P1-44	+11.3 to +12.1 Vdc.	Check zener A9VR12 and diode A9CR6.
	A9P1-46	-11.3 to -12.1 Vdc.	Check zener A9VR13 and diode A9CR3.
	A9P1-24 (logic 1)	NLT +3.2 Vdc.	
	A9P1-37 (logic 0)	NMT +0.45 Vdc.	
2. Output signals	a. Set POWER switch to OFF. Remove DCFE card A8 and set CONTROL switch to REMOTE. Connect 7404A-1 Source Generator/Display Unit LCU SINE WAVE connector to 651S-1/1A REMOTE INPUT connector using special cable (figure 3). Set 7404A-1 rear-panel controls as follows: Function: LCU Sine/logic: SINE Set 7404A-1 front-panel controls as follows: POWER: ON PARITY MODE: SENSED RETRANSMIT: OFF MODE: FXD ADDRESS LENGTH: 5 BIT PARITY ENCODE: MANUAL		
	b. Set 7404A-1 control word switches 0 thru 4 to logic 1 (up) and switch 5 to logic 0 (down) for all tests.		
	c. Set 7404A-1 control word switches 6 thru 31 to logic 0 (down). Set 651S-1/1A POWER switch to OPER. Press CLEAR button. Set RETRANSMIT switch to CONTINUAL and check the line-to-line voltage at pins A9P1-2, 4. (Measurement is made by adding the signal measured between each line and ground. The signals added should be 180 degrees out of phase.)	1.7 ±0.8 V p-p line to line.	Check monitor output circuit.
(Cont)			

Table 12. DCU Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	d. Set 7404A-1 RETRANSMIT switch to OFF. Connect the following pins, in turn, to A9P1-21. For each connection, push the 7404A-1 SEND/READY button and check the monitor response lights on the 7404A-1. (Light 0 should be off, 1 thru 4 on, and 5 off for all responses).		On 793-9414-001, if 3 or less of the first four points (A9P1-1, 3, 5, or 11) of test fail, check counter circuit. If all five points fail, check output flatpacks (U403, U303, or U904 and associated circuits). If the test fails at A9P1-17, check control gate circuits (U102B, etc). On 624-5781-001, if test fails at A9P1-11, check counter circuits U23 or U24 and U21. If test fails at A9P1-17, check control gate circuits (U14B, etc).
	A9P1-1 (793-9414-001 only)	7404A-1 lights 8 thru 15 on, 16 thru 23 off, and 24 thru 31 on.	
	A9P1-3 (793-9414-001 only)	Lights 8 thru 15 off and 16 thru 31 on.	
	A9P1-5 (793-9414-001 only)	Lights 6, 7 on; 8, 9 off; 10, 11 on; 12, 13 off, etc.	
	A9P1-11	Lights 6, 7 on; 8 thru 11 off; 12 thru 15 on, etc.	
	A9P1-17	Lights 6 thru 31 off.	
3. Carrier bus, bit clock phase relationship	a. Connect A channel of dual trace oscilloscope to carrier bus input pin A9P1-12. Connect B channel to bit clock pin A9P1-19 and sync scope with B channel input. Ac couple both inputs. Ground both scope probes. Set 7404A-1 RETRANSMIT switch to CONTINUAL.		
	b. Set channel B to 2 V/cm and channel A to 0.1 V/cm. Set sweep for 20 μs/cm and carefully center the horizontal sweep lines. Uncalibrate the scope and adjust the waveform period to exactly 10 cm. Check the phase relationship between the A and B channel waveforms. (Ignore any transient on the carrier bus near the crossover point.)	180.0 ±7.2 degrees out of phase.	Check clock generation circuits on 793-9414-001, U801, U903, U803, and U404A; on 624-5781-001, U62, U64, and U34B.
	c. Connect A channel of scope to sampling clock. On 793-9414-001, connect to flatpack pin A9U401-9. On 624-4781-001, connect to flatpack pin A9U34. Compare the falling edges of the A and B channel signals.	A channel leads B channel by 2.5 ±0.2 cm (50 ±4 μs).	
	d. Set 7404A-1 RETRANSMIT switch to OFF.		

Table 12. DCU Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Control data output, control gate, and monitor gate	a. Connect A channel of oscilloscope to control data output pin A9P1-17. Sync scope with TRAN GATE output on 7404A-1. Push CLEAR button on 7404A-1. Set 7404A-1 RETRANSMIT switch to CONTINUAL and check the control gate on the oscilloscope.	Bits 0 thru 5 are logic 0 and bits 6 thru 31 are logic 1.	
	b. Check the monitor gate pin A9P1-13.	Logic 0 from bit 0 to bit 31 of a control word period. Logic 0 from bit 0 to bit 5 and logic 1 from bit 6 to bit 31 of the next control word period. (Control gate and the monitor gate are never both logic 1 during the same period.)	
	c. Change 7404A-1 control word bit switches 1 thru 5 from the standard bit configuration and recheck the control gate (A9P1-17) and the monitor gate (A9P1-13).	Logic 0 in all bit positions.	Check address recognition circuit.
	d. Set 7404A-1 RETRANSMIT switch to OFF. Set 7404A-1 control word bit switches 0 thru 4 to up position and 5 thru 31 down. Connect oscilloscope to control data pin A9P1-23. Push 7404A-1 CLEAR button. Set 7404A-1 RETRANSMIT switch to CONTINUAL and check the control data on the oscilloscope.	Bits 0 thru 4 are logic 1, and 5 thru 31 are logic 0.	
	e. In turn, set each of the 7404A-1 control word bit switches 6 thru 31 to the up position. Check the control data on the oscilloscope for each switch position change.	Bits 0 thru 4 are logic 1 and 5 is 0. When one of switches 6 thru 31 is up, a logic 1 appears in that control word bit position. If a switch is down, that bit position is logic 0.	
	f. Set 7404A-1 RETRANSMIT switch to OFF.		

Table 12. DCU Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. Monitor data	a. Connect A9P1-21 to A9P1-37. Set 7404A-1 control word bit switches 0 thru 4 to up, 5 down, and 6 thru 31 up. Push 7404A-1 CLEAR button. Set RETRANSMIT switch to CONTINUAL. Check the logic levels represented on the monitor bus output from A9P1-4 (biphase modulated sine wave) with dual trace oscilloscope. Connect the other channel of the scope to carrier bus input A9P1-12. If a cycle of the signal at A9P1-4 is in phase with the signal at A9P1-12, a logic 1 is represented at A9P1-4. If a cycle is 180 degrees out-of-phase, a logic 0 is represented.	Bit 0 is logic 0, 1 thru 4 are 1, and 5 thru 31 are 0. Supervisory interval is all 1's.	
	b. Check the signal level at A9P1-24.	793-9414-001: Greater than 2.8 Vdc.	
	c. Set 7404A-1 RETRANSMIT switch to OFF. Disconnect A9P1-21 from A9P1-37 and connect A9P1-21 to A9P1-24. Push 7404A-1 CLEAR button. Set 7404A-1 RETRANSMIT switch to CONTINUAL and check the monitor bus output A9P1-4 as in step 5.a.	624-5781-001: Greater than 3.2 Vdc. Bit 0 is logic 0, 1 thru 4 are 1, 5 is 0, and 6 thru 31 are 1's. Supervisory interval is all 1's.	
	d. Set 7404A-1 RETRANSMIT switch to OFF. Disconnect A9P1-21 from A9P1-24 and connect A9P1-21 to A9P1-11. Push the 7404A-1 CLEAR button. Set 7404A-1 RETRANSMIT switch to CONTINUAL and check the monitor bus output at A9P1-4.	Bit 0 is logic 0, 1 thru 5 are 1, and 6 thru 31 alternate 1's and 0's.	
	e. Change 7404A-1 control word bit switches 1 thru 5 from the standard bit configuration and recheck monitor bus output at A9P1-4.	No monitor output.	
	f. Set 7404A-1 RETRANSMIT switch to OFF and disconnect A9P1-21 from A9P1-11.		

Table 13. TCU Card A9, Test Procedures.

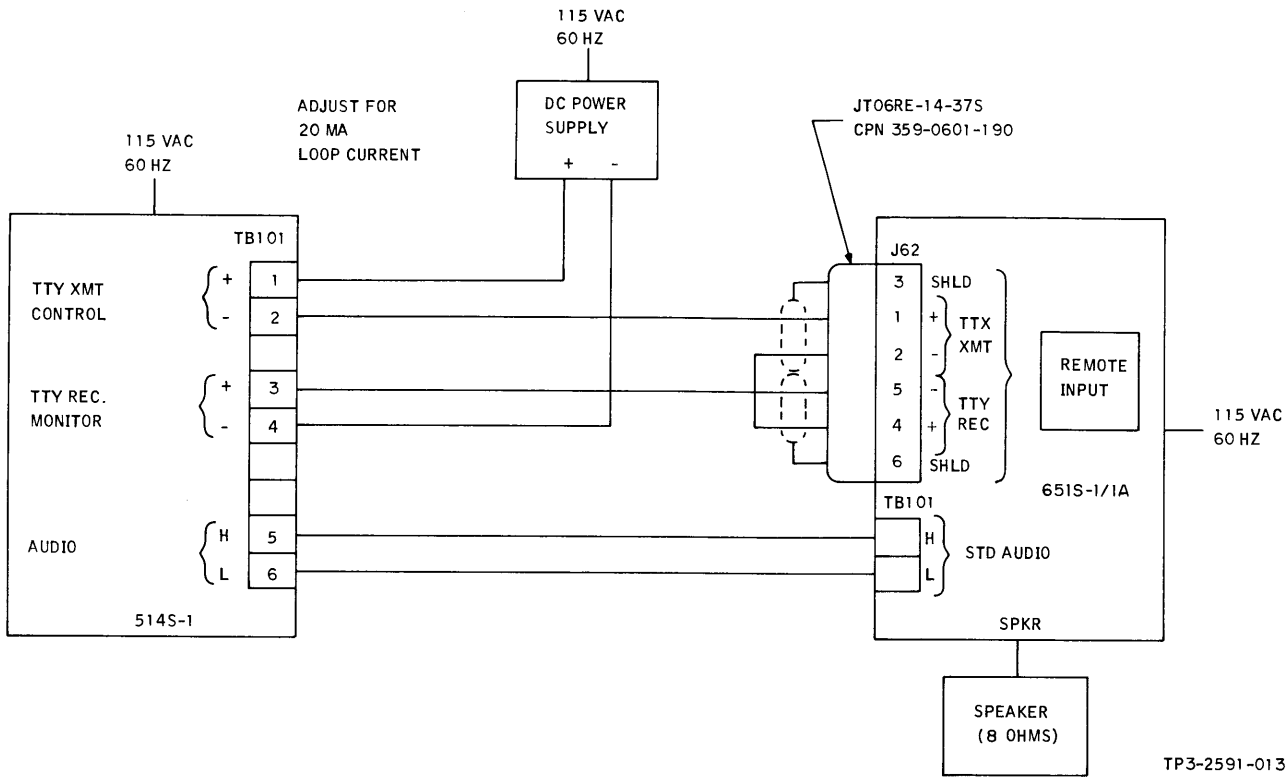
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Initial setup	a. Assure that TCU card A9 and 651S-1/1A sideboard are properly strapped (refer to the installation section of this instruction book). Refer to the 514S-1 control instruction book, Collins part number 523-0764187, for strapping information for the 514S-1. b. Using the appropriate extender card, extend the TCU card from the 651S-1/1A. Install DCFE card A8 in the 651S-1/1A. c. Connect the 651S-1/1A, speaker, 514S-1, and dc power supply as shown in figure 11. d. Set the 514S-1 controls as follows: POWER — OPER BFO — FIXED METER — RF AGC — FAST CONTROL — REMOTE VBFO — CCW RF GAIN — CW AF GAIN — Midrange MODE — SSB BANDWIDTH — 2.70 e. Set 651S-1/1A controls as follows: POWER — OPER CONTROL — REMOTE f. Turn on dc power supply and adjust output voltage to produce 20 mA output current. If more than 40 Vdc is required, remove cover from 514S-1 and adjust A9R3 as required.		
2. Voltage and logic levels	***Note*** Refer to figure 12 for location of test points and components. a. Set 514S-1 frequency to 10.0000 MHz. b. With dvm check for +5 Vdc to all microcircuits (refer to note 3 on schematic diagram for pin numbers). c. Check logic level at TPA.	651S-1/1A frequency reads 10.0000 MHz. 4.7 to 5.3 Vdc. Logic 1 (3.2 to 5.3 Vdc).	Continue tests. Check C4 through C8. Check R11.

Table 13. TCU Card A9, Test Procedures (Cont).

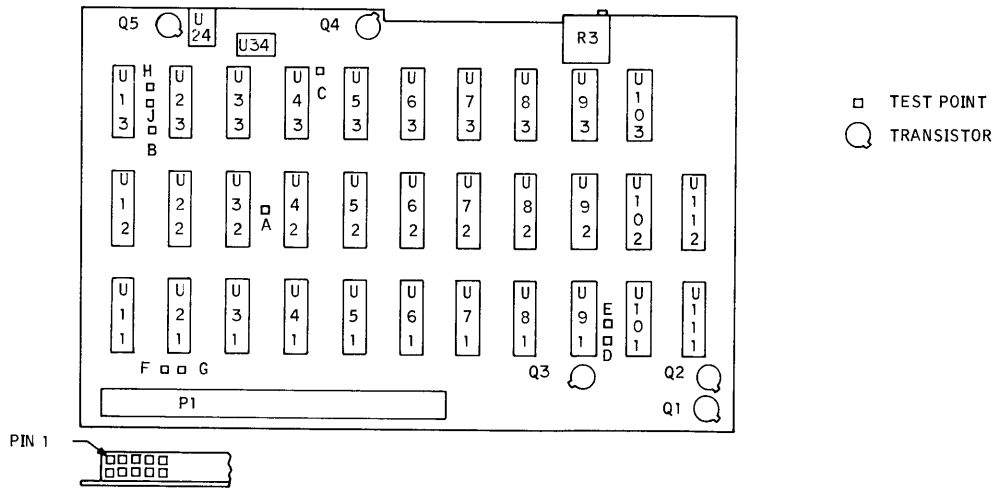
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Timing circuit	a. With an oscilloscope, measure the period (frequency) of the clock pulse at TPD.	282 to 286 μs (3520 Hz).	Adjust A9R3. If adjustment fails to bring pulse to within limits, check Q1, Q2, Q3, and associated components.
	b. Measure pulse rate (WT2F) at U12A-8.	1750 to 1770 Hz.	Check U12, U103C, and U103D.
4. Fault line	a. The equipment should not go into fault condition during normal testing.	Fault indicator on 514S-1 out at all times.	Check CR7, U34, U24, VR1, Q5, and associated components.
5. Frequency and mode	a. Increase 514S-1 frequency in 1-MHz increments to 29.0000 MHz.	651S-1/1A frequency shall increase in 1-MHz increments and track with the 514S-1 frequency.	Most circuits in TCU card A9 are interacting. Therefore, to locate a malfunction, troubleshoot in sequence the following circuits. (Refer to the schematic diagram and the functional block diagram as required.) (1) DCFE interface circuit; U22, U41, and associated drivers. (2) Subaddress decode circuit, U92A and associated drivers. (3) Down counter circuits; U82, U102B, U72, U92B, and associated drivers. (4) Scan control circuit; U51 and associated drivers. (5) Address control circuit; U31, U32, U42, U33A, U33B, and associated drivers. (6) TTY character receive circuit; U61, U34, U101, U102B, U73A, and associated drivers. (7) Error detection circuit; U24, U13, U22, U12, and associated drivers.
(Cont)	b. Increase 514S-1 frequency in 100-kHz increments to 29.9000 MHz.	651S-1/1A frequency shall increase in 100-kHz increments and	Same as step a.

Table 13. TCU Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)		track with the 514S-1 frequency.	
	c. Increase 514S-1 frequency in 100-Hz increments to 29.9999 MHz.	651S-1/1A frequency shall increase in 100-Hz increments and track with the 514S-1.	Same as step a.
6. Audio and vbfo	a. Set 514S-1 frequency to 9.9999 MHz and set 514S-1 AF GAIN fully ccw, then rotate slowly cw.	Shall have good control of audio level in speaker.	Same as test 5, step a.
	b. Set 514S-1 BFO switch to VAR and slowly rotate VBFO control cw, one position at a time, and note change in audio level in speaker.	Tone shall vary slightly (10 Hz) in each position.	Same as test 5, step a.
7. Rf gain	a. Rotate the 514S-1 RF GAIN control counterclockwise and note rf meters on the 514S-1 and 651S-1/1A.	Meter indication increase. The 651S-1/1A meter tracks the 514S-1 meter. Audio disappears in speaker.	Same as test 5, step a.



TCU Card A9, Test Setup
Figure 11



TCU Card A9, Test-Point and Component Location
Figure 12

Table 14. Scan Control Card A9, Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Continuity	Verify continuity between the following pin pairs: P1-15, 47 P1-42, 43 P1-10, 45 P1-2, J1-13 P1-4, J1-15 P1-6, J1-27 P1-8, J1-25 P1-12, J1-29 P1-14, J1-7 P1-16, J1-5 P1-18, J1-3 P1-20, J1-1 P1-24, J1-11 P1-26, J1-9	Continuity	Replace respective wire.
2. Preliminary setup	a. If required, remove jumpers from J30-29 to 31 and J30-32 to 34 on 651S-1/1A chassis sideboard. b. Strap the scan control card for a scan range of 100 kHz and a dwell time of 600 ms (refer to the installation section of this instruction book). c. Extend scan control card A9 using the appropriate extender card. Connect the 651S-1/1A to primary power and set controls as follows: POWER — OPER BFO — FIXED METER — RF AGC — FAST CONTROL — LOCAL SQUELCH — OFF (optional) DIAL — UNLOCK MODE — SSB BANDWIDTH — 2.7U AF GAIN — Midrange d. Select 10.0000 MHz and adjust the RF GAIN control for 1 mV on meter.		
3. Voltage and logic levels	a. Check the dc level at the following points: P1-35 and 36 P1-37 and 38 P1-21 b. Check for logic 1 at J1-33.	 4.7 to 5.3 Vdc. Ground. 0 Vdc. 4.3 to 5.7 Vdc.	 Check C8 through C10. Check wiring from P1-37 and 38 to ground. Check R17.

Table 14. Scan Control Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Scan operation	a. Set 651S-1/1A frequency to 10.0000 MHz.		
	Note Use a stopwatch, a standard watch, or clock with second hand to measure scan-up and scan-down time.		
	b. Set 651S-1/1A control switch to REMOTE and make the following checks:		
	(1) Up-scan tracking	Frequency display shall track upward in frequency in 100-Hz increments.	Perform test 5.
	(2) Scan range	100 kHz up from initial frequency of 10.0000 MHz.	Perform test 5.
	(3) Scan-up time	NMT 10 minutes.	Perform test 5.
	(4) Scan-down time	651S-1/1A shall automatically scan down to initial frequency in NMT 5 seconds then automatically repeat up-scan operation.	Perform test 5.
	c. Set 651S-1/1A CONTROL to LOCAL and reset frequency to 10.0000 MHz.	Scanning operation stops.	Perform test 5.
	d. Set 651S-1/1A POWER to OFF. Remove scan control card and strap for a scan range of 60 kHz and a dwell time of 100 ms (refer to the installation section of this instruction book). Reinstall the scan control card on the extender card.		
	e. Set 651S-1/1A POWER to OPER, CONTROL to REMOTE, and make the following checks:		
	(1) Scan range	60 kHz up from initial frequency of 10.0000 MHz.	Perform test 5.
	(2) Scan-up time	NMT 8 minutes.	Perform test 5.
(Cont)	(3) Scan-down time	NMT 5 seconds.	Perform test 5.

Table 14. Scan Control Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	(4) Automatic action	651S-1/1A shall automatically repeat scanning operation.	Perform test 5.
	(5) Set frequency counter TIME BASE to 10S and measure master clock pulse rate, during scan-up operation, at test point P2-1.	38 to 47 Hz.	Check Q2, A3, and associated circuits.
	(6) Set frequency counter TIME BASE to 1S and measure master clock pulse rate, during scan-down operation, at P2-1.	480 to 580 Hz.	Same as step (5).
	(7) Set frequency counter TIME BASE to 10S and measure the program clock pulse rate, during scan-up operation, at P2-2.	Pulse rate one-half the pulse rate in step (5) ±1 Hz.	Check U11, U12B, U22A, and U22B.
	(8) Set frequency counter TIME BASE to 1S and measure program clock pulse rate, during scan-down operation, at P2-2.	Pulse rate the same as the master clock pulse rate in step (6) ±10 Hz.	Same as step (7).
	(9) Repeat steps c, d, and e (1), (2), (3), (4) with the scan card strapped for dwell times of 200 ms, 300 ms, 400 ms, and 500 ms and various scan ranges from 5 kHz to 100 kHz. **Note** Test 5 should be performed only if some part of test 4 fails.	Scan range determined by strapping. Scan-up time NMT 10 minutes at any frequency. Scan-down time NMT 5 seconds at any frequency. Automatic scanning action.	Same as step e(1), (2), (3), and (4).
5. Fault isolation trouble-shooting (Cont)	a. Set 651S-1/1A CONTROL to LOCAL and POWER to OFF. Remove the scan control card and strap for a scan range of 100 kHz and a dwell time of 100 ms. Reinstall scan control card on extender. b. Set 651S-1/1A POWER to OPER, frequency to 10.0000 MHz, and CONTROL to REMOTE. **Note** Refer to the illustrated parts list, part 2, of this instruction book for location of components.		

Table 14. Scan Control Card A9, Test Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
5. (Cont)	c. Clock circuits		
	(1) With the 651S-1/1A in up-scan operation, check for an enabling signal (logic 0) on U41A-8.	Logic 0.	Proceed to step d.
	(2) Set frequency counter TIME BASE to 10S for up-scan, 1S for down-scan, and measure master clock pulse rate at P2-1.	Up-scan: 38 to 47 Hz. Down-scan: 480 to 580 Hz.	Check Q2, Q3, U62E, and associated circuits.
	(3) Measure program clock pulse rate at P2-2.	Up-scan: one-half the pulse in step (2) ±1 Hz. Down-scan: same as pulse rate in step (2) ±10 Hz.	Check U11, U12B, U21A, U22A, and U22B.
	(4) Measure scan clock pulse rate at P2-5.	One-half the program clock pulse rate.	Check U41B.
	d. Scan load and direction. With dvm, measure logic level on the following:		
	P2-3	Logic 1.	Check Q1 and associated circuit. Check U52A, U12A, U62A, B, and C.
	P2-6	Up-scan: logic 1. Down-scan: logic 0.	Check U41A.
	P1-34	Up-scan: logic 1. Down-scan: logic 0.	Check U31A, B, and D.
	P2-4 U21C-10	Logic 1 at all time. Logic 0 at all time.	Check flip-flop U21D and C.
	e. Automatic scan circuits. Observe frequency display.	Frequency will track (in 100-Hz increments) up through the scan range, then track down through the scan range to initial frequency, and then automatically repeat operation.	Check U42A and associated RC circuits. Check U31C, U32C and D. Check U51, U61, and U71, and associated circuits.

Table 15. Synthesizer Divider Card A10, Performance Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Divider ratio	a. Remove 651S-1/1A dust cover. Extend card A10. Disconnect the extender coaxial connector from A10P1. Connect the hf signal generator through a 6-dB pad to A10P1 using a BNC to subminiax adapter cable. Set if for CW output at 25 MHz at 0.8 V.		Return to Collins authorized repair facility.
	b. Disconnect extender coax from A10P4 and connect A10P4 to the frequency counter.		
	c. Connect the uncalibrated rf output of the hf signal generator to the external time base input on the frequency counter.		
	d. Set the 651S-1/1A POWER switch to OPER and set it to 3.3333 MHz (any mode).		
	e. Record the division ratio indicated on the frequency counter.	717.	
	f. Set the 651S-1/1A to 29.9999 MHz and record the division ratio.	3449.	
	g. Set the 651S-1/1A to 16.6666 MHz and record the division ratio.	2083.	
	h. Reinstall card A10.		

Table 16. Synthesizer Reference Card A11, Performance Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Signal levels	a. Remove the 651S-1/1A dust cover and connect to primary power. Extend card A11. Disconnect extender coaxial connector from A11P9. Connect the power meter to A11P9 using the power meter adapter cable (figure 4).		Return to Collins authorized repair facility.
	b. Set the 651S-1/1A POWER switch to OPER, any frequency, and any mode.		
	c. Record the power meter indication.	3.5 to 4.6 mW.	
	d. Disconnect extender coax from A11P8 and connect the power meter to A11P8 using the power meter adapter cable. Record the power meter indication.	0.14 to 0.19 mW.	
	e. Reconnect extender coaxes to A11P8 and A11P9 respectively. Disconnect extender coax from A11P2. Clip a 75-ohm, 1/2-watt resistor from the center conductor of A11P2 to ground. Measure the rf level at A11P2 with an rf voltmeter.	550 to 710 mV.	Select new value of A11R2.
	f. Reconnect coax to A11P2. Disconnect extender coax from A11P1 and clip 1000-Ω, 1/2-watt resistor from A11P1 to ground. Measure the rf level at A11P1.	550 to 710 mV.	Select new value of A11R1.
	g. Ground pin A11P5-4 and measure the rf level at A11P1 again.	NMT 100 mV.	
	h. Unground A11P5-4. Measure the frequency at A11P1.	450.000 kHz.	
	i. Reconnect coax to A11P1.		
2. Loop 1 divider	a. Connect an oscilloscope to the center conductor of A11P6.		
	b. Measure the pulse width of one pulse in the pulse train displayed at 2 V up from zero.	20 to 80 μs.	
	c. Leave the scope connected and disconnect coax from A11P7.	Scope display should drop to 0 ±0.2 Vdc, no pulses.	
	d. Reconnect coax to A11P7. Disconnect coax from A11P6.	Scope display should go to 4.9 ±0.2 Vdc, no pulses.	
	e. Reconnect coax to A11P6.		

Table 16. Synthesizer Reference Card A11, Performance Test Procedures (Cont).

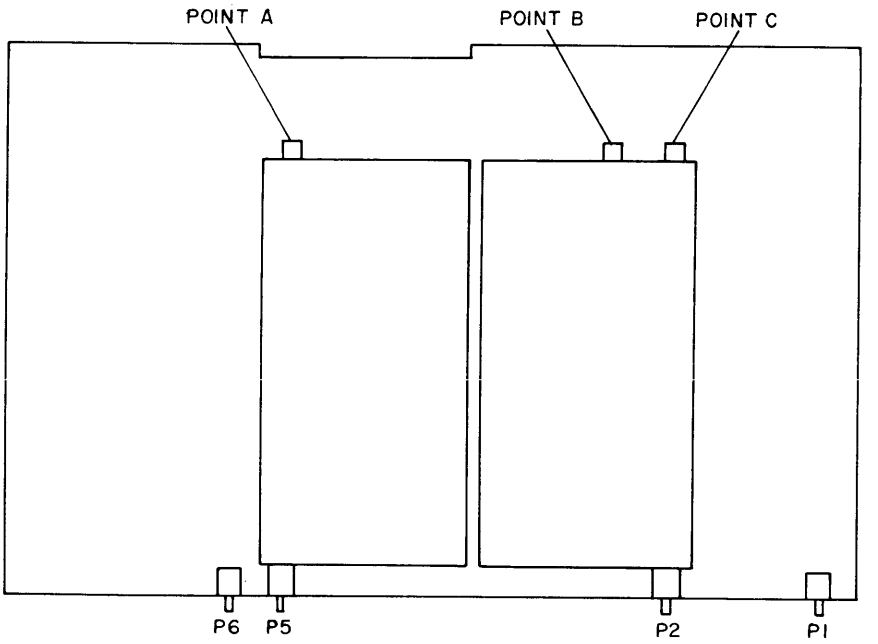
TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. Loop 2 divider	a. Monitor A11P3 with the scope. Measure one pulse width.	20 to 80 μs.	
	b. Disconnect coax from A11P3, with scope still on A11P3.	Scope display should go to 0 ±0.2 Vdc, no pulses.	
	c. Reconnect coax to A11P3. Disconnect coax from A11P4.	Scope display should go to 3.5 ±0.6 Vdc, no pulses.	
	d. Reconnect coax to A11P4.		
4. Fault line check	a. Check the dc level at A11P5-2 with digital voltmeter.	0 ±0.2 Vdc.	
	b. Disconnect coax from A11P7. Check dc level at A11P5-2.	+3.7 ±0.7 Vdc.	
	c. Reconnect coax to A11P7. Disconnect coax from A11P4. Check dc level at A11P5-2.	+3.7 ±0.7 Vdc.	
	d. Reconnect coax to A11P4.		
5. Frequency test	a. Disconnect coax from A11P3. Connect frequency counter to A11P3 with BNC to subminiax adapter cable.		
	b. Check frequency at A11P3.	10 kHz ±1 Hz.	
	c. Reconnect coax to A11P3. Disconnect coax from A11P6. Check frequency (as above) at A11P6.	9.9 kHz ±1 Hz.	
	d. Reconnect coax to A11P6. Disconnect coax from A11P2. Check frequency at A11P2.	9.9 MHz ±10 Hz.	
	e. Reconnect coax to A11P2. Disconnect coax from A11P9. Check frequency at A11P9.	99 MHz ±10 Hz.	
	f. Reconnect coax to A11P9. Disconnect coax from A11P8. Check frequency at A11P8.	99 MHz ±10 Hz.	
	g. Reinstall card A11.		

Table 17. Synthesizer Mixer Card A12, Performance Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Divider test	a. Remove 651S-1/1A dust cover. Extend card A12. Disconnect extender coax from A12P4. Connect an hf signal generator to A12P4. Set it to 80 MHz with 100-mV output.		Return to Collins authorized repair facility.
	b. Disconnect coax from A12P5 and connect an hf signal generator to A12P5. Set it to 101 MHz with 100-mV output.		
	c. Disconnect coax from A12P7. Connect the frequency counter input to A12P7, and connect the frequency counter external time base to A12TP14.		
	d. Set the 651S-1/1A POWER switch to OPER at 10.0033 MHz.		
	e. Record the frequency counter indication.	1433.	
	f. Set the 651S-1/1A to 10.0066 MHz and record the frequency counter indication.	1466.	
	g. Set the 651S-1/1A to 10.0099 MHz and record the frequency counter indication.	1499.	
2. Mixer	a. Reconnect extender coaxes to A12P4, A12P5, and A12P7. Disconnect coax from A12P2 and connect an hf signal generator to A12P2. Set it for 99 MHz with 100-mV output.		
	b. Disconnect coax from A12P3 and connect an hf signal generator to A12P3. Set it to 59 MHz with 100-mV output.		
	c. Connect a 261-ohm resistor from A12TP14 to ground.		
	d. Measure the rf level at A12TP14.	NLT 0.7 Vrms.	

Table 18. Synthesizer VCO Card A13, Performance Test Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Regulator	a. Remove dust cover. Set 651S-1/1A POWER switch to OPER, any mode, any frequency.		Return to Collins authorized repair facility.
	b. Check dc levels at points A, B, and C (figure 13).	A = +10.5 ±0.2 Vdc. B = -10.5 ±0.3 Vdc. C = +10.6 ±0.2 Vdc.	
2. Filter driver	a. Extend card A13. Disconnect extender coaxes from A13P1 and A13P6. Connect a pulse generator to both A13P1 and A13P6.		
	b. Disconnect extender coaxes from A13P2 and A13P5. Connect a frequency counter to A13P2.		
	c. Set the pulse generator to 10.000 kHz with 5.0-V pulses. Monitor pulse generator output with oscilloscope. Set pulse width to equal pulse and space timing (50% duty cycle).		
	d. Measure frequency at A13P2.	91 ±4 MHz.	
	e. Measure frequency at A13P5.	105 ±4 MHz.	



VCO Card A13, Test-Point Location
Figure 13

Table 19. Frequency Control Card A14, Test Procedures.

TEST	PROCEDURES	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Voltage and logic levels	a. Using the appropriate card extender, extend frequency control card A14 from the 651S-1/1A chassis. Set CONTROL switch to LOCAL.		
	b. On 651S-1/1A receivers that have the keep-alive voltage option, connect a +6-Vdc power source to the battery terminals at rear of receiver.		
	c. Set 651S-1/1A POWER to OPER, MODE to SSB, BANDWIDTH to 2.7U, and frequency to 10.9990 MHz.		
	d. Measure the dc level at the following pins:		
	P1-3 and 4	+26.5 to +29 Vdc.	Check Q1 through Q5 and associated circuits.
	P1-17 and 18	+4.3 to +5.7 Vdc.	Check C24, C26, and C28 through C33.
	P1-19 and 20	+4.3 to +5.7 Vdc.	Check C25, C27, C34 and C35.
	P1-1 and 2	Ground	Check wiring on pins.
	e. Measure the logic level at the following points:		
	P1-57	Logic 1.	Check R3 and R4.
	P1-5	Logic 1.	Check R5 and R7.
2. Remote control mode	a. Set 651S-1/1A frequency to 19.9999 MHz and CONTROL switch to REMOTE.	Frequency display reads 19.9999 MHz. Comma indicator is lit.	Check U36, U35 and U29. Check U31, U32, U38, and U28. Check U40, U41, U30, U39, and U33.
	b. Set 651S-1/1A frequency to 26.6666 MHz.	Frequency display reads 26.6666 MHz. Comma indicator is lit.	Same as step a.
3. Remote to local transfer	a. Set 651S-1/1A CONTROL switch to LOCAL.	Same as step b.	Check 651S-1/1A CONTROL switch.

Table 19. Frequency Control Card A14, Test Procedures (Cont).

TEST	PROCEDURES	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. Frequency controls	a. Set 651S-1/1A frequency to X2.2222 MHz. Slowly rotate the 1-MHz control clockwise (increase) one increment at a time at least 20 steps and observe frequency.	Frequency increases in 1-MHz steps. Comma indicator lit.	From 2 to 9 MHz, check U5, U25, U18, and U12. From 10 MHz up, check U6, U27, U34, U26, U33, U19, U20, and U7. Check Q8, Q9, and associated circuits.
	b. Slowly rotate the 1-MHz control counterclockwise (decrease) one increment at a time to X1.2222 MHz.	Frequency decreases in 1-MHz steps to X1.2222 MHz.	Same as step a.
	c. Slowly rotate the 100-kHz control clockwise (increase) one increment at a time to 1.9222 MHz.	Frequency increases in 100-kHz steps to 1.9222 MHz.	Check U4, U24, UT1, and U17.
	d. Slowly rotate the 100-kHz control counterclockwise one increment at a time to 1.2222 MHz.	Frequency decreases in 100-kHz steps to 1.2222 MHz.	Same as step c.
	e. Rotate the 1-MHz control counterclockwise (decrease) one increment.	Frequency display shall read XX2222. The 10-MHz and 1-MHz digits and the comma indicator shall be out.	Same as step a.
	f. Set 651S-1/1A frequency to XX1990. Slowly rotate the 100-Hz control (tuning knob) clockwise one increment at a time to XX1999.	The 100-Hz digit increases in 100-Hz steps.	Check U1, U21, U14, and U8.
	g. Continue to rotate the 100-Hz control clockwise, one increment at a time to XX2090.	The 1-kHz digit will increase one 1-kHz step for each ten 100-Hz steps.	Check I2, U22, U15, and U9.
	h. Continue to rotate the 100-Hz control clockwise one increment at a time to XX2900.	The 10-kHz digit will increase one 10-kHz step for each ten 1-kHz steps.	Check U3, U23, U16, and U10.
5. 30-MHz reset	a. Set 651S-1/1A frequency to 29.9999 MHz. Rotate the 100-Hz control (tuning knob) clockwise one increment.	Frequency display reads XX0000, note that the 10-MHz and 1-MHz digits and comma indicator are OUT.	Repeat tests 1 through 4.

Table 19. Frequency Control Card A14, Test Procedures (Cont).

TEST	PROCEDURES	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. Tuning control slew rate	a. Set 651S-1/1A frequency to 11.1111 MHz. Set 651S-1/1A POWER to OFF then back to OPER.	Frequency display shall read XX0000 when power is turned back on.	
	b. Observe the knob position of the 100-Hz tuning control for reference; then rotate the tuning control clockwise, three complete rotations, at a rate of approximately one rotation per second.	Frequency display shall track as tuning control is rotated.	
	c. Rotate the tuning control three complete rotations counter-clockwise at a rate of approximately one rotation per second and observe the frequency display.	Frequency display shall track as tuning control is rotated. When tuning control is returned to the initial starting point (reference), the frequency display shall read XX0000.	
7. Power loss frequency storage	a. On 651S-1/1A receivers having the keep-alive voltage circuit option, (assure that a +6-Vdc source is connected to the battery terminals at the rear of the receiver) set frequency controls to any frequency between 10.0000 and 29.9999 MHz and note the reading.		
	b. Unplug the primary power cable from the 651S-1/1A for 5 to 6 seconds and then reconnect.	Frequency display shall read the same as in step a.	
8. Dial lock	a. Depress the dial lock switch. Rotate tuning control while observing frequency display.	Frequency reading shall not change.	

651S-1/1A General Purpose HF Receiver

COLLINS

diagrams

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18 Blank	1 Oct 71
19	1 Nov 72
20 Blank	1 Oct 71
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22 Blank	1 Oct 71
*23	1 Apr 73
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*25	1 Apr 73
26 Blank	1 Oct 71
*27	1 Apr 73
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*29	1 Apr 73
30 Blank	1 Oct 71
31	1 Nov 72
32 Blank	1 Oct 71
33	1 Nov 72
34 Blank	1 Oct 71
*35	1 Apr 73
36 Blank	1 Oct 71
*37	1 Apr 73
38 Blank	1 Oct 71
39	1 Nov 72
40 Blank	1 Oct 71
41	1 Nov 72
42 Blank	1 Oct 71
43	1 Nov 72
44 Blank	1 Oct 71
45	1 Nov 72
46 Blank	1 Oct 71
47	1 Nov 72
48 Blank	1 Oct 71
*49	1 Apr 73
50 Blank	1 Oct 71
*51	1 Apr 73
52 Blank	1 Oct 71
*52A	1 Apr 73
52B Blank Added	1 Jul 72
*53	1 Apr 73
54 Blank	1 Oct 71
*54A	1 Apr 73
54B Blank Added	1 Jul 72
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56 Blank	1 Oct 71
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*61	1 Apr 73
62 Blank	1 Oct 71
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107	1 Nov 72
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116 Blank	1 Oct 71
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118 Blank	1 Oct 71
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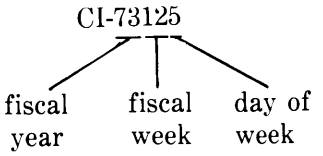
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1. CONFIGURATION STATUS CONTROL

Collins has two methods for identifying the configuration status of a unit or subassembly. One method uses a 5-digit number referred to as the configuration identifier (CI). A typical 5-digit CI is as follows:



Whenever a change (process, mechanical, or electrical) occurs, the CI changes. For example, if a subassembly configuration status identified by CI-73125 has an electrical component change on the 5th day of the 14th fiscal week of fiscal year 1973, then the new CI appearing on the subassembly would be CI-73145.

Whenever possible, the identifier number is marked on the unit/subassembly approximately two spaces following the 10-digit part number. When this is not practicable, it is marked as close as possible to, but not immediately following, the part number. As an example, in a subassembly with high parts density, the 10-digit part number may appear on one side of the subassembly, the identifier number on the other.

Note

If two identifier numbers appear on the same subassembly, the numerically larger identifier would be used for configuration.

The second method uses a 2-character (maximum) alphabetic identifier. The alphabetic identifier will be preceded by the letters, "REV" (revision) and will start with 0 if no changes have been processed. The first change will be identified as "A," the second as "B," and continuing through Z to AA and ultimately to ZZ.

At the time of rework, the unit or subassembly will be re-marked to reflect the design level to which it is being upgraded. This is done by leaving the original marking on the unit or subassembly and adding the letters "RWK" (rework) followed by the alphabetic identifier of the latest change incorporated in the rework. For example, this will differentiate between a version B unit that has been reworked to version F from a newly manufactured version F.

Only configuration/alphabetic identifiers that result in schematic and parts breakdown changes are covered in this manual. Therefore, if a unit or subassembly has an identifier that numerically/alphabetically falls between identifiers listed on the schematic change page, the electrical configuration is represented by the earlier identifier.

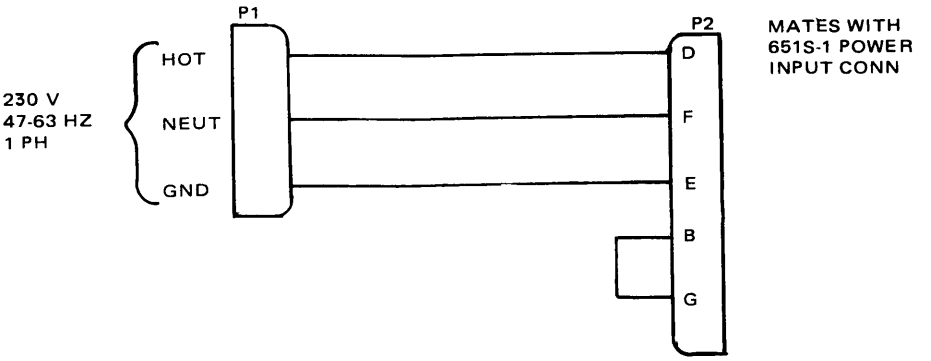
2. CONFIGURATION EFFECTIVITY

Refer to the schematic changes page preceding each subassembly schematic for any subassembly changes that may have occurred and the corresponding identifier covering each change.

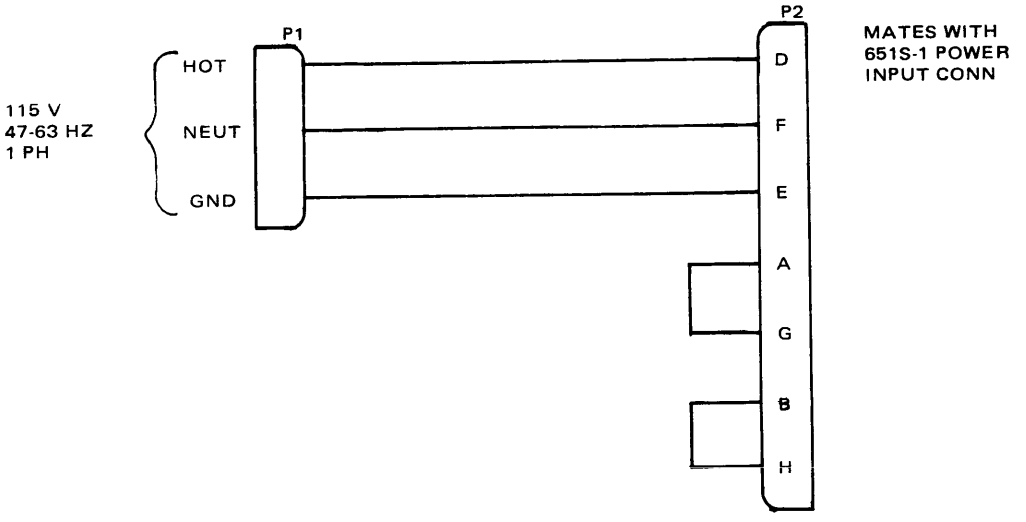
Listed below are the units/subassemblies with the latest identifier covered by this document.

UNIT/SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Chassis	606-9423-003	72173
	606-9423-005	72274
	606-9423-006	72354
	606-9423-007	72326
Power supply regulator card A1	778-2949-001	73116
Audio card A2	778-2948-002	73116
	778-2948-003	73116
	778-2948-004	73116
	778-2948-005	73116
ISB card A3	778-2952-001	73046
If amplifier card A4	778-2951-001	73156
	778-2951-003	73156
	778-2951-004	73156

UNIT/SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
If filter card A5A1	797-3571-001	73136
	797-3571-002	73136
	797-3571-006	73136
	797-3571-007	73136
	797-3571-010	73136
	797-3571-011	73136
	797-3571-012	73136
If filter card A5A2	797-3585-002	73026
	797-3585-003	73026
	797-3585-010	73026
	797-3585-011	73026
	797-3585-012	73026
Rf module A6	790-1048-008	72263
	790-1048-010	72314
	790-1048-020	73056
	790-1048-021	73056
Decoder/driver A7	778-2928-003	73046
Decoder/driver A7	608-9087-001	73012
Decoder/driver A7	608-9121-001	73033
DCFE card A8	624-5744-001	73036
Interface card A8	778-2924-004	72346
	778-2924-006	72353
	778-2924-007	73075
DCU card A9	793-9414-001	72473
DCU card A9	624-5781-001	72393
	774-7842-001	72523
TCU card A9	783-9480-001	73083
Auto scan card A9	783-9368-001	73023
Synthesizer divider card A10	793-9334-002	73026
	793-9334-006	73033
Synthesizer reference card A11	793-9333-002	72246
Synthesizer mixer card A12	793-9332-002	72146
Synthesizer VCO card A13	793-9331-003	73253
Frequency control card A14	783-9283-001	72313



230 VOLT POWER CABLE



115 VOLT POWER CABLE

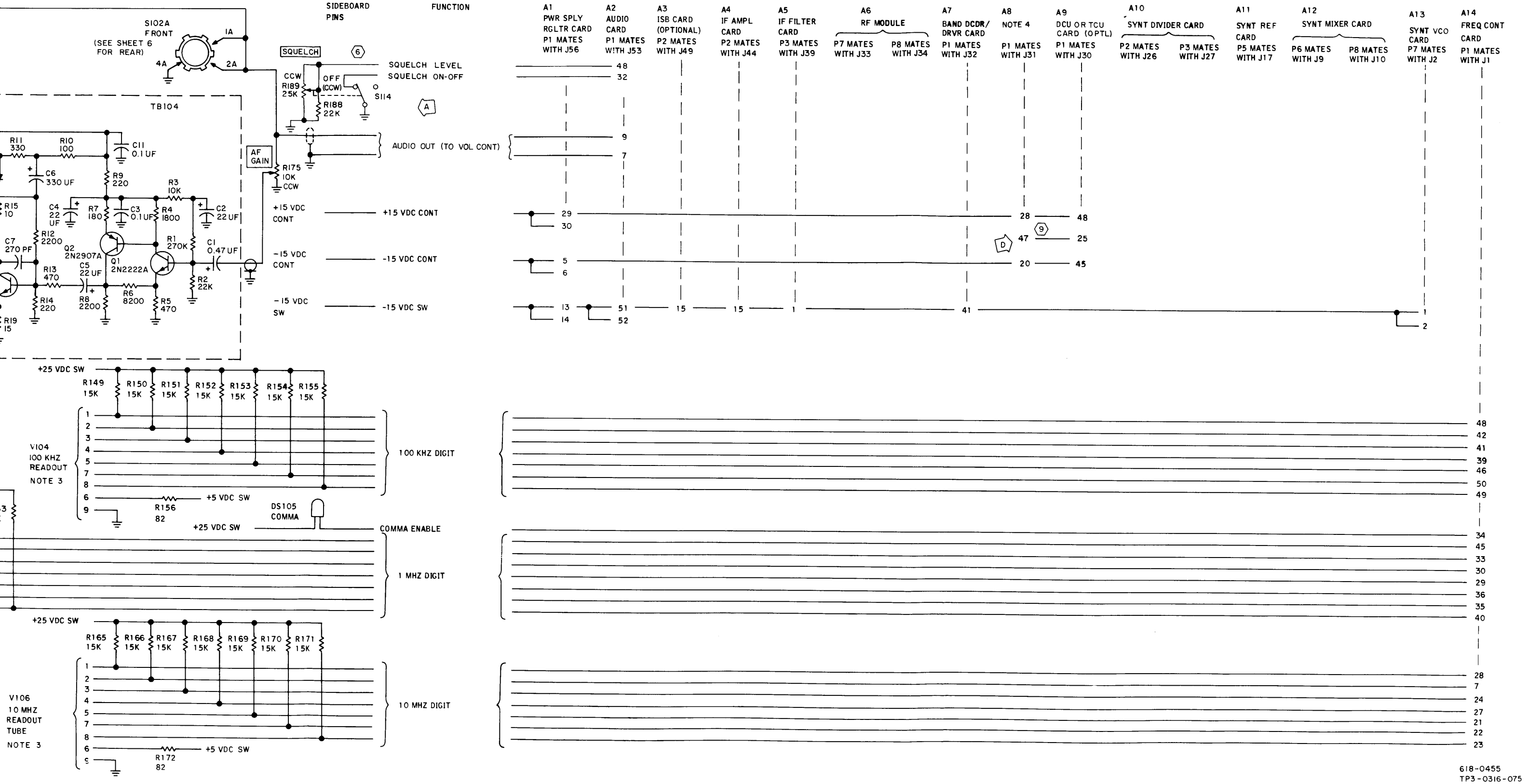
609-1123
TP2-5666-013

Power Cables, Schematic Diagram
Figure 1

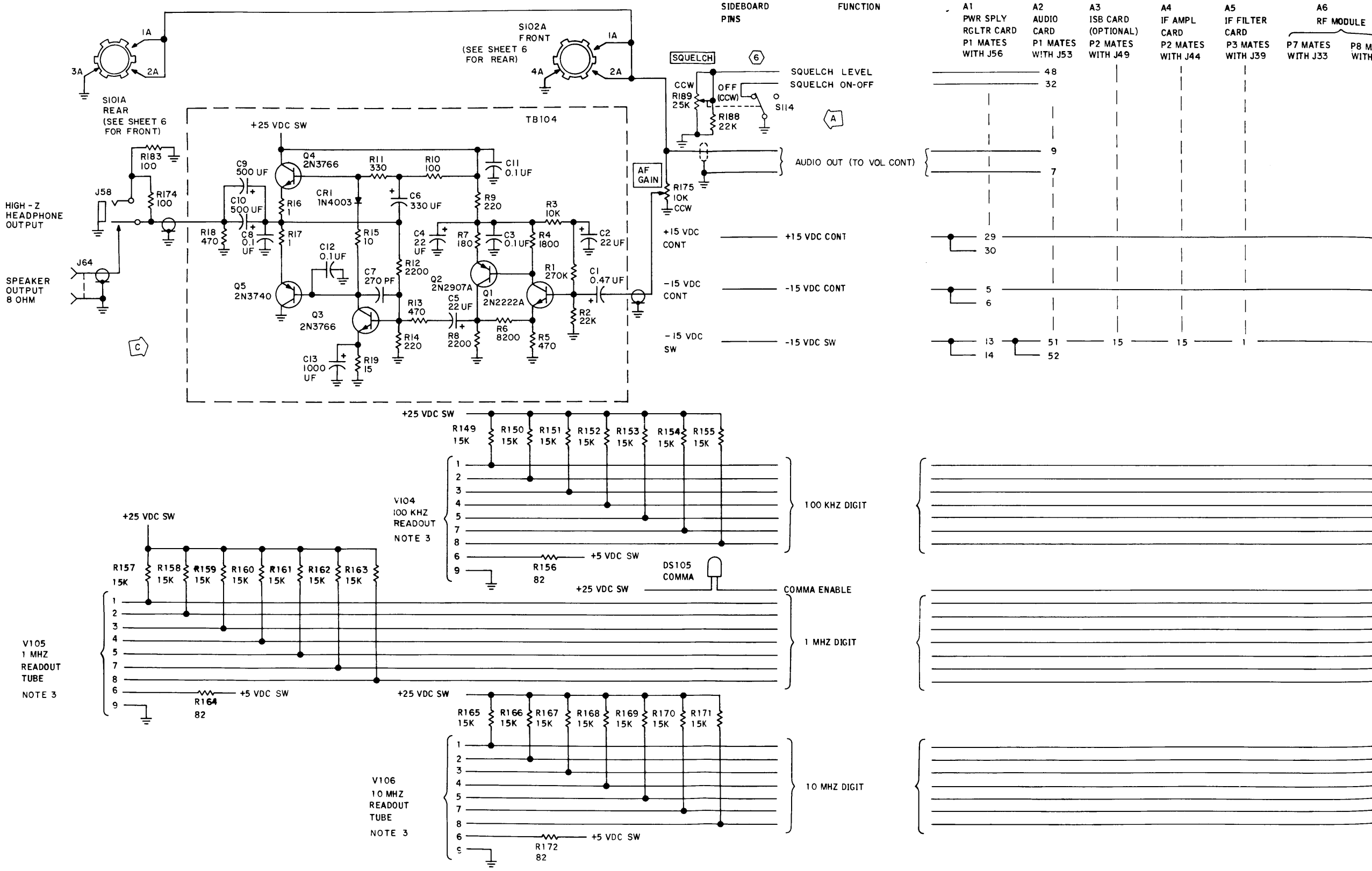
SCHEMATIC CHANGES

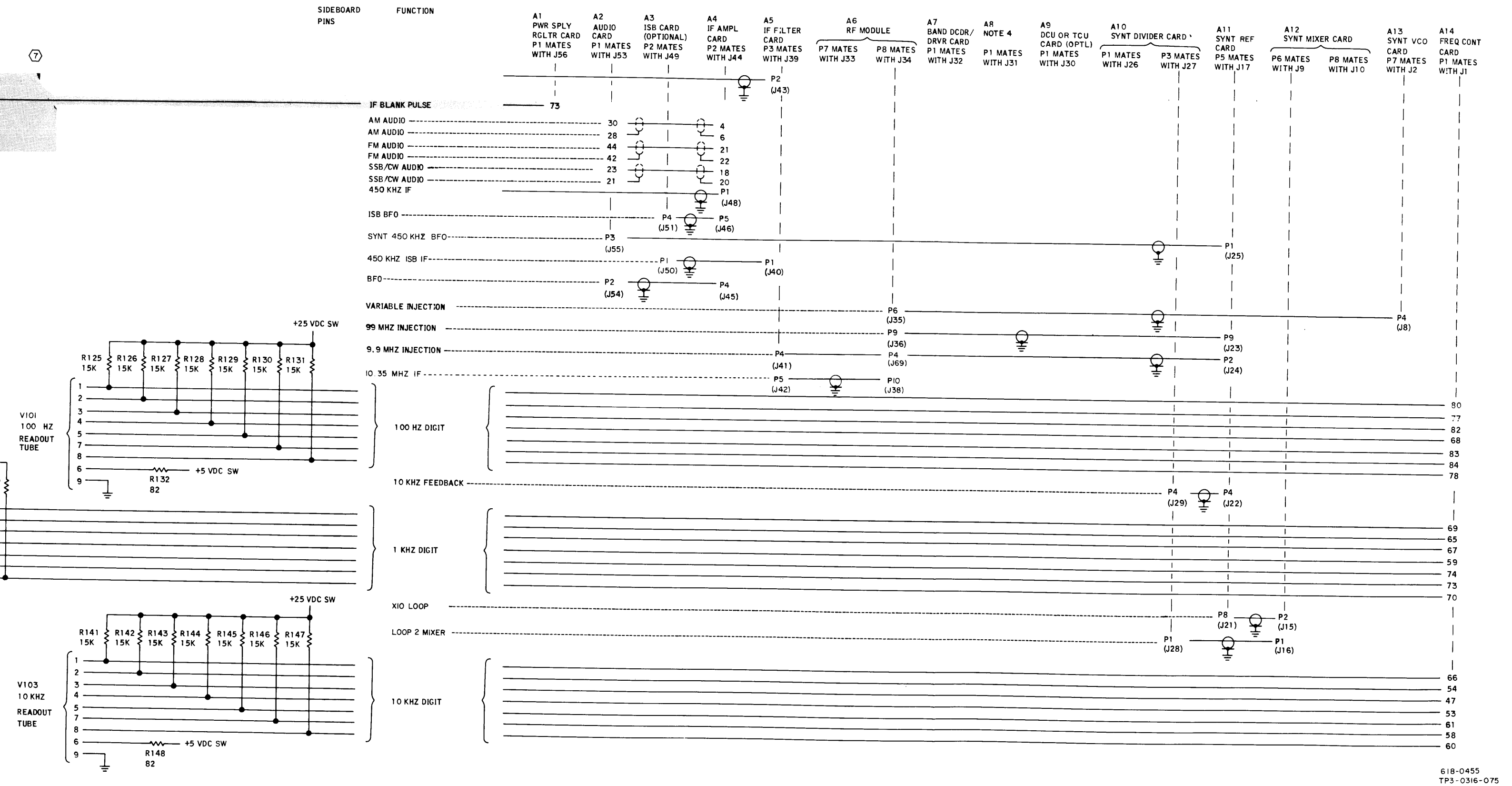
REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R18 changed to R189 (25 kΩ). R188 added (12 kΩ). To improve squelch control.		72244
B	CR207 and CR208 changed to 1N5550's.		72304
C	Speaker amplifier circuit card (TB104) replaced with new speaker amplifier card (TB104). If blanker circuit deleted.		72354
D	Jumper deleted between J30-46 and J31-47. Jumper added between J31-47 and J30-25. Makes 651S-1A compatible with serial control systems.		651S-1A only Effectivity MCN 757

Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet A)

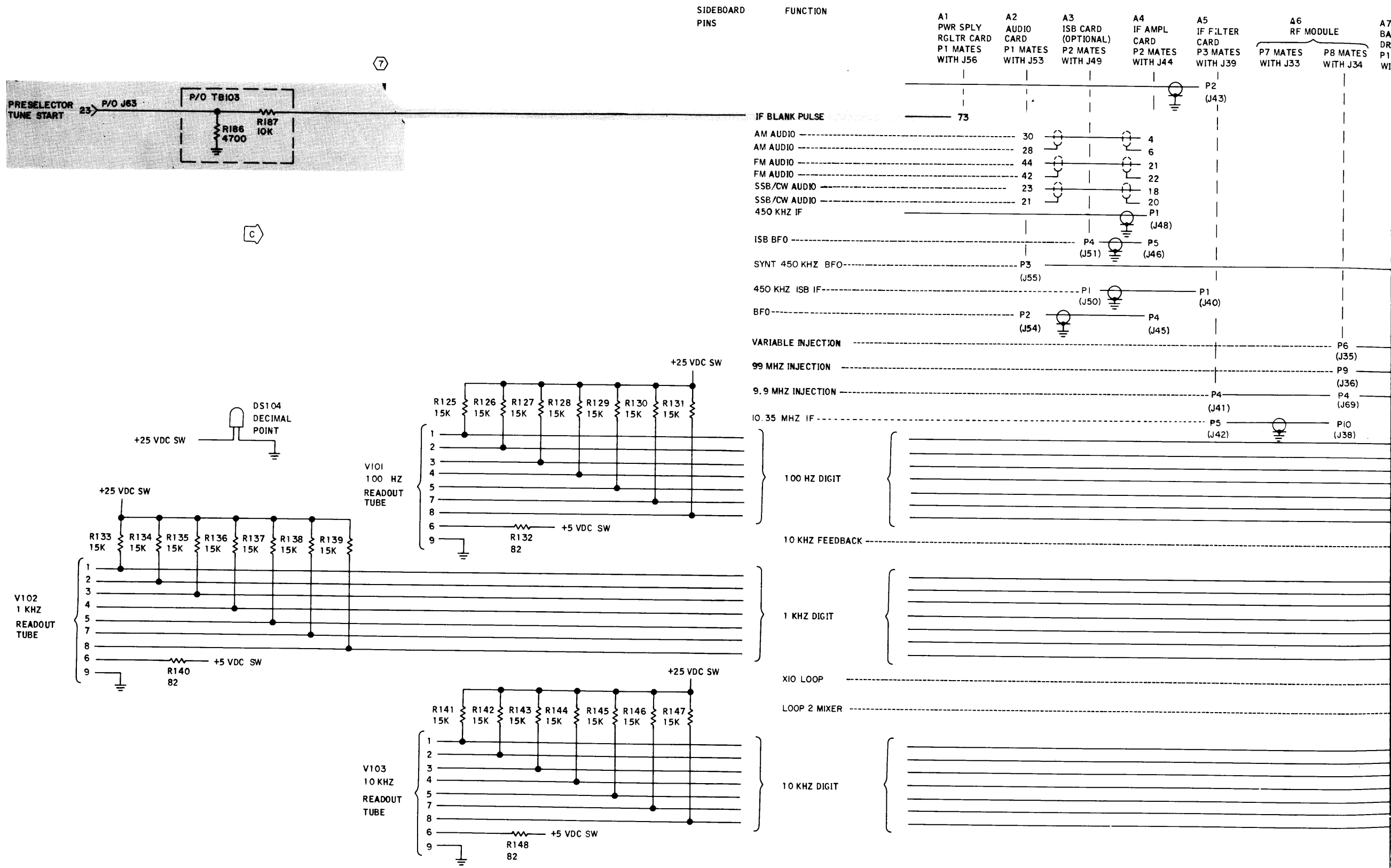


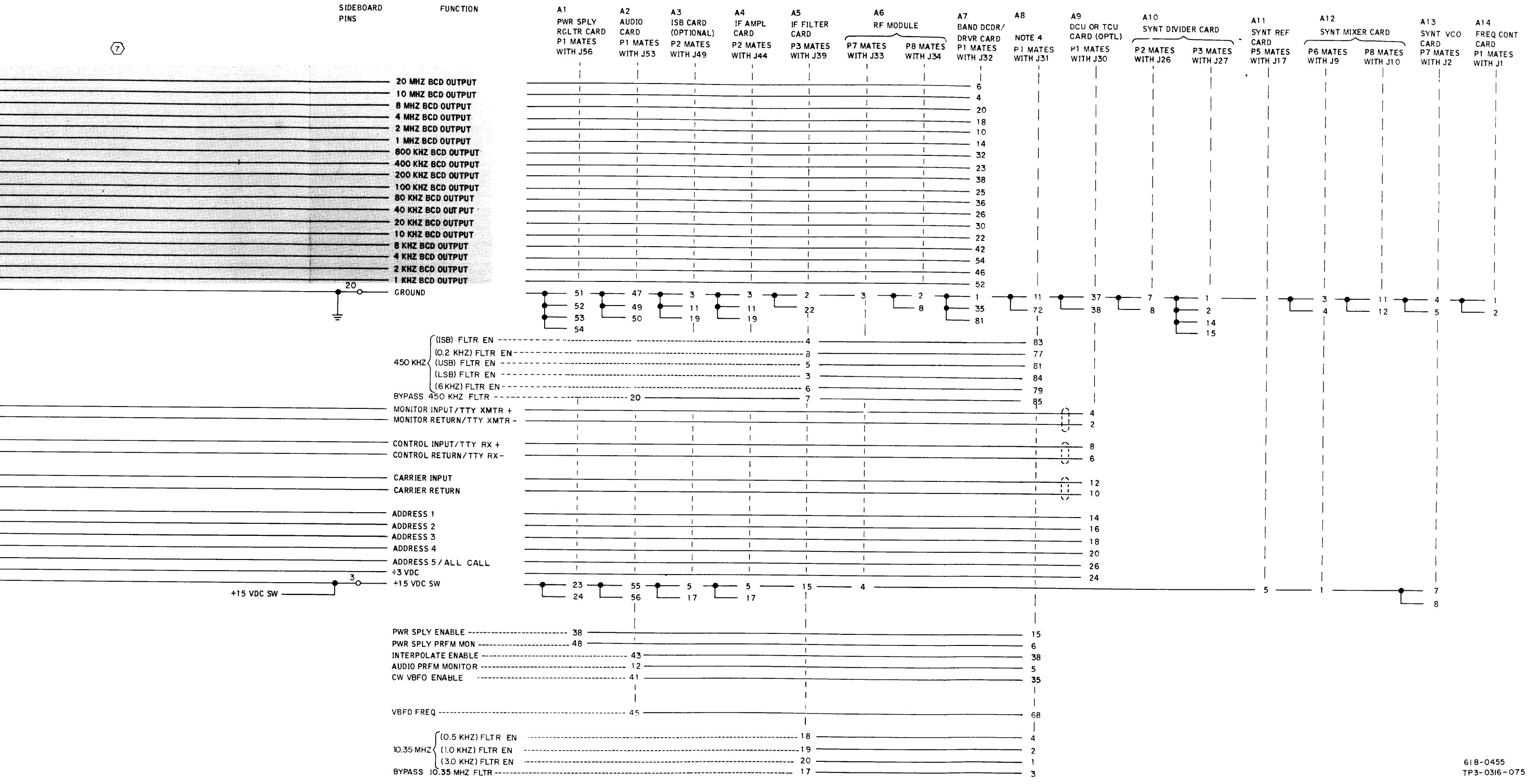
Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 1 of 7)


SIDEBOARD PINS
FUNCTION
A1 PWR SPLY RGLTR CARD P1 MATES WITH J56
A2 AUDIO CARD P1 MATES WITH J53
A3 ISB CARD (OPTIONAL) P2 MATES WITH J49
A4 IF AMPL CARD P2 MATES WITH J44
A5 IF FILTER CARD P3 MATES WITH J39
A6 RF MODULE
P7 MATES WITH J33
P8 M WITH
S102A FRONT (SEE SHEET 6 FOR REAR)
S101A REAR (SEE SHEET 6 FOR FRONT)
TB104
SQUELCH
SQUELCH LEVEL
SQUELCH ON-OFF
CCW R189 25K
OFF (CCW)
S114
R188 22K
AF GAIN
R175 10K CCW
AUDIO OUT (TO VOL CONT)
+25 VDC SW
R183 100
J58
HIGH - Z HEADPHONE OUTPUT
R174 100
J64
SPEAKER OUTPUT 8 OHM
C9 500 UF
C10 500 UF
C8 0.1 UF
R18 470
Q4 2N3766
R16 1
R17 1
CR1 1N4003
R11 330
R10 100
C11 0.1 UF
C6 330 UF
R9 220
R3 10K
R15 10
C12 0.1 UF
C4 22 UF
R7 180
C3 0.1 UF
R4 1800
C2 22 UF
R12 2200
C7 270 PF
Q5 2N3740
Q3 2N3766
Q2 2N2907A
Q1 2N2222A
R1 270K
C1 0.47 UF
R13 470
C5 22 UF
R2 22K
R14 220
R8 2200
R6 8200
R5 470
C13 1000 UF
R19 15
+15 VDC CONT
-15 VDC CONT
-15 VDC SW
+25 VDC SW
R149 15K
R150 15K
R151 15K
R152 15K
R153 15K
R154 15K
R155 15K
V104 100 KHZ READOUT NOTE 3
R156 82
+5 VDC SW
100 KHZ DIGIT
DS105 COMMA
COMMA ENABLE
+25 VDC SW
R157 15K
R158 15K
R159 15K
R160 15K
R161 15K
R162 15K
R163 15K
V105 1 MHZ READOUT TUBE NOTE 3
R164 82
+5 VDC SW
1 MHZ DIGIT
+25 VDC SW
R165 15K
R166 15K
R167 15K
R168 15K
R169 15K
R170 15K
R171 15K
V106 10 MHZ READOUT TUBE NOTE 3
R172 82
+5 VDC SW
10 MHZ DIGIT

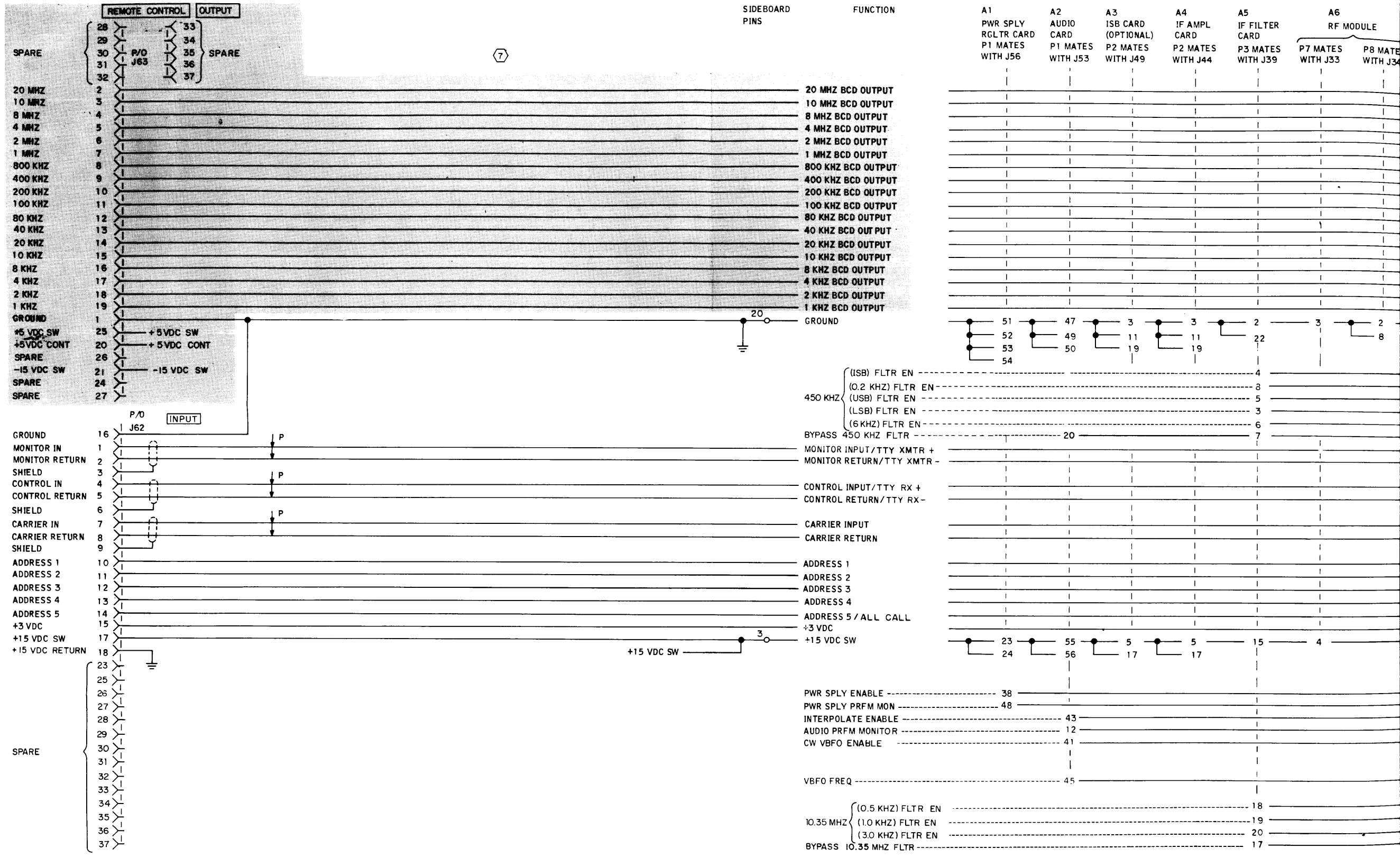


Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 2 of 7)


SIDEBOARD PINS
FUNCTION
A1 PWR SPLY RGLTR CARD P1 MATES WITH J56
A2 AUDIO CARD P1 MATES WITH J53
A3 ISB CARD (OPTIONAL) P2 MATES WITH J49
A4 IF AMPL CARD P2 MATES WITH J44
A5 IF FILTER CARD P3 MATES WITH J39
A6 RF MODULE
P7 MATES WITH J33
P8 MATES WITH J34
7
PRESELECTOR TUNE START
23
P/O J63
P/O TB103
R186 4700
R187 10K
IF BLANK PULSE
73
AM AUDIO
30
4
AM AUDIO
28
6
FM AUDIO
44
21
FM AUDIO
42
22
SSB/CW AUDIO
23
18
SSB/CW AUDIO
21
20
450 KHZ IF
P1 (J48)
P2 (J43)
C
ISB BFO
P4 (J51)
P5 (J46)
SYNT 450 KHZ BFO
P3 (J55)
450 KHZ ISB IF
P1 (J50)
P1 (J40)
BFO
P2 (J54)
P4 (J45)
VARIABLE INJECTION
P6 (J35)
99 MHZ INJECTION
P9 (J36)
9.9 MHZ INJECTION
P4 (J41)
P4 (J69)
10.35 MHZ IF
P5 (J42)
P10 (J38)
DS104 DECIMAL POINT
+25 VDC SW
V101 100 HZ READOUT TUBE
R125 15K
R126 15K
R127 15K
R128 15K
R129 15K
R130 15K
R131 15K
R132 82
+5 VDC SW
100 HZ DIGIT
10 KHZ FEEDBACK
R133 15K
R134 15K
R135 15K
R136 15K
R137 15K
R138 15K
R139 15K
R140 82
V102 1 KHZ READOUT TUBE
1 KHZ DIGIT
XIO LOOP
LOOP 2 MIXER
R141 15K
R142 15K
R143 15K
R144 15K
R145 15K
R146 15K
R147 15K
R148 82
V103 10 KHZ READOUT TUBE
10 KHZ DIGIT



Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 3 of 7)

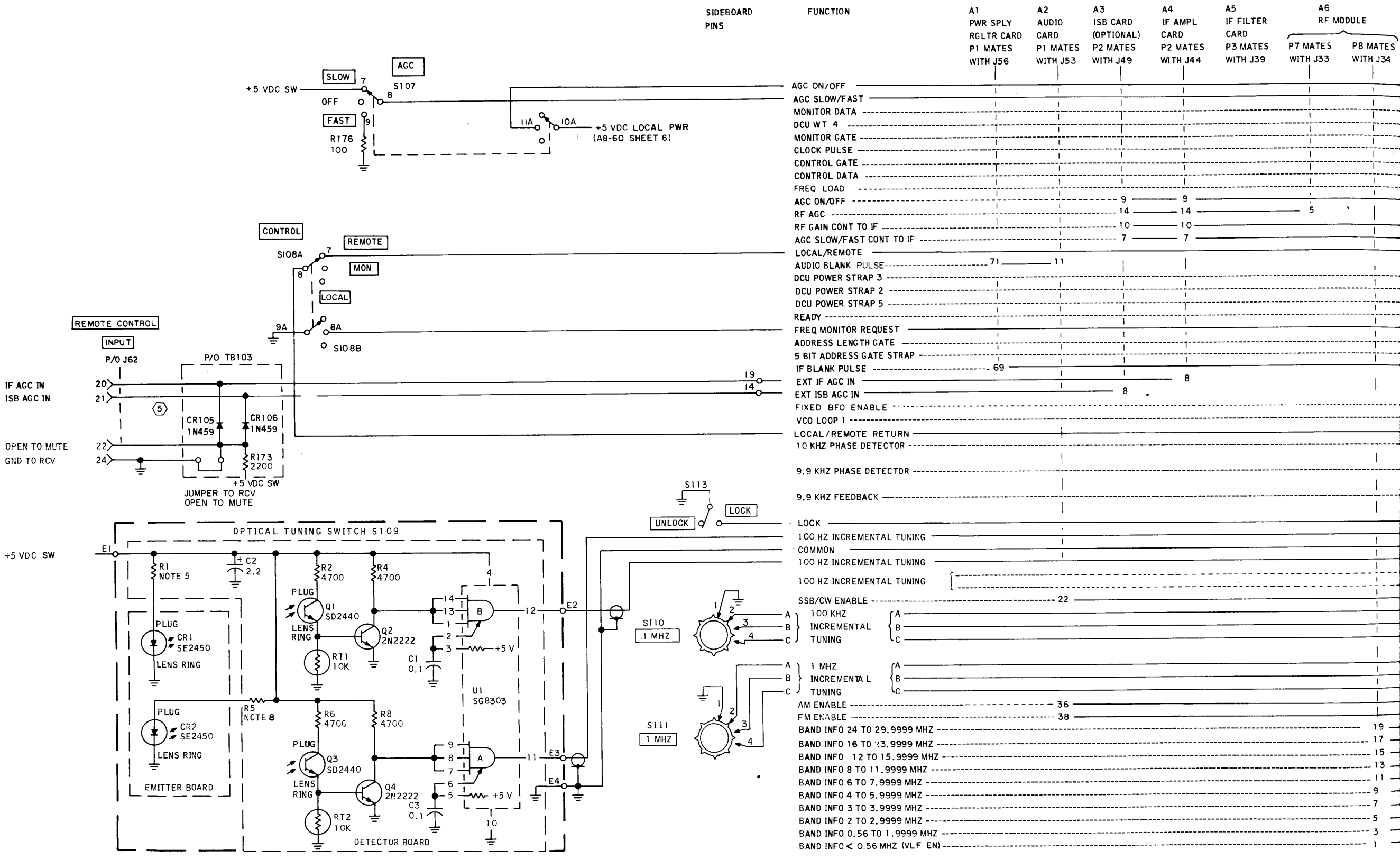

REMOTE CONTROL
OUTPUT
SPARE
P/O J63
SPARE
20 MHZ 2
10 MHZ 3
8 MHZ 4
4 MHZ 5
2 MHZ 6
1 MHZ 7
800 KHZ 8
400 KHZ 9
200 KHZ 10
100 KHZ 11
80 KHZ 12
40 KHZ 13
20 KHZ 14
10 KHZ 15
8 KHZ 16
4 KHZ 17
2 KHZ 18
1 KHZ 19
GROUND 1
+5 VDC SW 25
+5VDC CONT 20
SPARE 26
-15 VDC SW 21
SPARE 24
SPARE 27
+5 VDC SW
+5 VDC CONT
-15 VDC SW
7
SIDEBOARD PINS
FUNCTION
20 MHZ BCD OUTPUT
10 MHZ BCD OUTPUT
8 MHZ BCD OUTPUT
4 MHZ BCD OUTPUT
2 MHZ BCD OUTPUT
1 MHZ BCD OUTPUT
800 KHZ BCD OUTPUT
400 KHZ BCD OUTPUT
200 KHZ BCD OUTPUT
100 KHZ BCD OUTPUT
80 KHZ BCD OUTPUT
40 KHZ BCD OUTPUT
20 KHZ BCD OUTPUT
10 KHZ BCD OUTPUT
8 KHZ BCD OUTPUT
4 KHZ BCD OUTPUT
2 KHZ BCD OUTPUT
1 KHZ BCD OUTPUT
20
GROUND
A1 PWR SPLY RGLTR CARD P1 MATES WITH J56
A2 AUDIO CARD P1 MATES WITH J53
A3 ISB CARD (OPTIONAL) P2 MATES WITH J49
A4 IF AMPL CARD P2 MATES WITH J44
A5 IF FILTER CARD P3 MATES WITH J39
A6 RF MODULE
P7 MATES WITH J33
P8 MATES WITH J34
51 52 53 54
47 49 50
3 11 19
3 11 19
2 22
3
2 8
P/O J62
INPUT
GROUND 16
MONITOR IN 1
MONITOR RETURN 2
SHIELD 3
CONTROL IN 4
CONTROL RETURN 5
SHIELD 6
CARRIER IN 7
CARRIER RETURN 8
SHIELD 9
ADDRESS 1 10
ADDRESS 2 11
ADDRESS 3 12
ADDRESS 4 13
ADDRESS 5 14
+3 VDC 15
+15 VDC SW 17
+15 VDC RETURN 18
P
P
P
MONITOR INPUT/TTY XMTR +
MONITOR RETURN/TTY XMTR -
CONTROL INPUT/TTY RX +
CONTROL RETURN/TTY RX -
CARRIER INPUT
CARRIER RETURN
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4
ADDRESS 5 / ALL CALL
+3 VDC
+15 VDC SW
3
+15 VDC SW
23 24
55 56
5 17
5 17
15
4
SPARE 23 25 26 27 28 29 30 31 32 33 34 35 36 37
450 KHZ
(ISB) FLTR EN 4
(0.2 KHZ) FLTR EN 8
(USB) FLTR EN 5
(LSB) FLTR EN 3
(6 KHZ) FLTR EN 6
BYPASS 450 KHZ FLTR 20 7
PWR SPLY ENABLE 38
PWR SPLY PRFM MON 48
INTERPOLATE ENABLE 43
AUDIO PRFM MONITOR 12
CW VBFO ENABLE 41
VBFO FREQ 45
10.35 MHZ
(0.5 KHZ) FLTR EN 18
(1.0 KHZ) FLTR EN 19
(3.0 KHZ) FLTR EN 20
BYPASS 10.35 MHZ FLTR 17

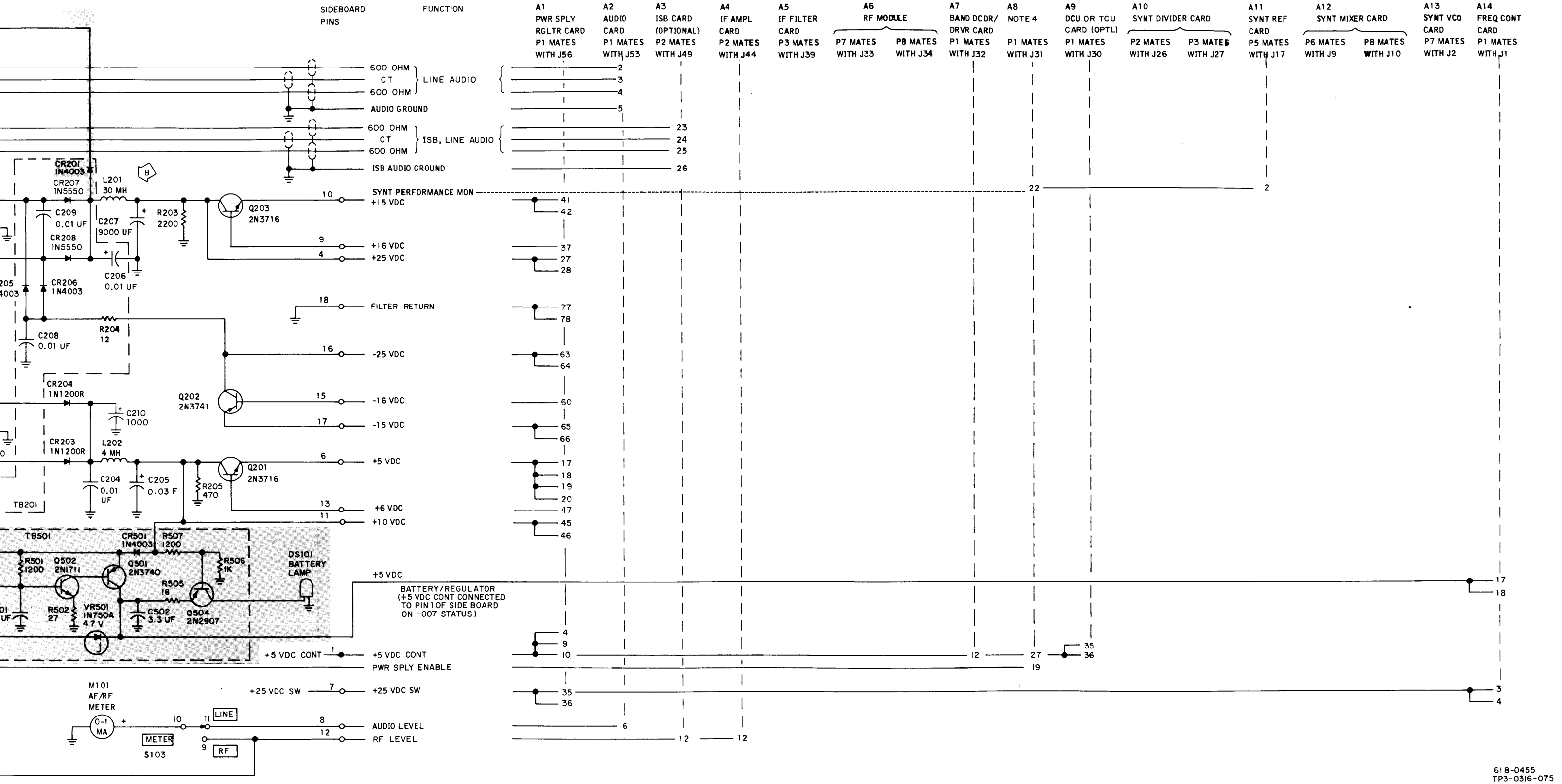
FUNCTION	SIDEBOARD PINS	A1 PWR SPLY RGLTR CARD P1 MATES WITH J56	A2 AUDIO CARD P1 MATES WITH J53	A3 ISB CARD (OPTIONAL) P2 MATES WITH J49	A4 IF AMPL CARD P2 MATES WITH J44	A5 IF FILTER CARD P3 MATES WITH J39	A6 RF MODULE P7 MATES WITH J33	A6 RF MODULE P8 MATES WITH J34	A7 BAND DCDR/ DRVR CARD P1 MATES WITH J32	A8 NOTE 4 P1 MATES WITH J31	A9 DCU OR TCU CARD (OPTL) P1 MATES WITH J30	A10 SYNT DIVIDER CARD P2 MATES WITH J26	A10 SYNT DIVIDER CARD P3 MATES WITH J27	A11 SYNT REF CARD P5 MATES WITH J17	A12 SYNT MIXER CARD P6 MATES WITH J9	A12 SYNT MIXER CARD P8 MATES WITH J10	A13 SYNT VCO CARD P7 MATES WITH J2	A14 FREQ CONT CARD P1 MATES WITH J1
AGC ON/OFF										44								
AGC SLOW/FAST										55								
MONITOR DATA										12	21							
DCU WT 4										13	11							
MONITOR GATE										14	13							
CLOCK PULSE										16	19							
CONTROL GATE										17	17							
CONTROL DATA										18	23							
FREQ LOAD										30								64
AGC ON/OFF				9	9					24								
RF AGC				14	14		5			11	C405 4.7 UF							
RF GAIN CONT TO IF				10	10					64								
AGC SLOW/FAST CONT TO IF				7	7					56								
LOCAL/REMOTE										7	15,47							57
AUDIO BLANK PULSE		71	11															
DCU POWER STRAP 3											39							
DCU POWER STRAP 2											41							
DCU POWER STRAP 5											40							
READY											27							
FREQ MONITOR REQUEST										8								
ADDRESS LENGTH GATE											28							
5 BIT ADDRESS GATE STRAP											7							
IF BLANK PULSE		69									9							6
EXT IF AGC IN	19				8													
EXT ISB AGC IN	14			8														
FIXED BFO ENABLE										37				4				
VCO LOOP 1																P5 (J13)	P5 (J5)	
LOCAL/REMOTE RETURN										10								
10 KHZ PHASE DETECTOR														P3 (J18)			P1 (J6)	
9.9 KHZ PHASE DETECTOR														P6 (J19)			P6 (J7)	
9.9 KHZ FEEDBACK														P7 (J20)			P7 (J14)	
LOCK											42,43							5
100 HZ INCREMENTAL TUNING											29							
COMMON																		
100 HZ INCREMENTAL TUNING											32							
100 HZ INCREMENTAL TUNING											31							85
											34							86
SSB/CW ENABLE										25								
100 KHZ INCREMENTAL TUNING A																		15
100 KHZ INCREMENTAL TUNING B																		14
100 KHZ INCREMENTAL TUNING C																		13
1 MHZ INCREMENTAL TUNING A																		9
1 MHZ INCREMENTAL TUNING B																		11
1 MHZ INCREMENTAL TUNING C																		8
AM ENABLE				36						23								
FM ENABLE				38						21								
BAND INFO 24 TO 29.9999 MHZ							19		62									
BAND INFO 16 TO 23.9999 MHZ							17		45									
BAND INFO 12 TO 15.9999 MHZ							15		64									
BAND INFO 8 TO 11.9999 MHZ							13		72									
BAND INFO 6 TO 7.9999 MHZ							11		43									
BAND INFO 4 TO 5.9999 MHZ							9		60									
BAND INFO 3 TO 3.9999 MHZ							7		44									
BAND INFO 2 TO 2.9999 MHZ							5		56									
BAND INFO 0.56 TO 1.9999 MHZ							3		84									
BAND INFO < 0.56 MHZ (VLF EN)							1		86	8								

AGC
S107
8
11A
10A
+5 VDC LOCAL PWR (A8-60 SHEET 6)
OTE
19
14
S109
R4 4700
4
14
13
1
B
12
E2
2
3
+5 V
Q2 2N2222
C1 0.1
U1 SG8303
R8 4700
9
8
7
A
11
E3
6
5
+5 V
Q4 2N2222
C3 0.1
10
E4
ECTOR BOARD
S113
UNLOCK
LOCK
S110 .1 MHZ
S111 1 MHZ
1
2
3
4
A
B
C

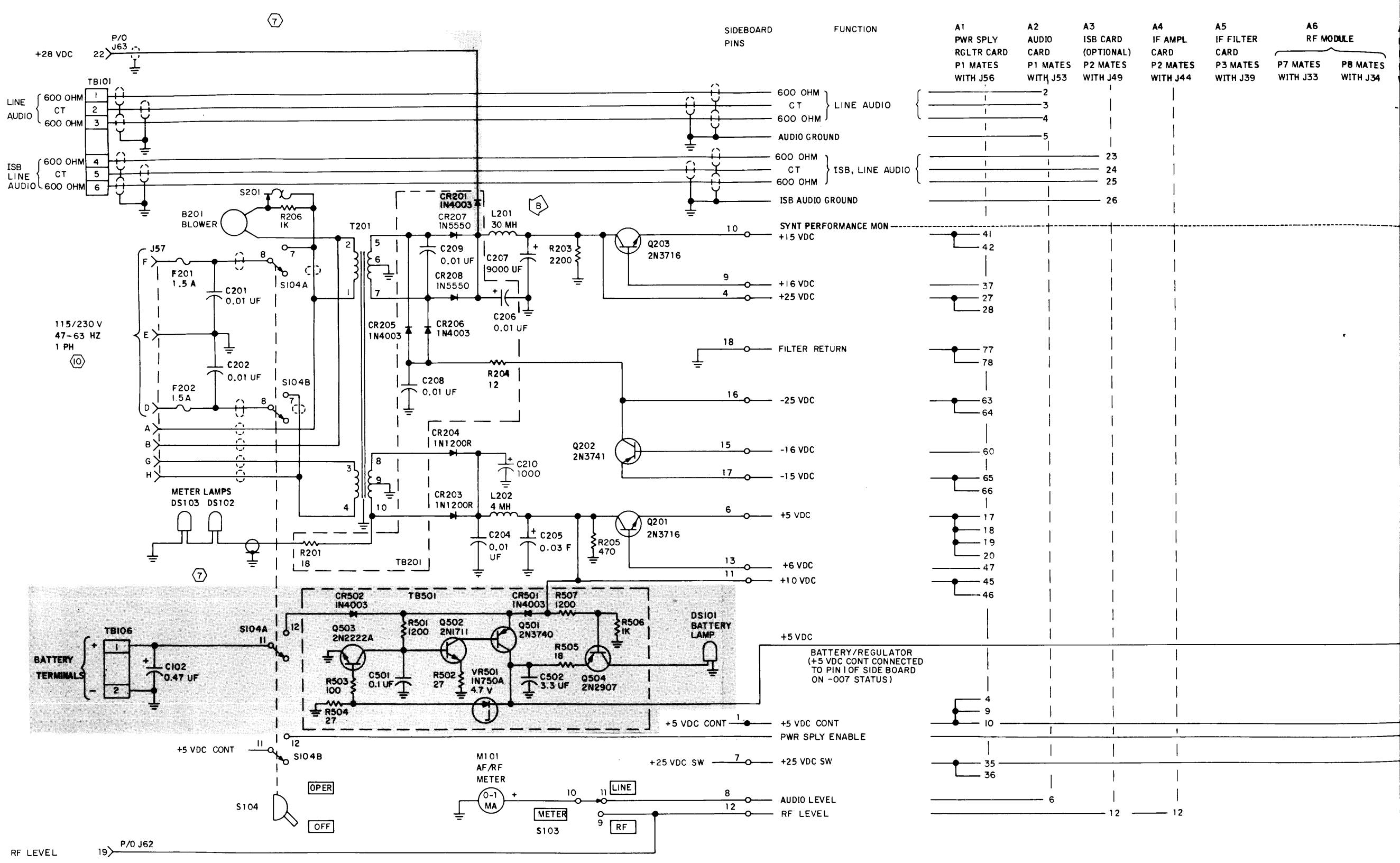
618-0455
TP3-0316-075

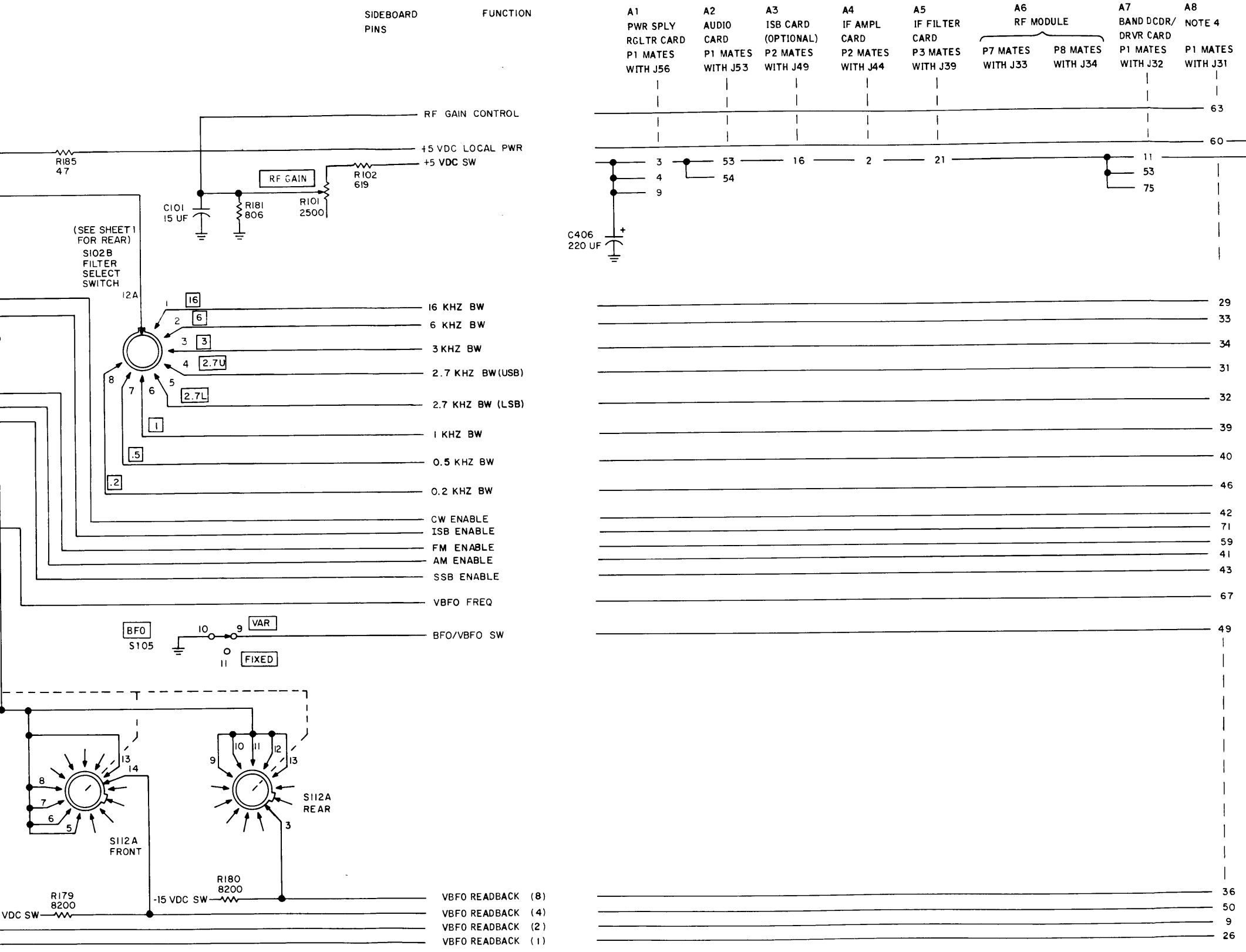
Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 4 of 7)


SIDEBOARD PINS
FUNCTION
A1 PWR SPLY RGLTR CARD P1 MATES WITH J56
A2 AUDIO CARD P1 MATES WITH J53
A3 ISB CARD (OPTIONAL) P2 MATES WITH J49
A4 IF AMPL CARD P2 MATES WITH J44
A5 IF FILTER CARD P3 MATES WITH J39
A6 RF MODULE P7 MATES WITH J33
A6 RF MODULE P8 MATES WITH J34
AGC ON/OFF
AGC SLOW/FAST
MONITOR DATA
DCU WT 4
MONITOR GATE
CLOCK PULSE
CONTROL GATE
CONTROL DATA
FREQ LOAD
AGC ON/OFF 9 9
RF AGC 14 14 5
RF GAIN CONT TO IF 10 10
AGC SLOW/FAST CONT TO IF 7 7
LOCAL/REMOTE
AUDIO BLANK PULSE 71 11
DCU POWER STRAP 3
DCU POWER STRAP 2
DCU POWER STRAP 5
READY
FREQ MONITOR REQUEST
ADDRESS LENGTH GATE
5 BIT ADDRESS GATE STRAP
IF BLANK PULSE 69
EXT IF AGC IN 8
EXT ISB AGC IN 8
FIXED BFO ENABLE
VCO LOOP 1
LOCAL/REMOTE RETURN
10 KHZ PHASE DETECTOR
9.9 KHZ PHASE DETECTOR
9.9 KHZ FEEDBACK
LOCK
100 HZ INCREMENTAL TUNING
COMMON
100 HZ INCREMENTAL TUNING
100 HZ INCREMENTAL TUNING
SSB/CW ENABLE 22
100 KHZ INCREMENTAL TUNING A B C
1 MHZ INCREMENTAL TUNING A B C
AM ENABLE 36
FM ENABLE 38
BAND INFO 24 TO 29.9999 MHZ 19
BAND INFO 16 TO 23.9999 MHZ 17
BAND INFO 12 TO 15.9999 MHZ 15
BAND INFO 8 TO 11.9999 MHZ 13
BAND INFO 6 TO 7.9999 MHZ 11
BAND INFO 4 TO 5.9999 MHZ 9
BAND INFO 3 TO 3.9999 MHZ 7
BAND INFO 2 TO 2.9999 MHZ 5
BAND INFO 0.56 TO 1.9999 MHZ 3
BAND INFO < 0.56 MHZ (VLF EN) 1
+5 VDC SW
SLOW
FAST
OFF
AGC
S107
R176 100
11A
10A
+5 VDC LOCAL PWR (A8-60 SHEET 6)
CONTROL
S108A
REMOTE
MON
LOCAL
S108B
REMOTE CONTROL
INPUT
P/O J62
P/O TB103
IF AGC IN
ISB AGC IN
OPEN TO MUTE
GND TO RCV
CR105 1N459
CR106 1N459
R173 2200
+5 VDC SW
JUMPER TO RCV
OPEN TO MUTE
S113
UNLOCK
LOCK
S110
.1 MHZ
S111
1 MHZ
OPTICAL TUNING SWITCH S109
+5 VDC SW
R1 NOTE 5
C2 2.2
R2 4700
R4 4700
Q1 SD2440
Q2 2N2222
RT1 10K
C1 0.1
U1 SG8303
+5 V
R5 NOTE 8
R6 4700
R8 4700
Q3 SD2440
Q4 2N2222
RT2 10K
C3 0.1
CR1 SE2450
CR2 SE2450
LENS RING
PLUG
EMITTER BOARD
DETECTOR BOARD



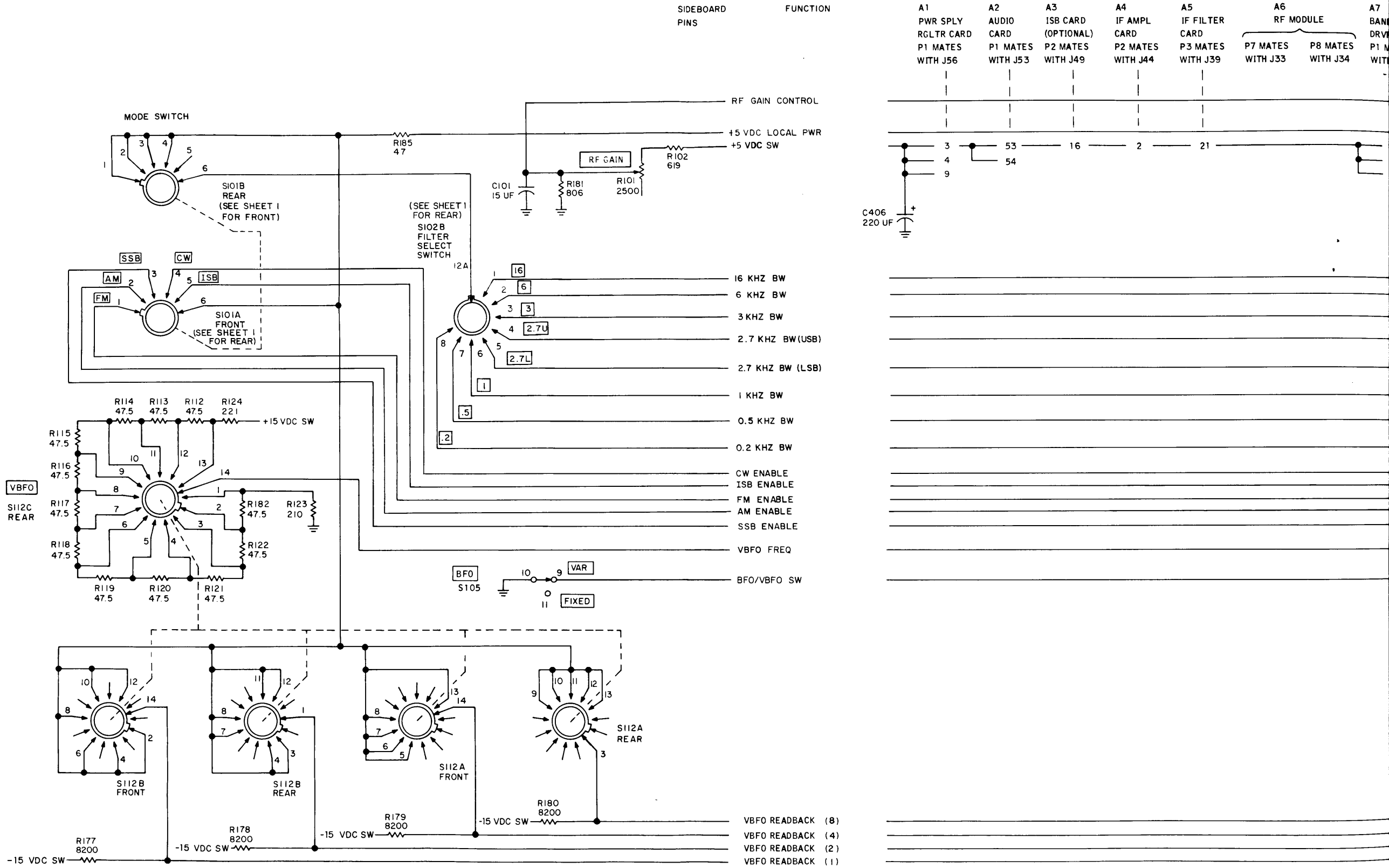
Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 5 of 7)

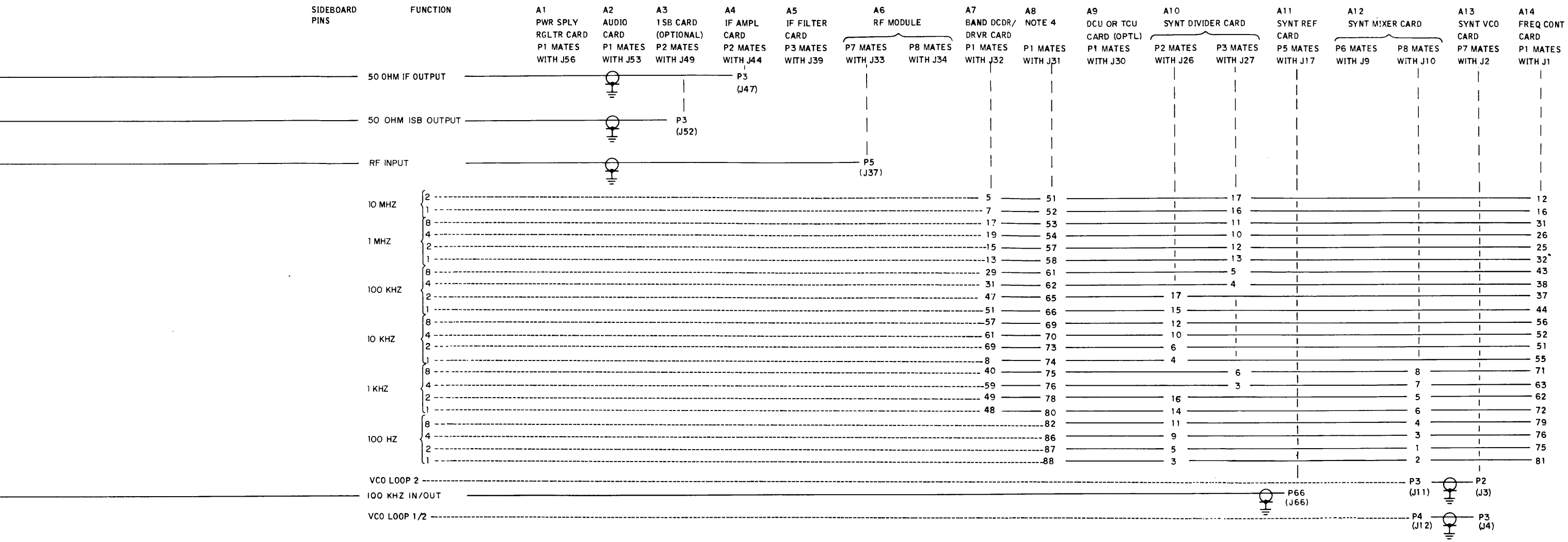

SIDEBOARD PINS
FUNCTION
A1 PWR SPLY RGLTR CARD P1 MATES WITH J56
A2 AUDIO CARD P1 MATES WITH J53
A3 ISB CARD (OPTIONAL) P2 MATES WITH J49
A4 IF AMPL CARD P2 MATES WITH J44
A5 IF FILTER CARD P3 MATES WITH J39
A6 RF MODULE P7 MATES WITH J33
A6 RF MODULE P8 MATES WITH J34
+28 VDC
P/O J63
22
TB101
LINE AUDIO
600 OHM
CT
600 OHM
1
2
3
ISB LINE AUDIO
600 OHM
CT
600 OHM
4
5
6
600 OHM
CT
600 OHM
LINE AUDIO
AUDIO GROUND
ISB, LINE AUDIO
ISB AUDIO GROUND
SYNT PERFORMANCE MON
+15 VDC
+16 VDC
+25 VDC
FILTER RETURN
-25 VDC
-16 VDC
-15 VDC
+5 VDC
+6 VDC
+10 VDC
+5 VDC
BATTERY/REGULATOR (+5 VDC CONT CONNECTED TO PIN 1 OF SIDE BOARD ON -007 STATUS)
+5 VDC CONT
PWR SPLY ENABLE
+25 VDC SW
AUDIO LEVEL
RF LEVEL
RF LEVEL
P/O J62
19
S201
B201 BLOWER
R206 1K
CR201 IN4003
CR207 1N5550
L201 30 MH
T201
C209 0.01 UF
CR208 1N5550
C207 9000 UF
R203 2200
Q203 2N3716
C206 0.01 UF
CR205 1N4003
CR206 1N4003
R204 12
C208 0.01 UF
J57
F201 1.5 A
C201 0.01 UF
S104A
115/230 V 47-63 HZ 1 PH
C202 0.01 UF
F202 1.5A
S104B
METER LAMPS DS103 DS102
R201 18
TB201
CR204 1N1200R
C210 1000
Q202 2N3741
CR203 1N1200R
L202 4 MH
C204 0.01 UF
C205 0.03 F
R205 470
Q201 2N3716
CR502 IN4003
TB501
CR501 IN4003
R507 1200
TB106
BATTERY TERMINALS
C102 0.47 UF
Q503 2N2222A
R501 1200
Q502 2N1711
Q501 2N3740
R506 1K
DS101 BATTERY LAMP
R505 18
R503 100
C501 0.1 UF
R502 27
VR501 IN750A 4.7 V
C502 3.3 UF
Q504 2N2907
R504 27
S104
OPER
OFF
M101 AF/RF METER
0-1 MA
LINE
METER
RF
S103



618-0455
TP3-0316-075

Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 6 of 7)


SIDEBOARD PINS
FUNCTION
A1 PWR SPLY RGLTR CARD P1 MATES WITH J56
A2 AUDIO CARD P1 MATES WITH J53
A3 ISB CARD (OPTIONAL) P2 MATES WITH J49
A4 IF AMPL CARD P2 MATES WITH J44
A5 IF FILTER CARD P3 MATES WITH J39
A6 RF MODULE
P7 MATES WITH J33
P8 MATES WITH J34
A7 BAND DRVR P1 MATES WITH
MODE SWITCH
S101B REAR (SEE SHEET 1 FOR FRONT)
S101A FRONT (SEE SHEET 1 FOR REAR)
SSB
CW
AM
ISB
FM
R185 47
RF GAIN CONTROL
+5 VDC LOCAL PWR
+5 VDC SW
RF GAIN
R102 619
R101 2500
R181 806
C101 15 UF
C406 220 UF
(SEE SHEET 1 FOR REAR)
S102B FILTER SELECT SWITCH
16 KHZ BW
6 KHZ BW
3 KHZ BW
2.7 KHZ BW(USB)
2.7 KHZ BW (LSB)
1 KHZ BW
0.5 KHZ BW
0.2 KHZ BW
CW ENABLE
ISB ENABLE
FM ENABLE
AM ENABLE
SSB ENABLE
VBFO FREQ
BFO S105
VAR
FIXED
BFO/VBFO SW
VBFO S112C REAR
R114 47.5
R113 47.5
R112 47.5
R124 221
+15 VDC SW
R115 47.5
R116 47.5
R117 47.5
R118 47.5
R182 47.5
R123 210
R122 47.5
R119 47.5
R120 47.5
R121 47.5
S112B FRONT
S112B REAR
S112A FRONT
S112A REAR
R177 8200
R178 8200
R179 8200
R180 8200
-15 VDC SW
VBFO READBACK (8)
VBFO READBACK (4)
VBFO READBACK (2)
VBFO READBACK (1)



E SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS,
ES ARE IN PICOFARADS.

NTS IN THE 0 THRU 99 SERIES ARE PART OF AUDIO AMPL CIRCUITS.
E 100 THRU 199 SERIES ARE PART OF FRONT PANEL CIRCUITS.
E 200 THRU 299 SERIES ARE PART OF REAR PANEL CIRCUITS.

YPICAL READOUT TUBE
NABLEING PINS SHOWN)

(4) STANDARD A8 CARD IS INTERCONNECT CARD. IF REMOTE CONTROL IS EMPLOYED A8 WILL BE A DCFE CARD.

(5) CR105, CR106 DELETED ON CPN 606-9423-006/009.

(6) SQUELCH OPTION AVAILABLE ON 606-9423-005 ONLY.

(7) CIRCUITS ENCLOSED IN GRAY AREAS ARE DELETED ON CPN 606-9423-007/009.

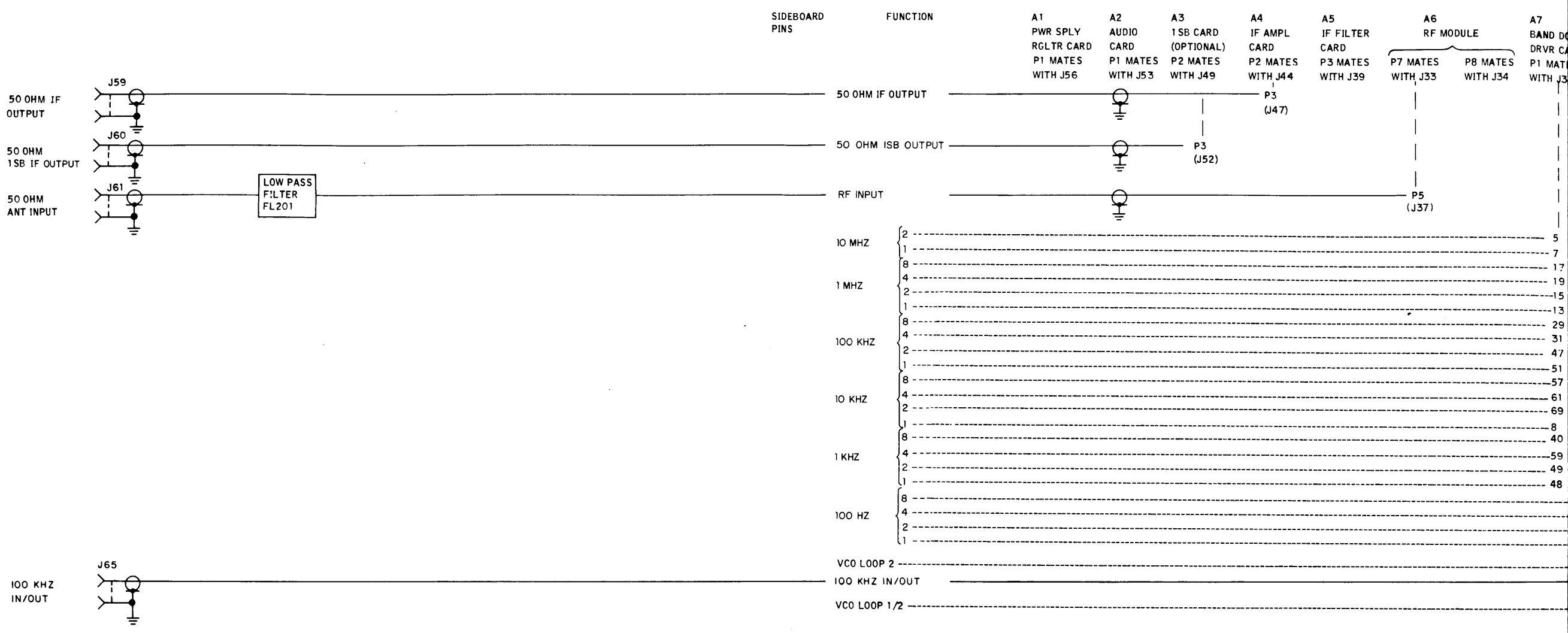
(8) TEST SELECT COMPONENT

(9) 6515-1A ONLY EFFECTIVITY MCN 756 AND BELOW. J30-46 IS STRAPPED TO J31-47. STRAP MUST BE REMOVED FOR SERIAL CONTROL (DCU, DCFE) OPERATION.

(10) FOR 230V 47 TO 63 HZ 1 PH INPUT, F201 AND F202 SHOULD BE 0.75A.

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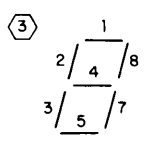
Chassis/Sideboard, Schematic Diagram
Figure 2 (Sheet 7 of 7)



NOTES:

(1) UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN PICOFARADS.

(2) CHASSIS COMPONENTS IN THE 0 THRU 99 SERIES ARE PART OF AUDIO AMPL CIRCUITS. COMPONENTS IN THE 100 THRU 199 SERIES ARE PART OF FRONT PANEL CIRCUITS. COMPONENTS IN THE 200 THRU 299 SERIES ARE PART OF REAR PANEL CIRCUITS.

(3) 

TYPICAL READOUT TUBE (ENABLEING PINS SHOWN)

(4) STANDARD A8 CARD IS INTERCONNECT CARD. IF REMOTE CONTROL IS EMPLOYED A8 WILL BE A DCFE CARD.

(5) CR105, CR106 DELETED ON CPN 606-9423-006/009.

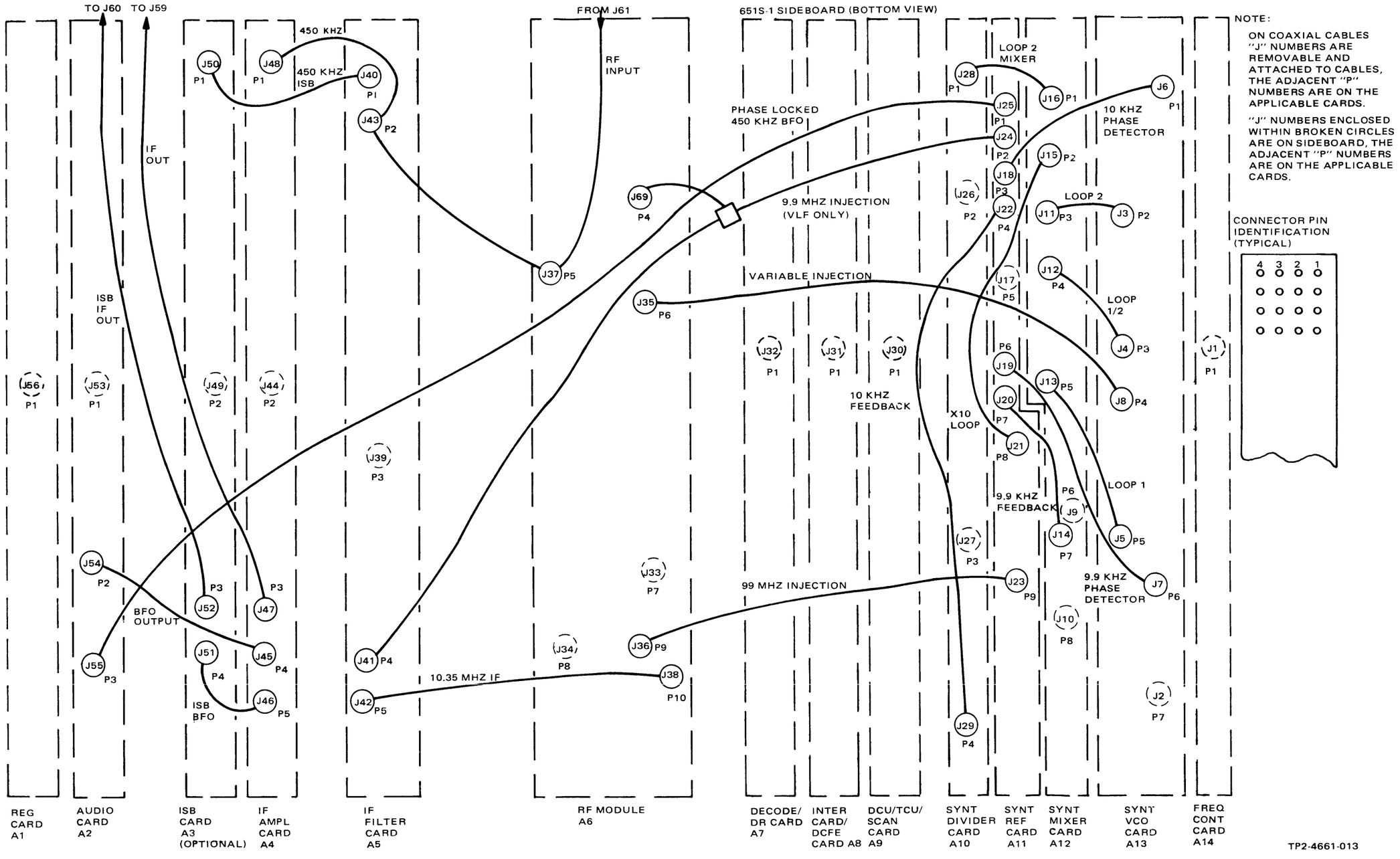
(6) SQUELCH OPTION AVAILABLE ON 606-9423-005 ONLY.

(7) CIRCUITS ENCLOSED IN GRAY AREAS ARE DELETED ON CPN 606-9423-007/009.

(8) TEST SELECT COMPONENT

(9) 6515-1A ONLY EFFECTIVITY MCN 756 AND BELOW. J30-46 IS STRAPPED TO J31-47. STRAP MUST BE REMOVED FOR SERIAL CONTROL (DCU, DCFE) OPERATION.

(10) FOR 230V 47 TO 63 HZ 1 PH INPUT, F201 AND F202 SHOULD BE 0.75A.

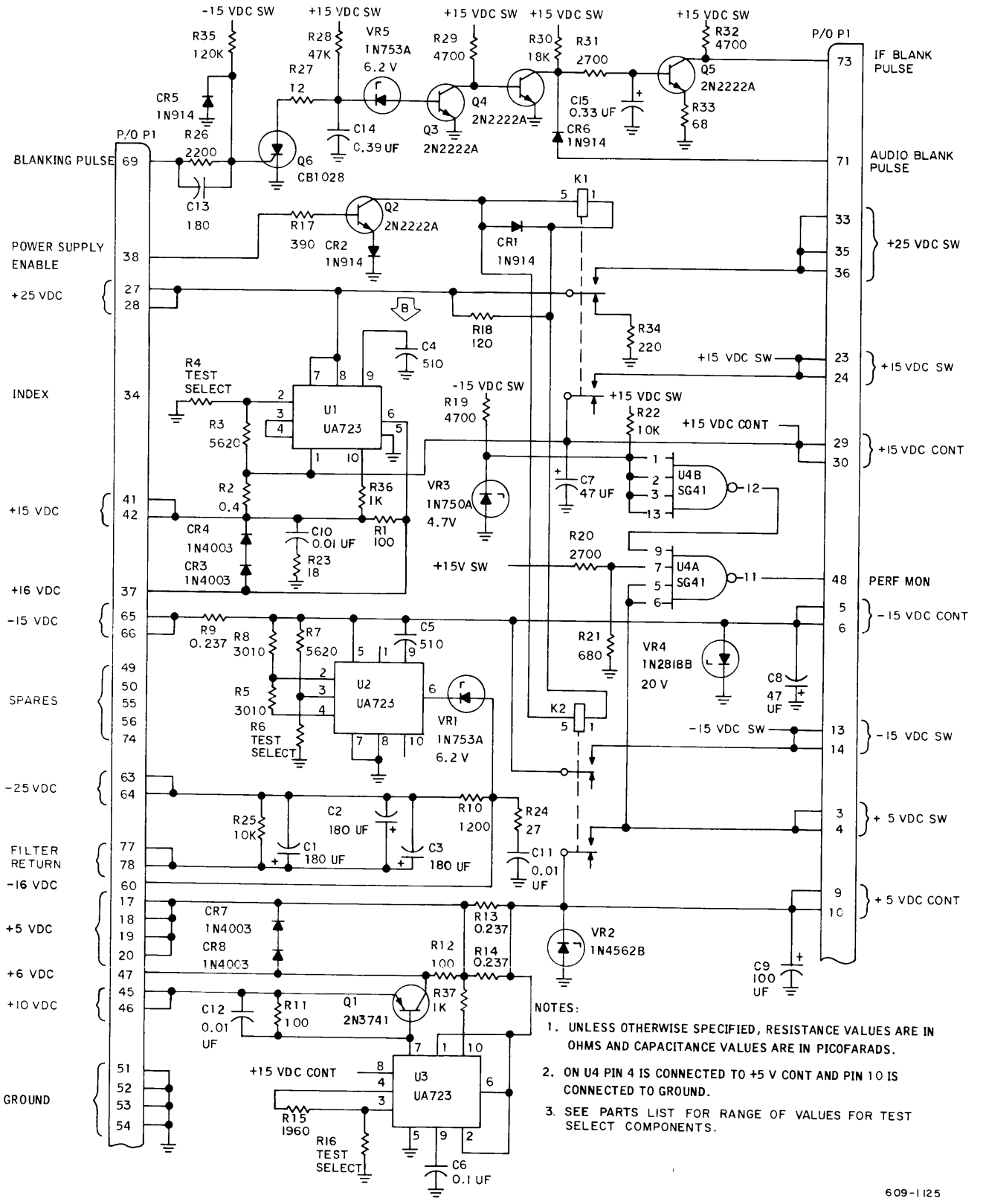


Coaxial Cable Routing and Connector Identification
Figure 3

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	Removed unnecessary pins from P1.		Na
B	C4 changed to 510 pF.		73116

Power Supply Regulator Card A1 (778-2949-001), Schematic Diagram
Figure 4 (Sheet A)

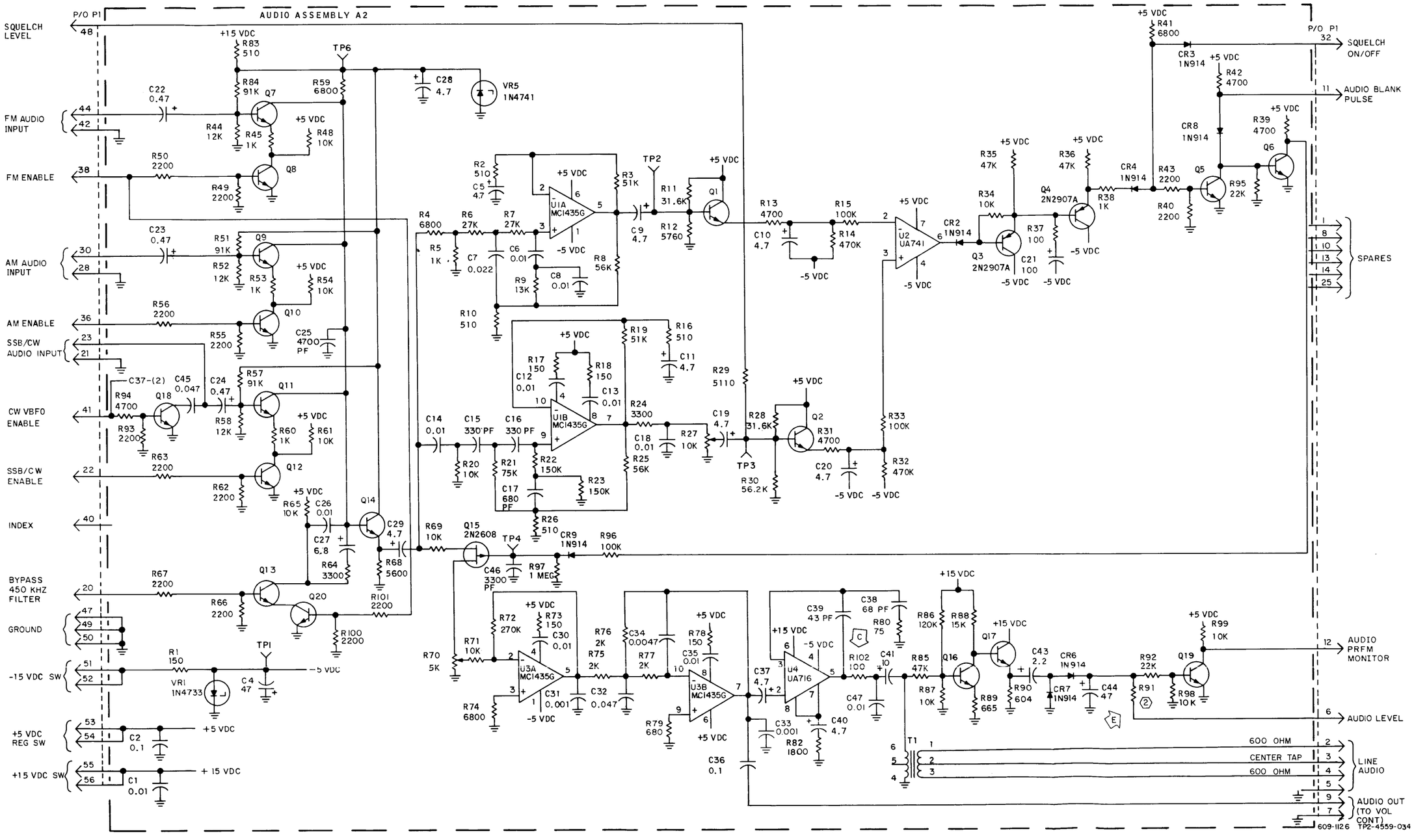


Power Supply Regulator Card A1 (778-2949-001), Schematic Diagram
Figure 4

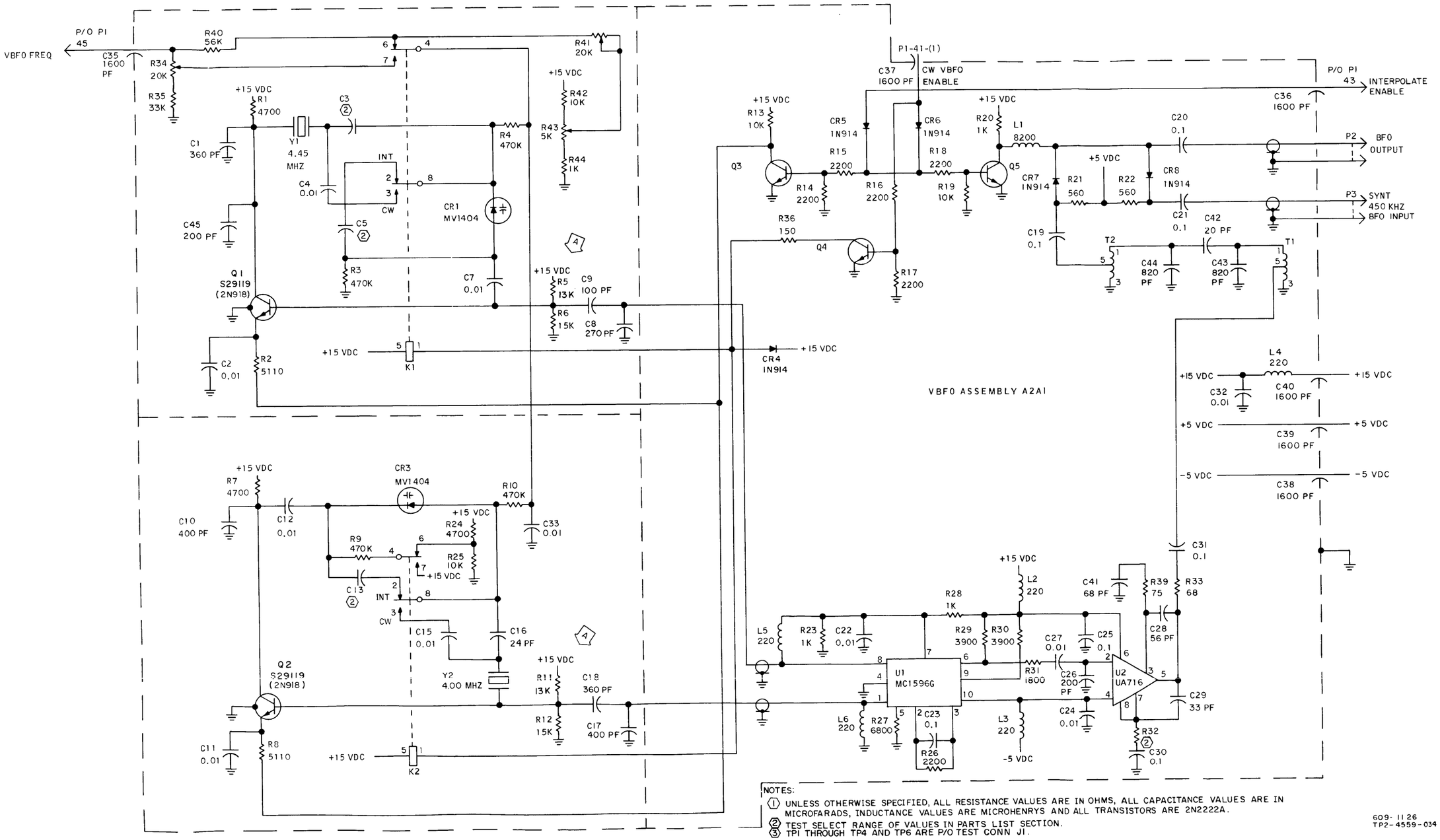
SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R5 and R11 changed to 13 kΩ to stabilize oscillator bias for improved CW pullability.		72297
B	Sheet 3 of schematic diagram added to include coverage of -004 status.		
C	L1 deleted, R102 (100 ohms) added. A2A1R36 deleted. A2A1R14 and A2A1R17 changed from 2200 ohms to 10 kΩ.		72373
D	C46 (180 pF) added to -004 status.		72465
E	R91 changed to test select.		73116

Audio Card A2 (778-2948-002, -004), Schematic Diagram
Figure 5 (Sheet A)



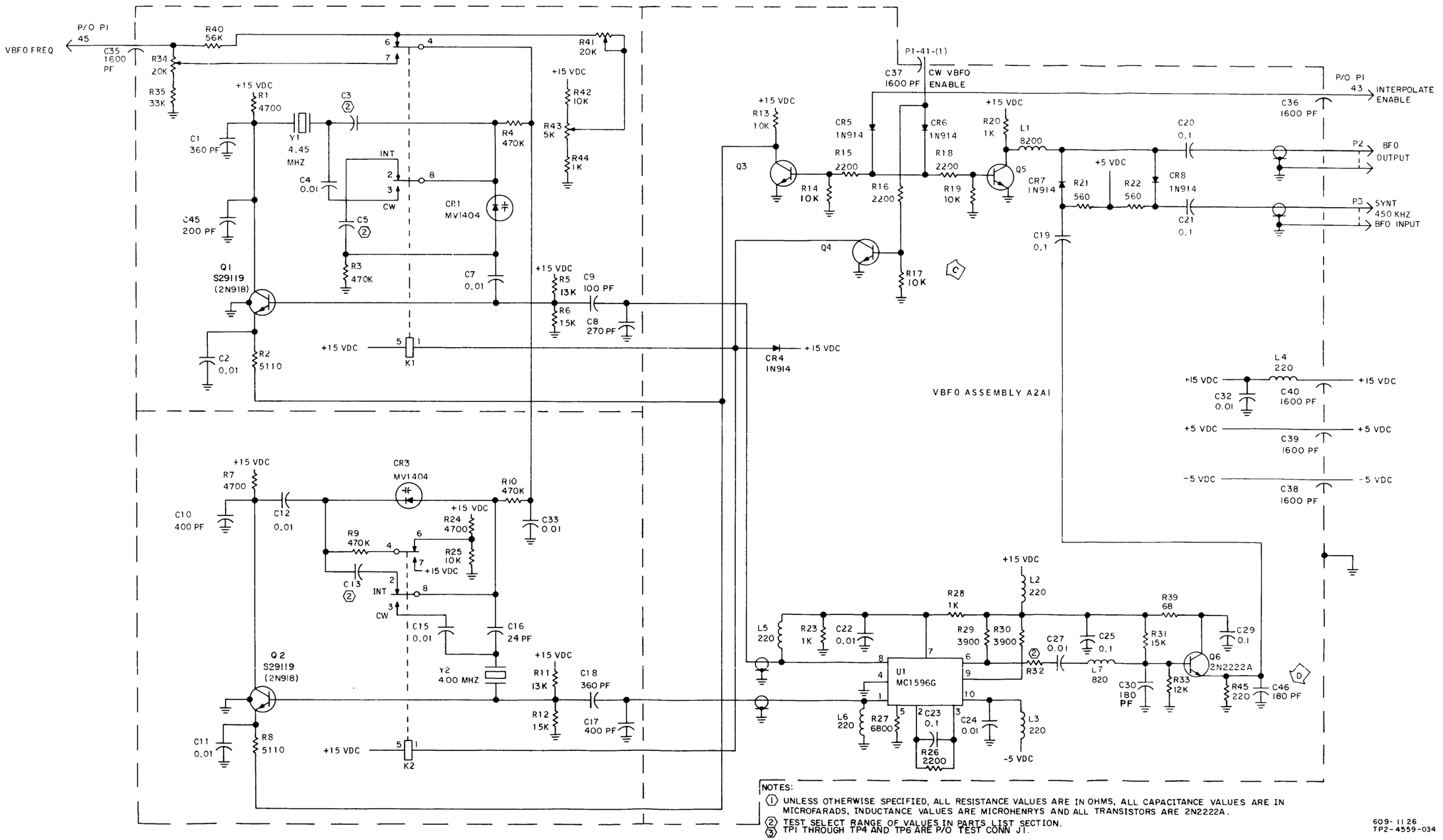
Audio Card A2 (778-2948-002, -004), Schematic Diagram
Figure 5 (Sheet 1 of 3)



NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE MICROHENRYS AND ALL TRANSISTORS ARE 2N2222A.
2. TEST SELECT RANGE OF VALUES IN PARTS LIST SECTION.
3. TP1 THROUGH TP4 AND TP6 ARE P/O TEST CONN J1.

609-1126
TP2-4559-034

Audio Card A2 (778-2948-002 Only), Schematic Diagram
Figure 5 (Sheet 2 of 3)



NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE MICROHENRYS AND ALL TRANSISTORS ARE 2N2222A.
2. TEST SELECT RANGE OF VALUES IN PARTS LIST SECTION.
3. TP1 THROUGH TP4 AND TP6 ARE P/O TEST CONN J1.

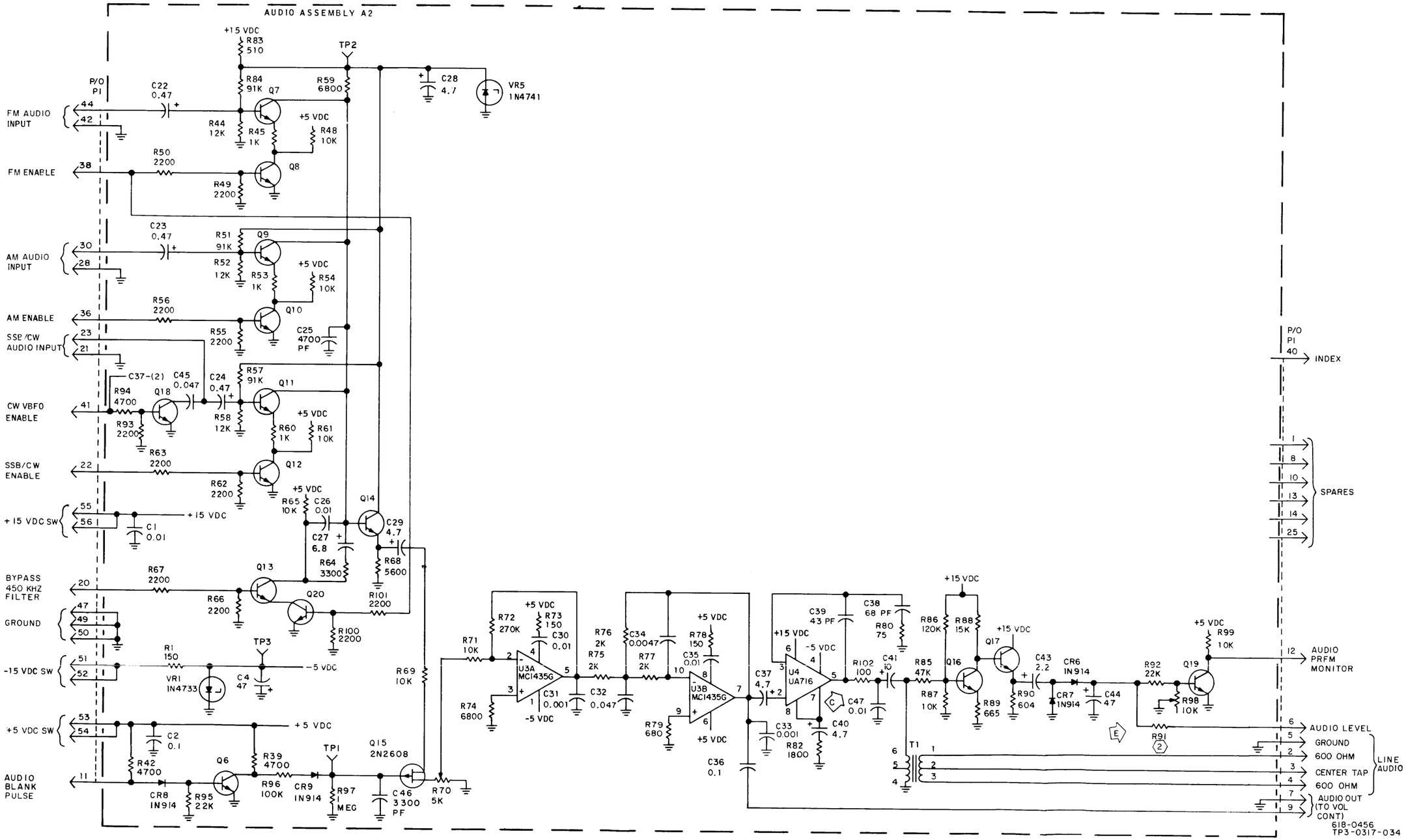
609-1126
TP2-4559-034

Audio Card A2 (778-2948-004 Only), Schematic Diagram
Figure 5 (Sheet 3 of 3)

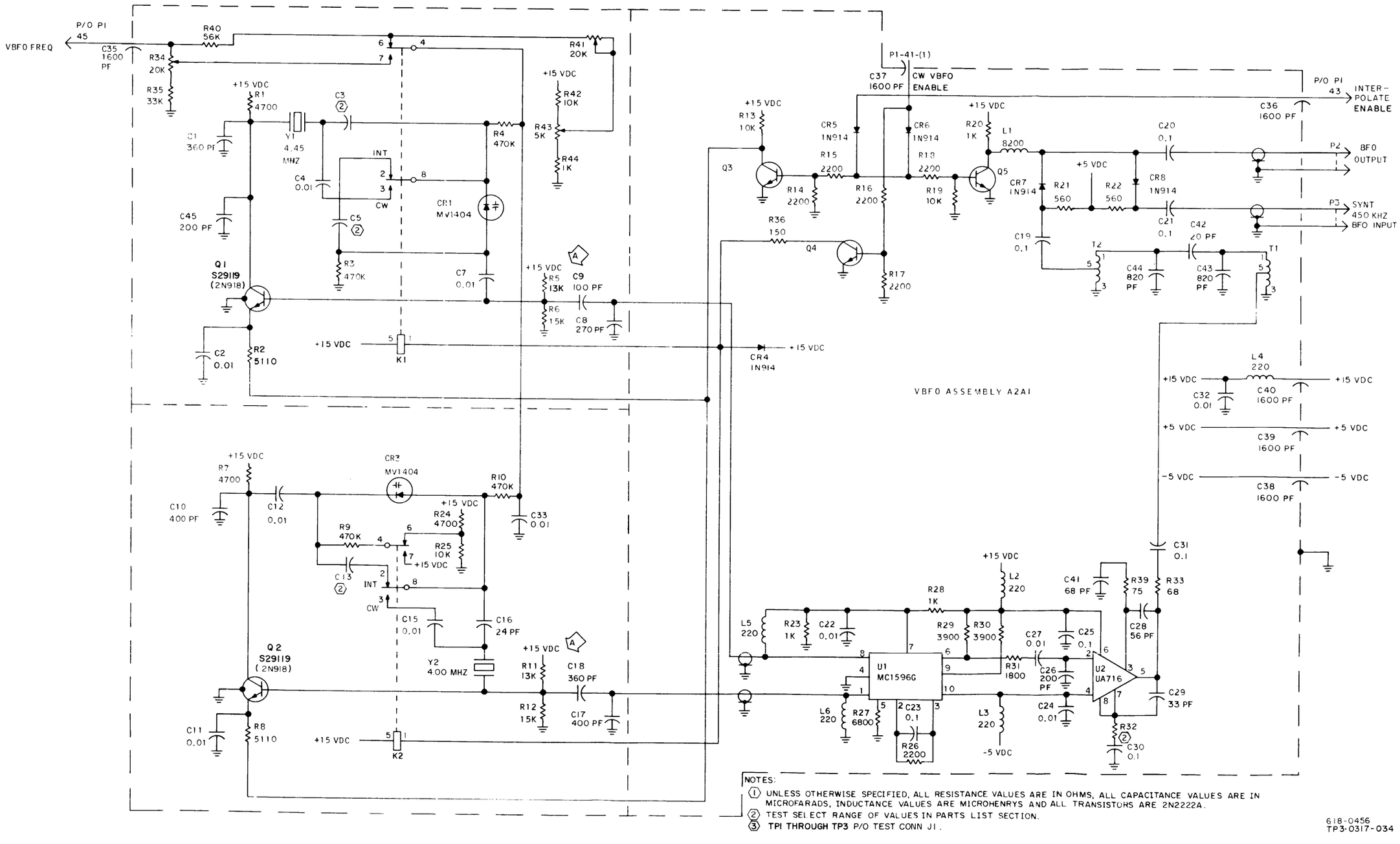
SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R5 and R11 changed to 13 kΩ to stabilize oscillator bias for improved CW pullability.		72297
B	Sheet 3 of schematic diagram added to include coverage of current production model effectivity.		-003, 72373 -005, 72396
C	L1 deleted, R102 (100 ohms) added. A2A1R36 deleted, A2A1R14 and A2A1R17 changed from 2200 ohms to 10 kΩ.		72396
D	C46 (180 pF) added.		72465
E	R91 changed to test select.		73116

Audio Card A2 (778-2948-003, -005), Schematic Diagram
Figure 6 (Sheet A)



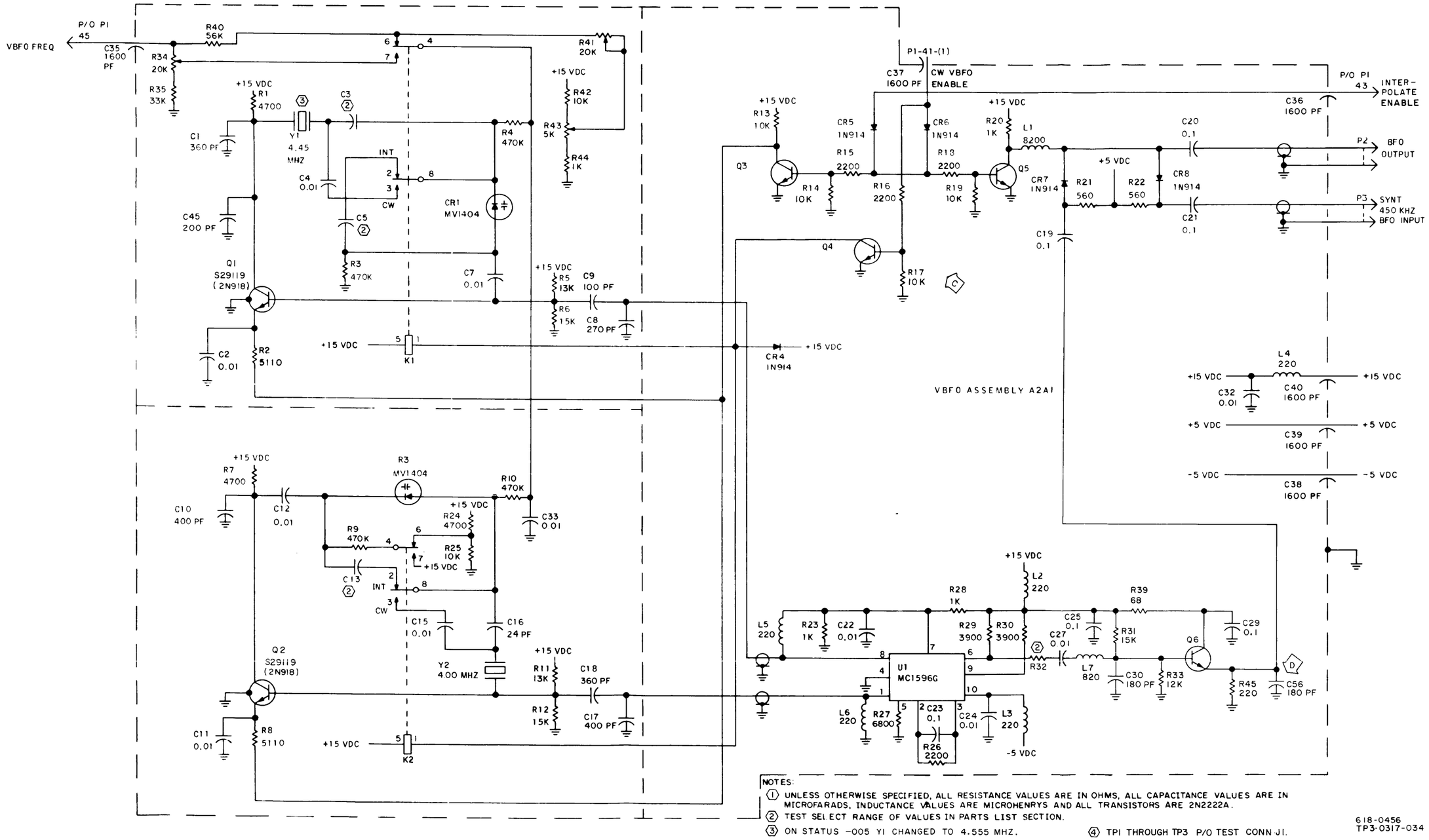
Audio Card A2 (778-2948-003, -005), Schematic Diagram
Figure 6 (Sheet 1 of 3)



NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE MICROHENRYS AND ALL TRANSISTORS ARE 2N2222A.
2. TEST SELECT RANGE OF VALUES IN PARTS LIST SECTION.
3. TP1 THROUGH TP3 P/O TEST CONN J1.

618-0456
TP3-0317-034

Audio Card A2 (778-2948-003, -005, Effectivity up to CI-72353), Schematic Diagram
Figure 6 (Sheet 2 of 3)



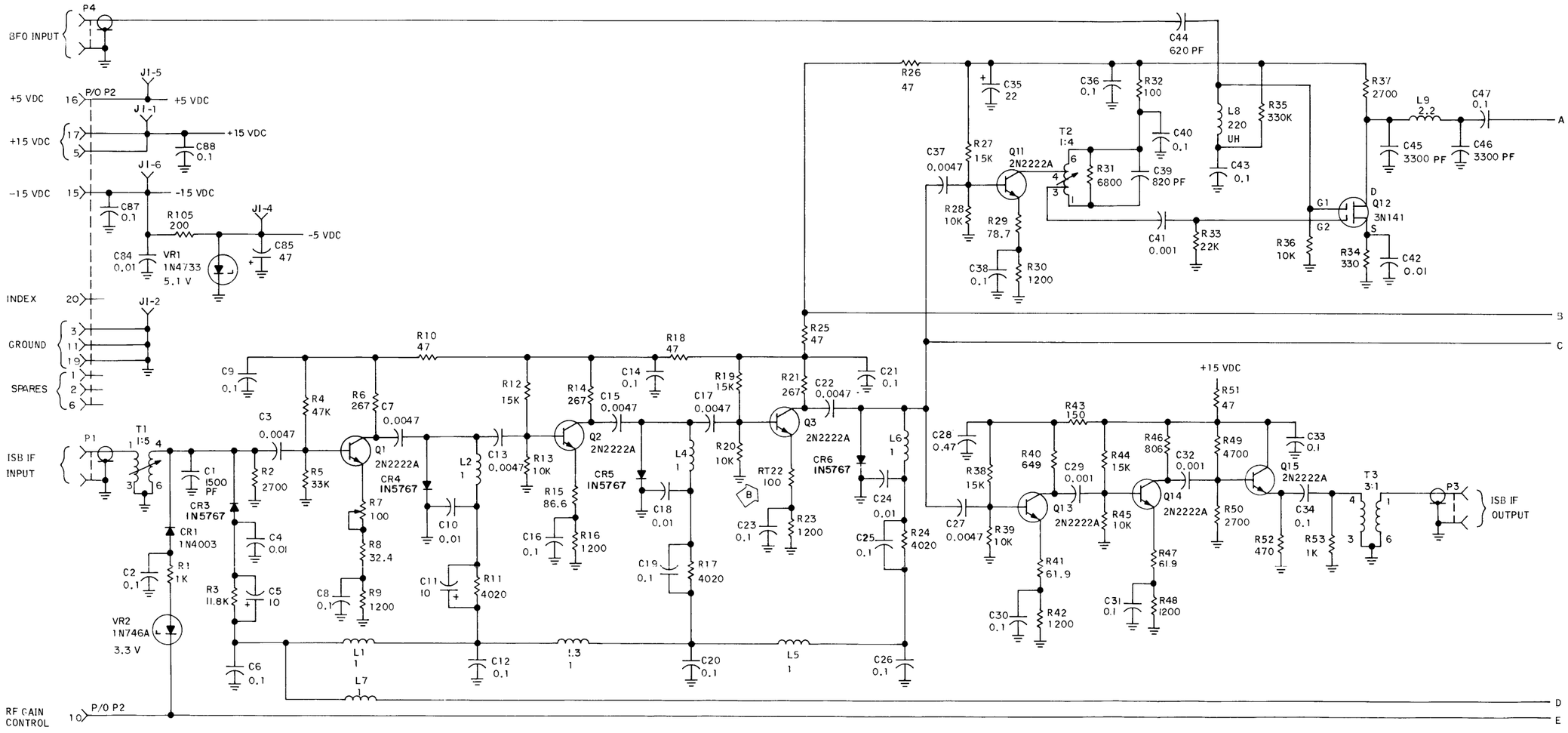
Audio Card A2 (778-2948-003, Effectivity CI-72373, -005, Effectivity CI-72396), Schematic Diagram
Figure 6 (Sheet 3 of 3)

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R61 changed to 45.3 ohms to improve gain. R66 changed to 2700 ohms.		72263
B	R22 changed to RT22, 100-ohm thermistor, to stabilize gain.		72376

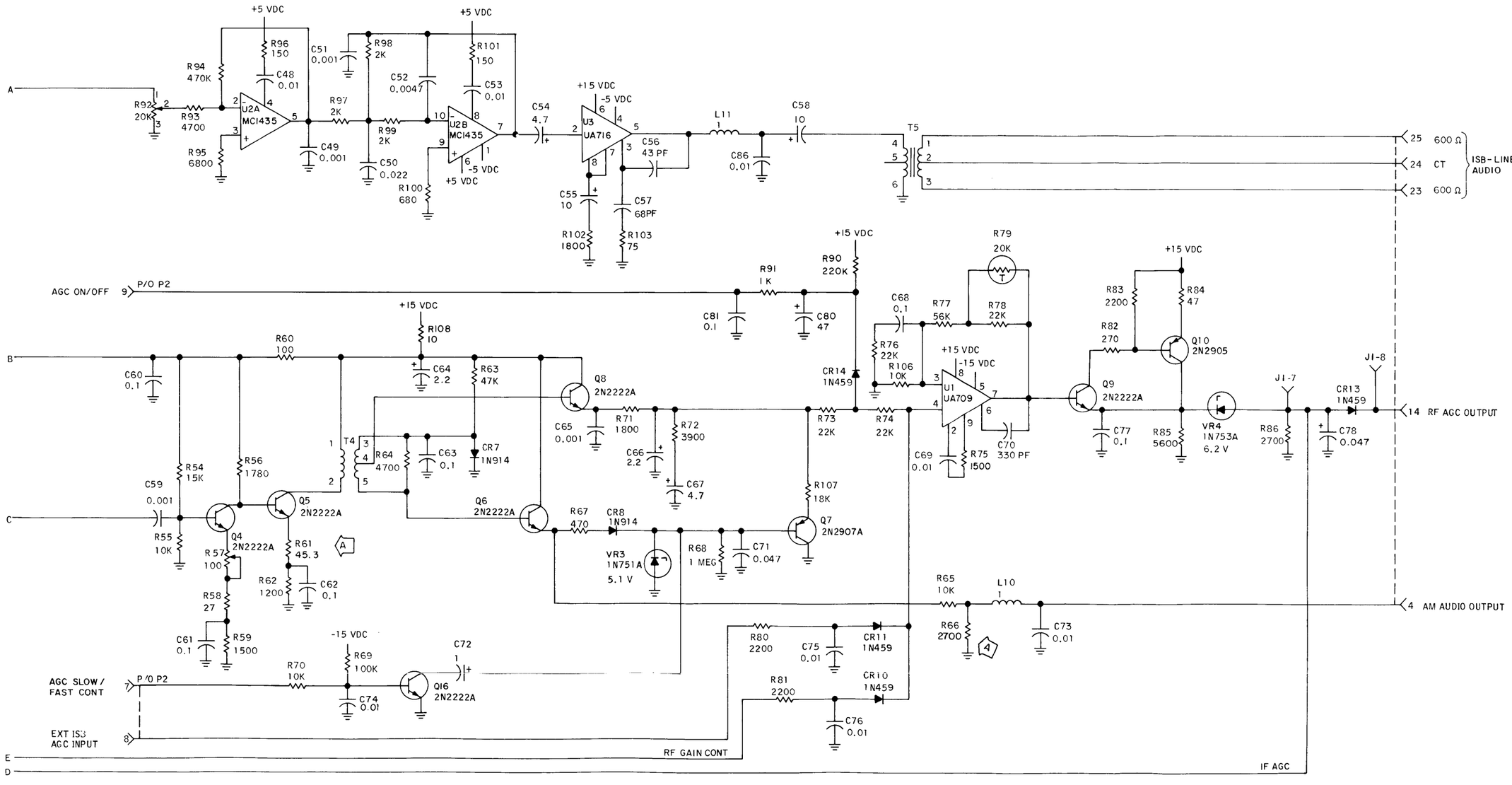
ISB Amplifier Card A3 (778-2952-001) (Optional), Schematic Diagram
Figure 7 (Sheet A)

NOTE:
UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS , AND INDUCTANCE VALUES ARE IN MILLIHENRYS.



609-1127

ISB Amplifier Card A3 (778-2952-001) (Optional), Schematic Diagram
Figure 7 (Sheet 1 of 2)



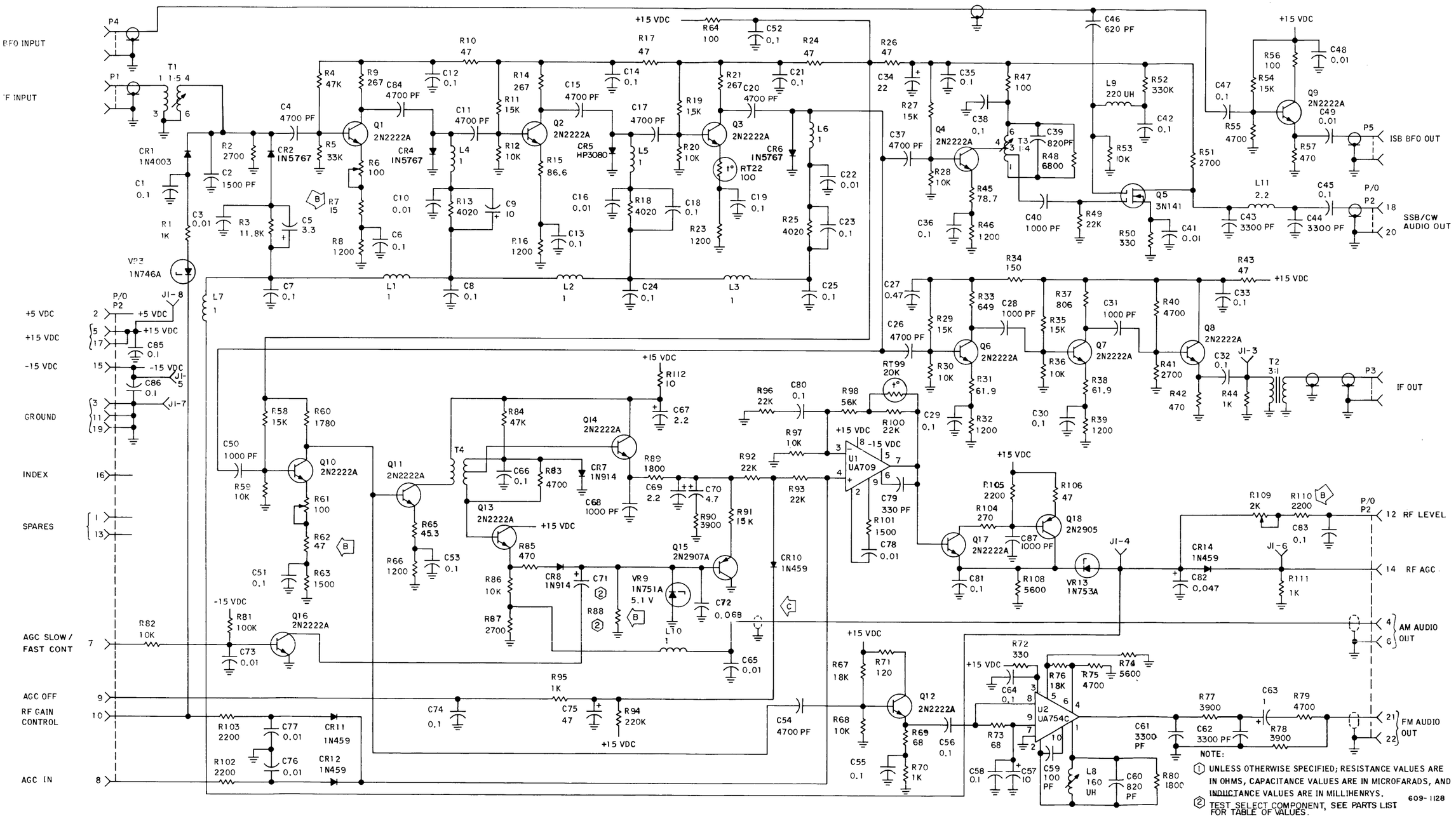
609-1127

ISB Amplifier Card A3 (778-2952-001) (Optional), Schematic Diagram
Figure 7 (Sheet 2 of 2)

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R22 changed to RT22, 100-ohm thermistor, to stabilize gain.		72373
B	R7 changed to 15 ohms, R110 changed to 2200 ohms, and R62 changed to 47 ohms. C71 and R88 changed to test select components to improve gain.		72483
C	C72 changed to 0.068 μF.		73156

IF Amplifier Card A4 (778-2951-001), Schematic Diagram
Figure 8 (Sheet A)

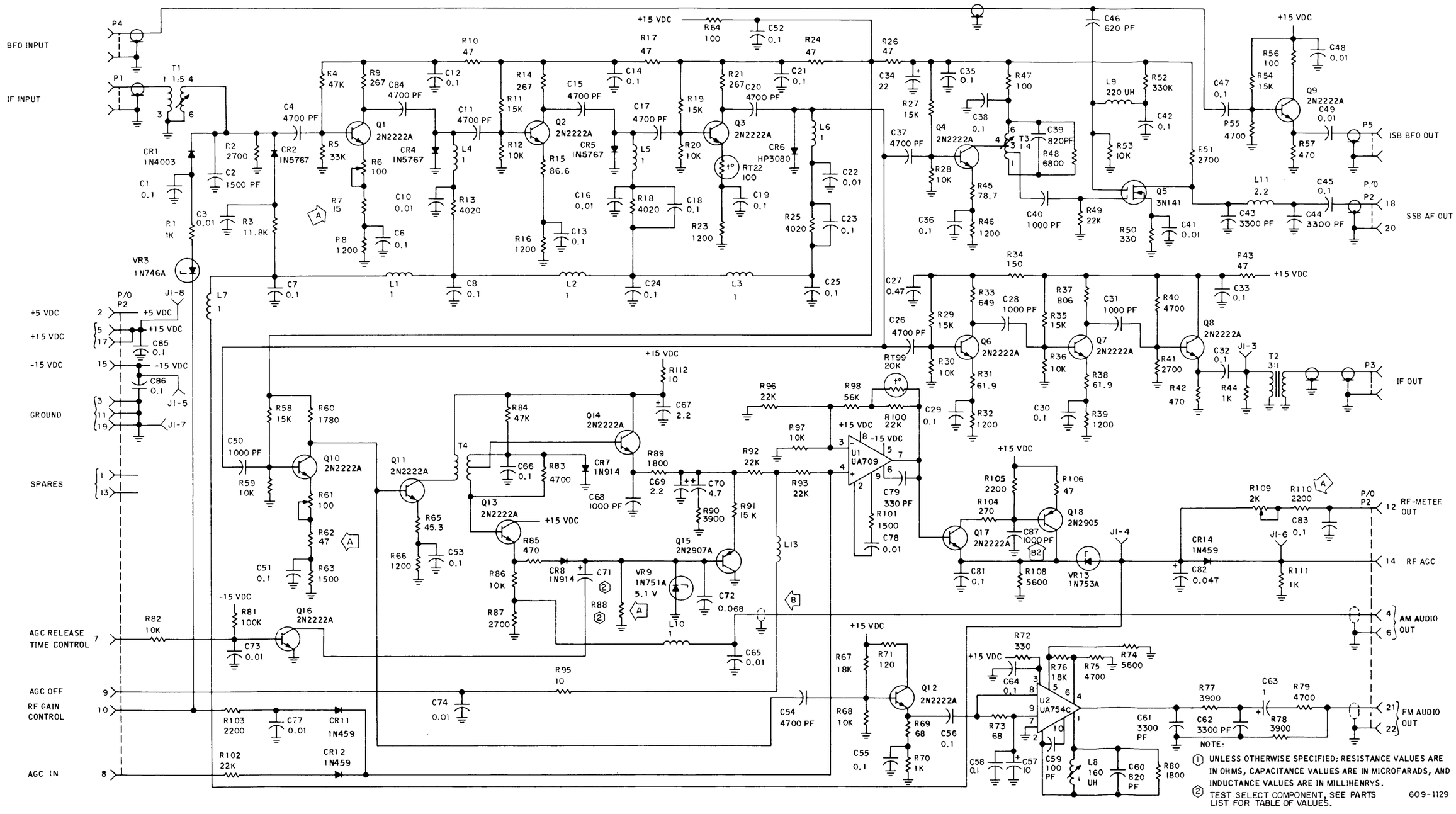


IF Amplifier Card A4 (778-2951-001), Schematic Diagram
Figure 8

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R7 changed to 15 ohms, R110 changed to 2200 ohms, and R62 changed to 47 ohms. C71 and R88 changed to test select components to improve gain.		72473
B	C72 changed to 0.068 μF.		73156

IF Amplifier Card A4 (778-2951-003), Schematic Diagram
Figure 9 (Sheet A)

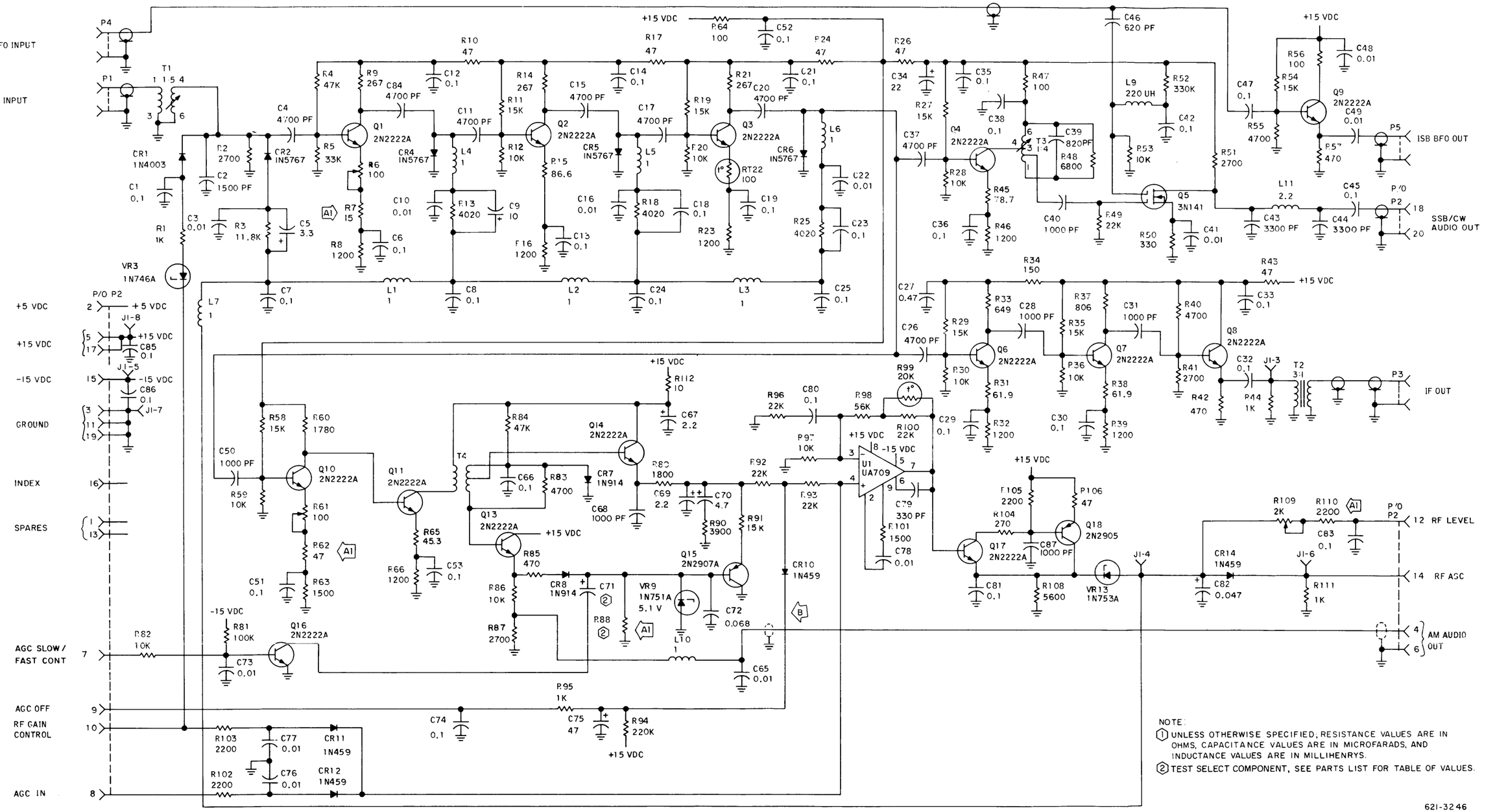


IF Amplifier Card A4 (778-2951-003), Schematic Diagram
Figure 9

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	R7 changed to 15 ohms, R110 changed to 2200 ohms, and R62 changed to 47 ohms. C71 and R88 changed to test select components to improve gain.		72463
B	C72 changed to 0.068 μF.		73156

IF Amplifier Card A4 (778-2951-004), Schematic Diagram
Figure 10 (Sheet A)

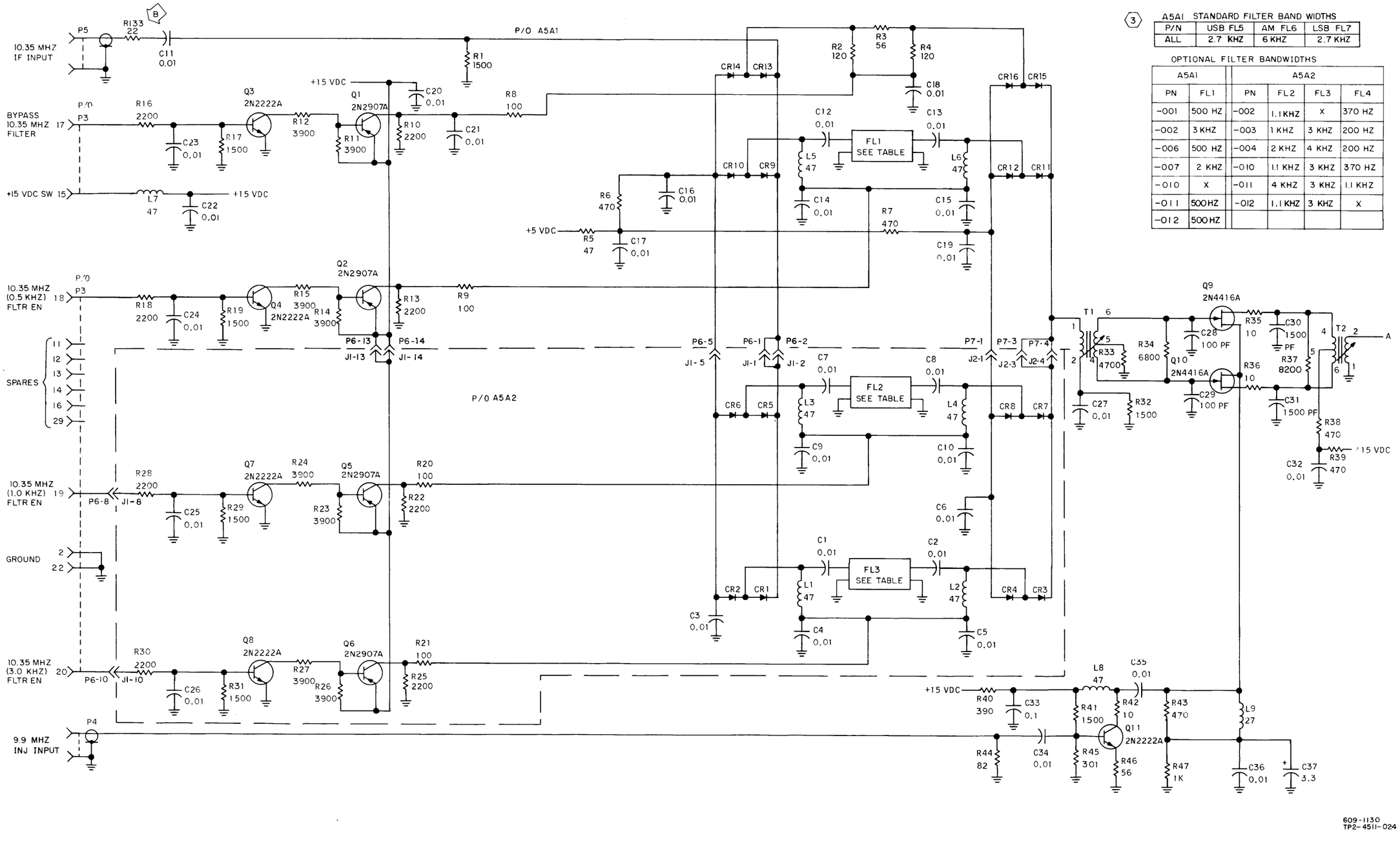


IF Amplifier Card A4 (778-2951-004), Schematic Diagram
Figure 10

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	Additional optional filter bandwidths included. See table and note on schematic diagram.		Refer to paragraph 2, configuration effectivity.
B	R33 (22 ohms) added.		72426
C	R63 changed to 3.3 kΩ.		73136

IF Filter Card A5A1 and IF Filter Card A5A2, Schematic Diagram
Figure 11 (Sheet A)



(3) A5A1 STANDARD FILTER BAND WIDTHS

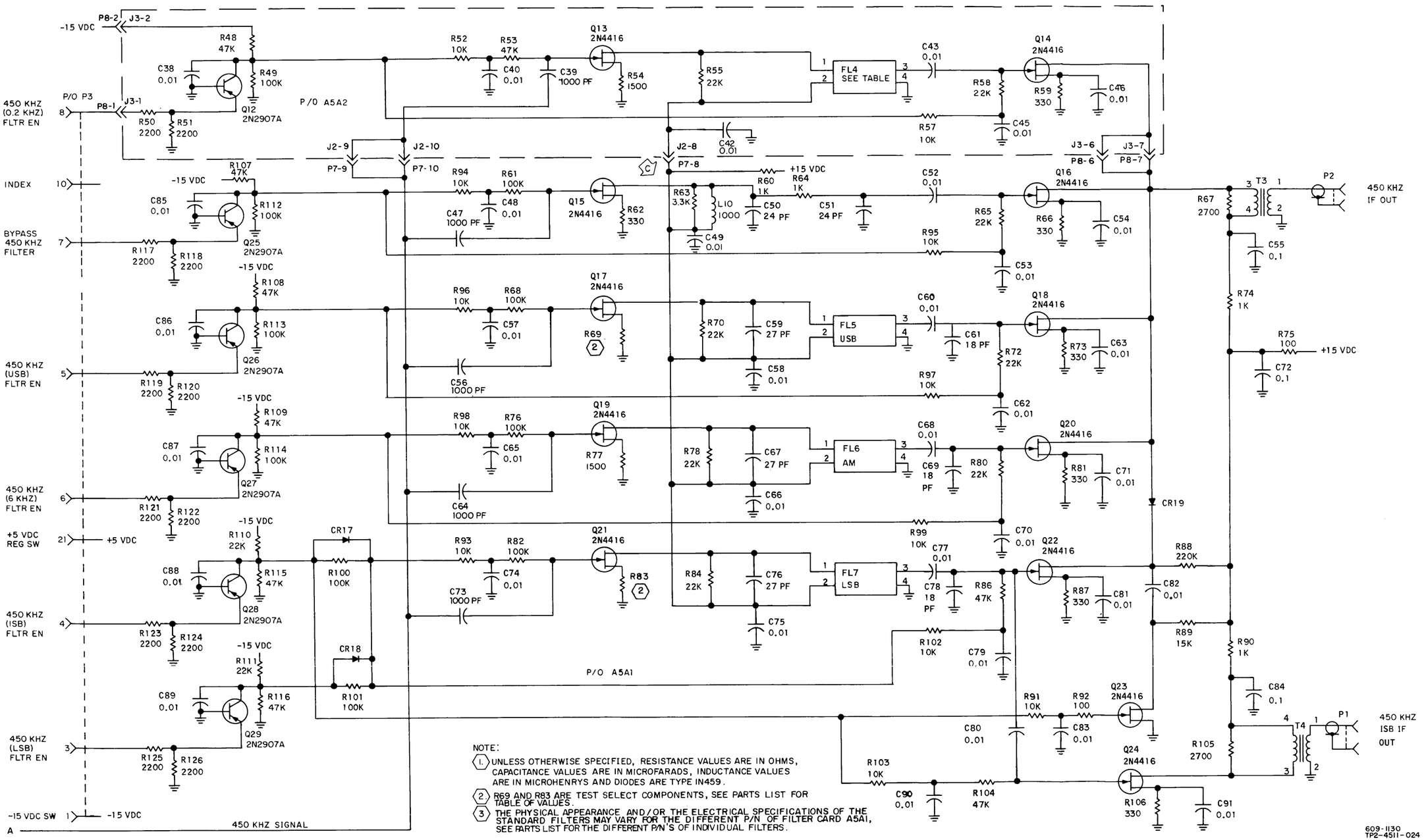
P/N	USB FL5	AM FL6	LSB FL7
ALL	2.7 KHZ	6 KHZ	2.7 KHZ

OPTIONAL FILTER BANDWIDTHS

A5A1		A5A2			
PN	FL1	PN	FL2	FL3	FL4
-001	500 HZ	-002	1.1KHZ	X	370 HZ
-002	3 KHZ	-003	1 KHZ	3 KHZ	200 HZ
-006	500 HZ	-004	2 KHZ	4 KHZ	200 HZ
-007	2 KHZ	-010	1.1 KHZ	3 KHZ	370 HZ
-010	X	-011	4 KHZ	3 KHZ	1.1 KHZ
-011	500HZ	-012	1.1 KHZ	3 KHZ	X
-012	500HZ				

609-1130
TP2-4511-024

IF Filter Card A5A1 and IF Filter Card A5A2,
Schematic Diagram
Figure 11 (Sheet 1 of 2)

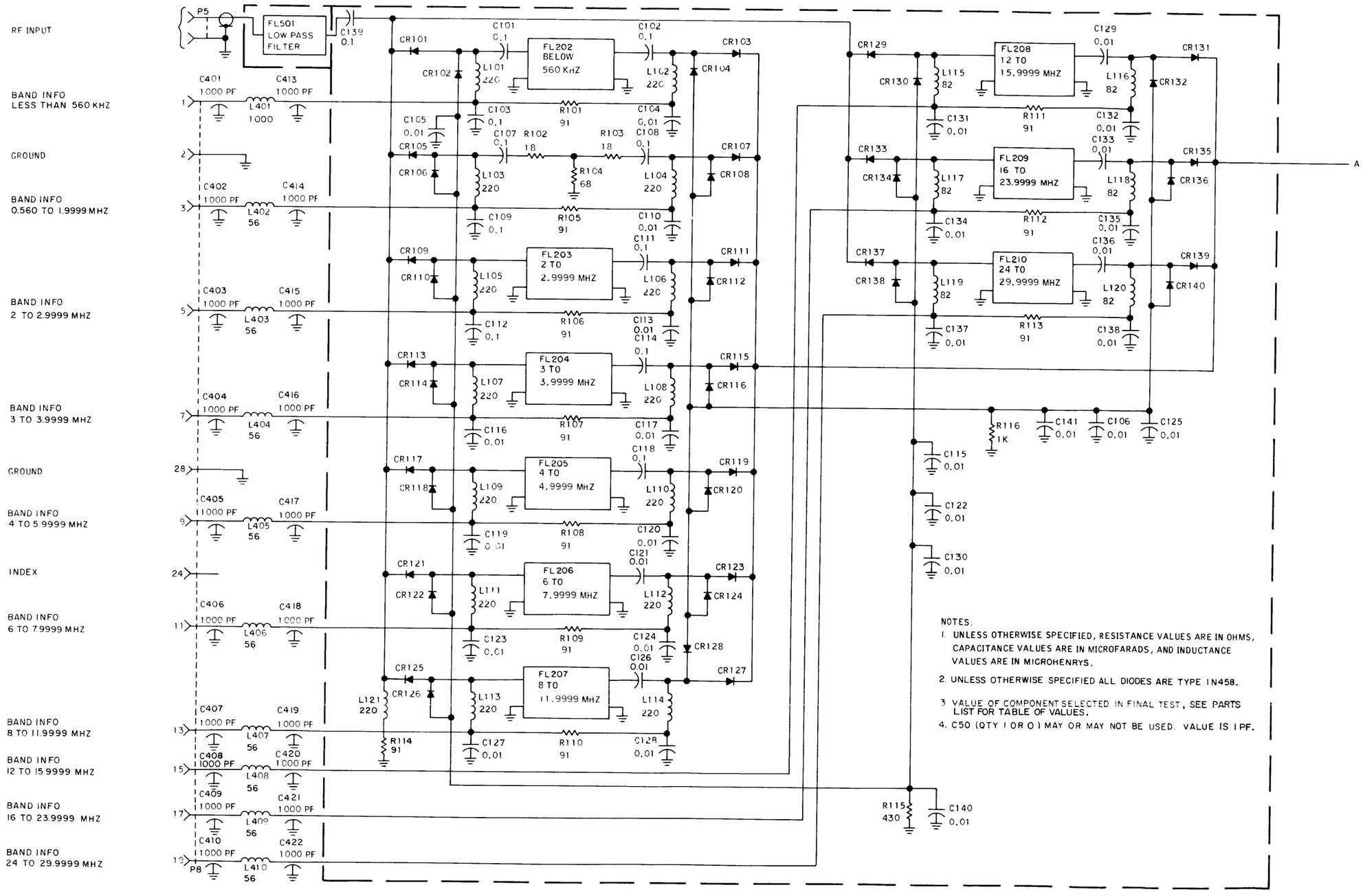


IF Filter Card A5A1 and IF Filter Card A5A2.
Schematic Diagram
Figure 11 (Sheet 2 of 2)

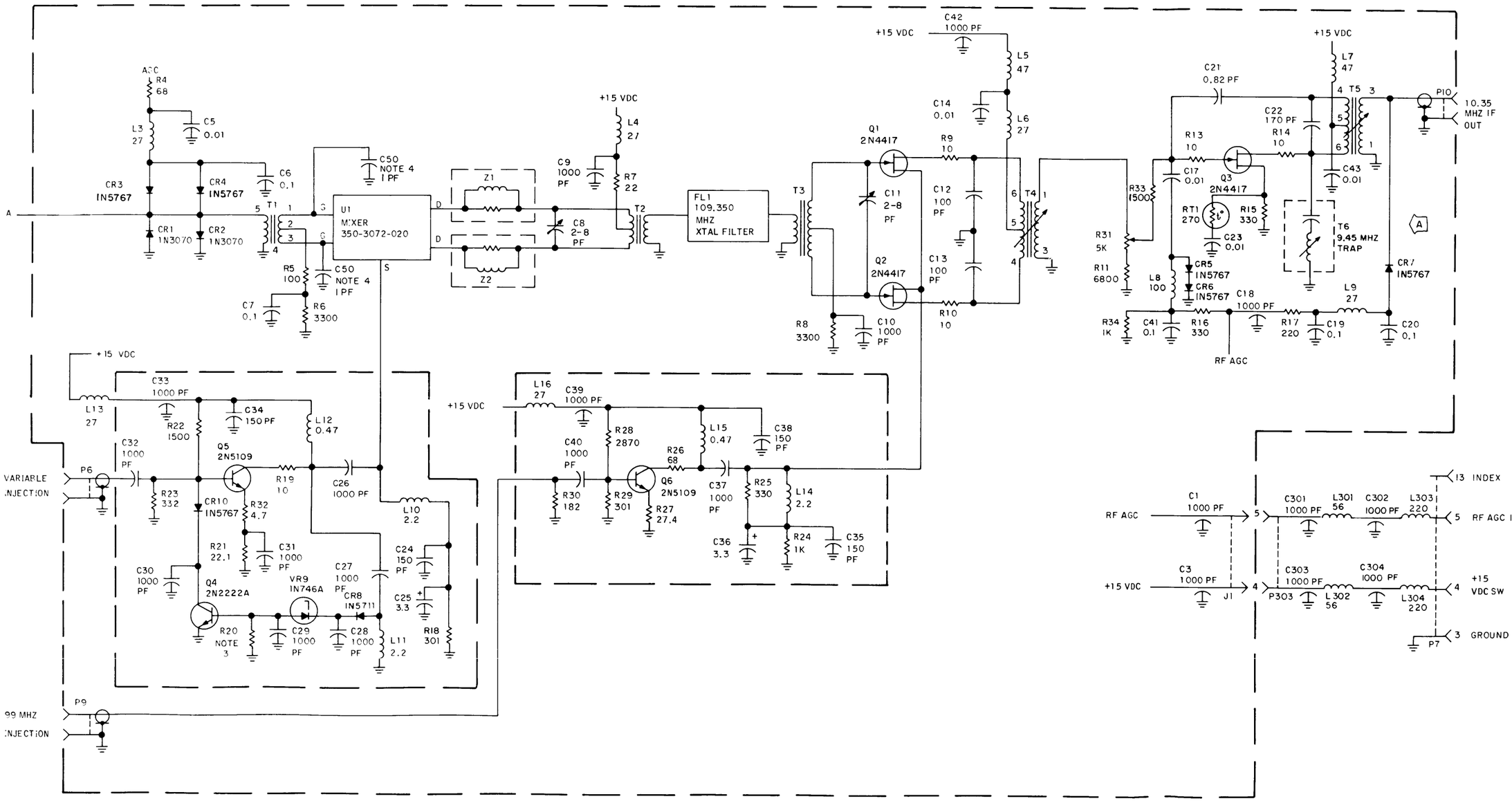
SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	A1 through Q3 changed to type 2N4417.		72263

RF Module A6 (790-1048-008), Schematic Diagram
Figure 12 (Sheet A)



RF Module A6 (790-1048-008), Schematic Diagram
Figure 12 (Sheet 1 of 2)

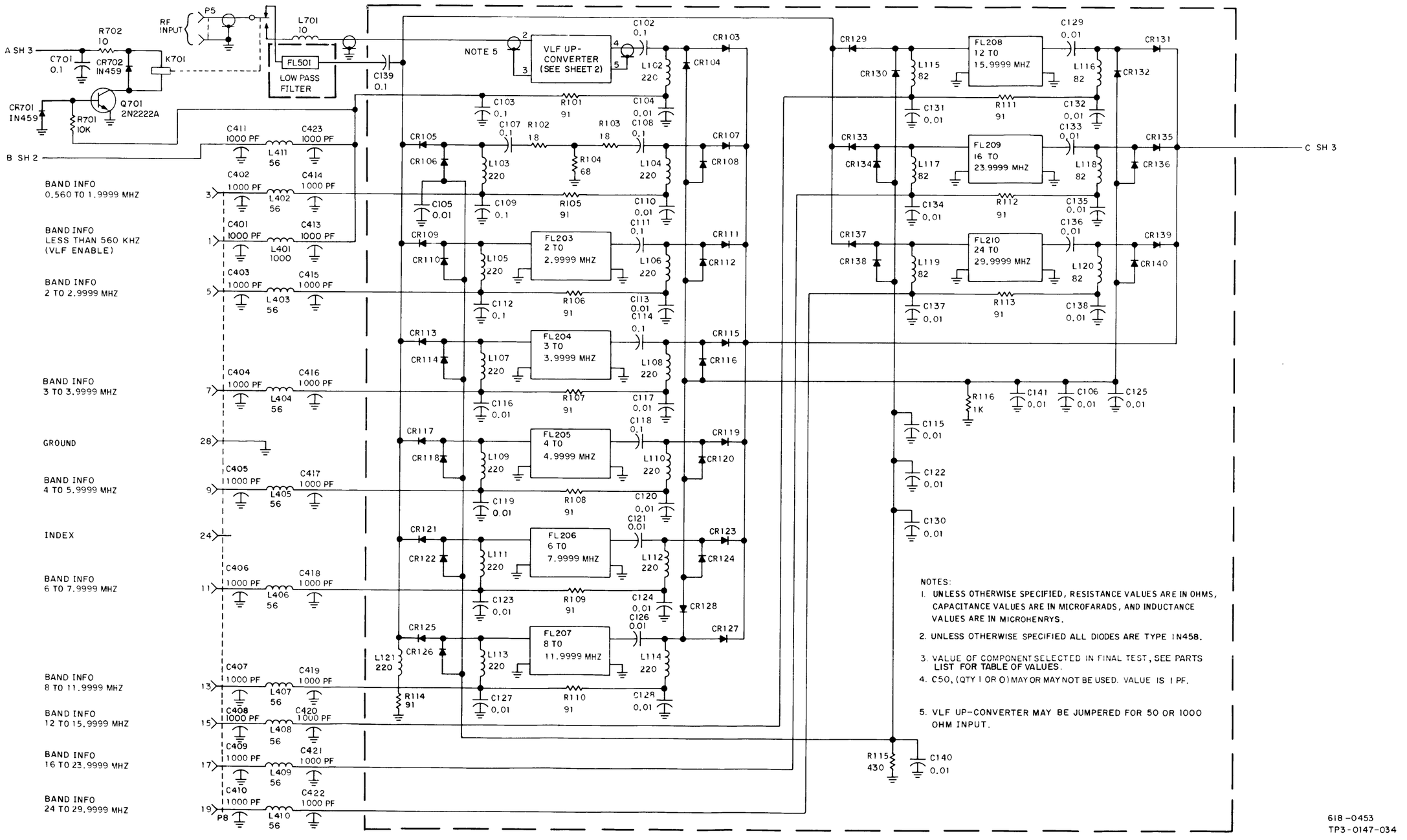


RF Module A6 (790-1048-008), Schematic Diagram
Figure 12 (Sheet 2 of 2)

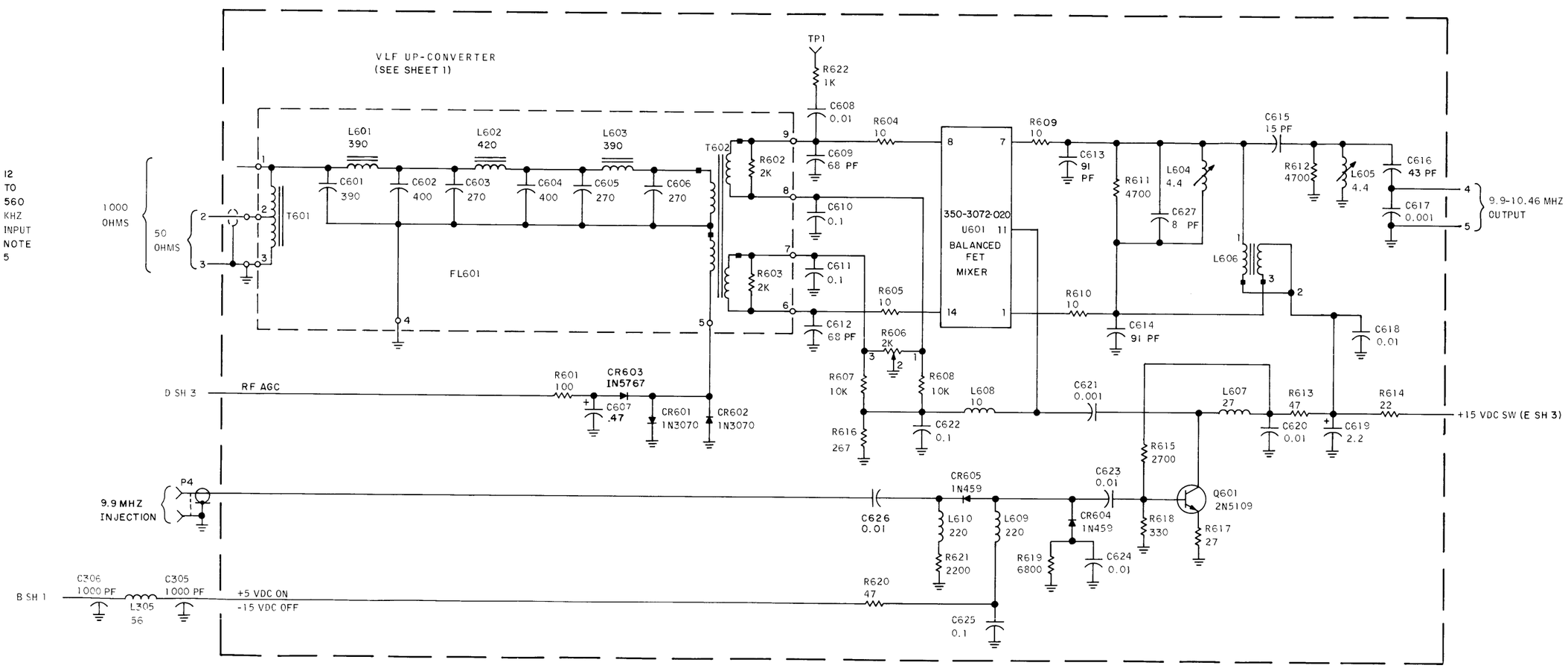
SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
	Updated preliminary schematic, added wiring change to K701. C609 and C610 changed to 91 pF, C616 changed to 43 pF. CR603 changed to HP 3080. L601 and L603 changed to 390 μH. L602 changed to 420 μH.		All
A	Q1 through Q3 changed to types 2N4417.		72314

RF Module A6 (790-1048-010), Schematic Diagram
Figure 13 (Sheet A)

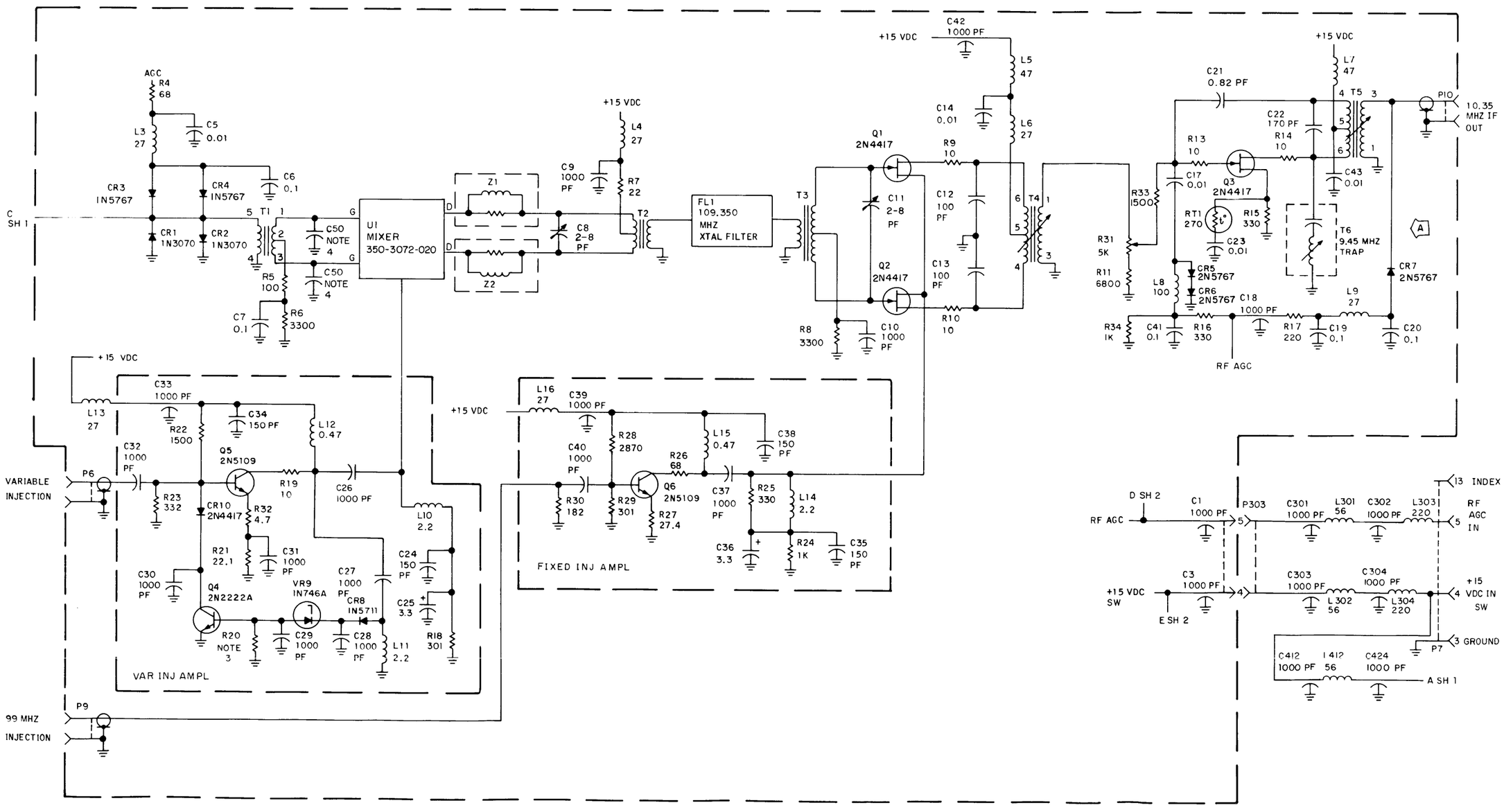


RF Module A6 (790-1048-010), Schematic Diagram
Figure 13 (Sheet 1 of 3)



618-0453
TP3-0147-034

RF Module A6 (790-1048-010), Schematic Diagram
Figure 13 (Sheet 2 of 3)

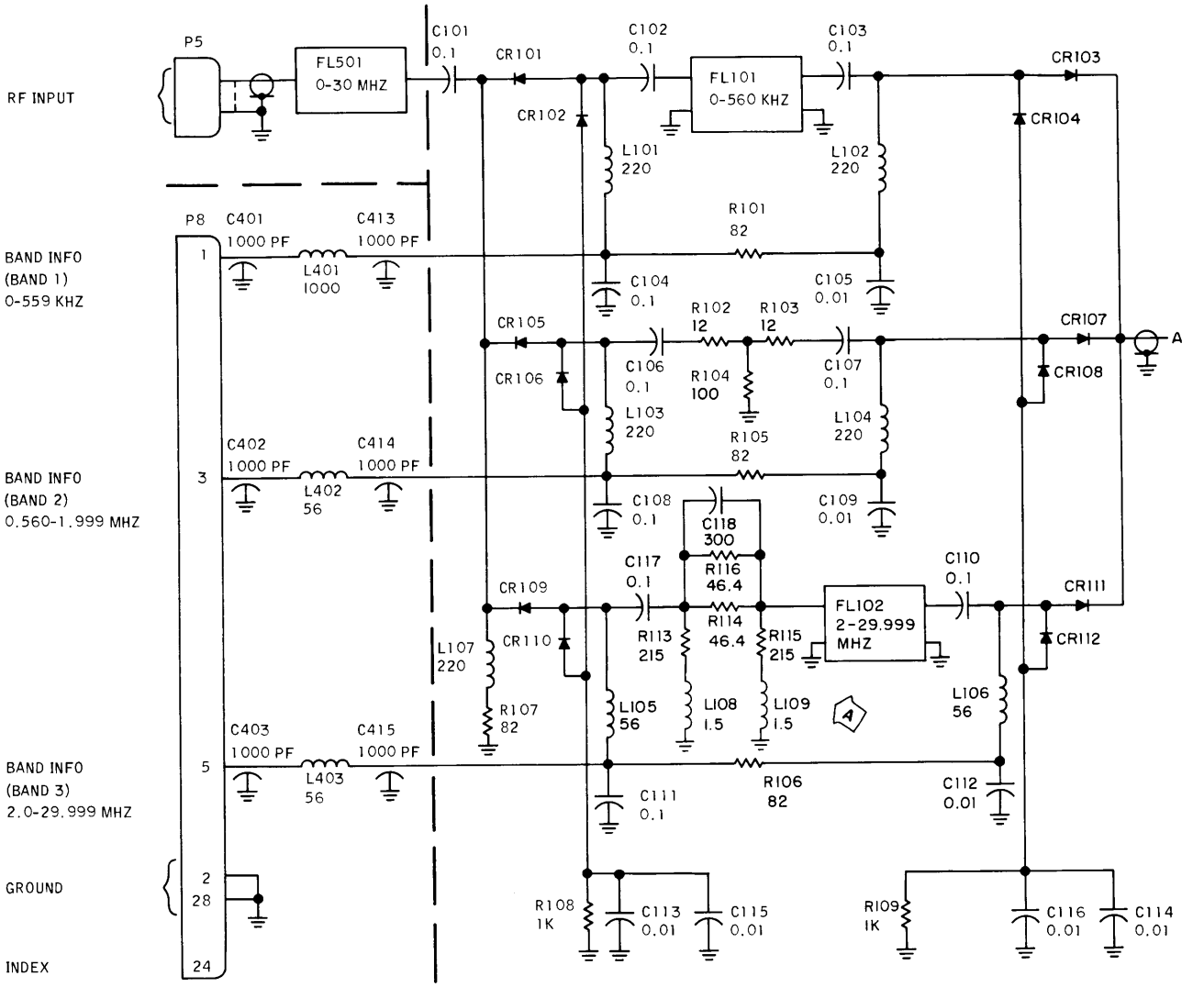


RF Module A6 (790-1048-010), Schematic Diagram
Figure 13 (Sheet 3 of 3)

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	C118 changed to 300 μF, L108 and L109 (1.5 μH). Added for better filtering action.		73056

RF Module A6 (790-1048-020), Schematic Diagram
Figure 14 (Sheet A)

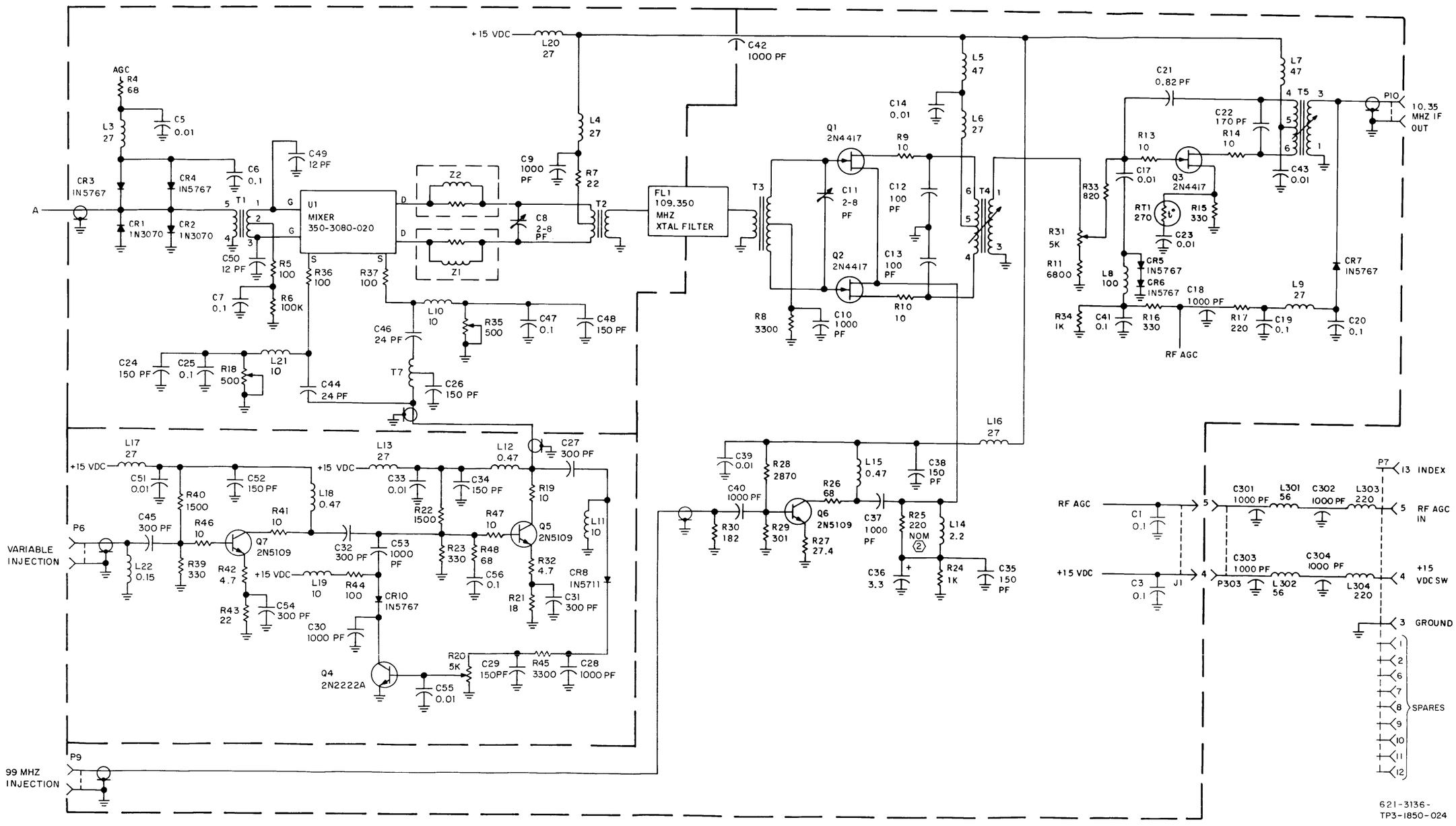


NOTES:

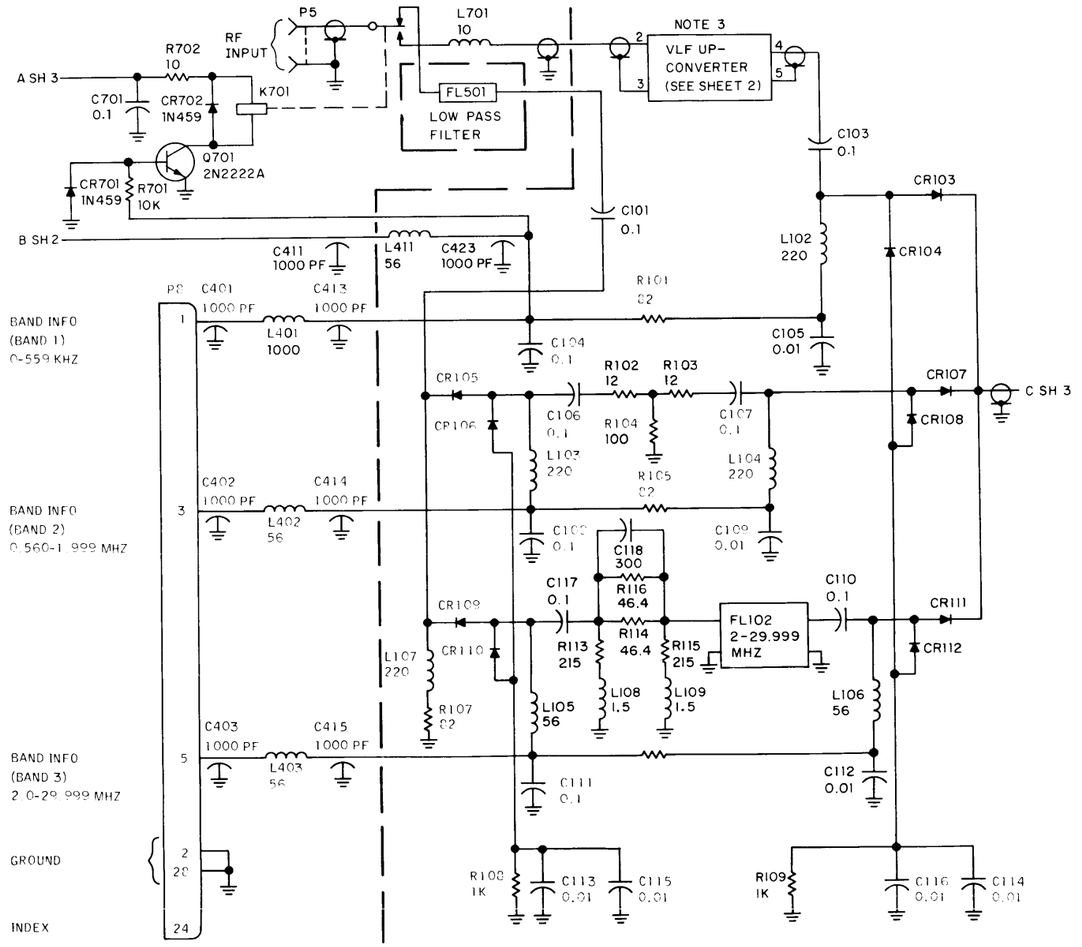
1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS, AND ALL DIODES ARE TYPE 1N458.
2. R25 IS A TEST SELECT COMPONENT, SEE TABLE OF VALUES IN PARTS LIST.

621-3136-001
TP3-1850-024

RF Module A6 (790-1048-020), Schematic Diagram
Figure 14 (Sheet 1 of 2)



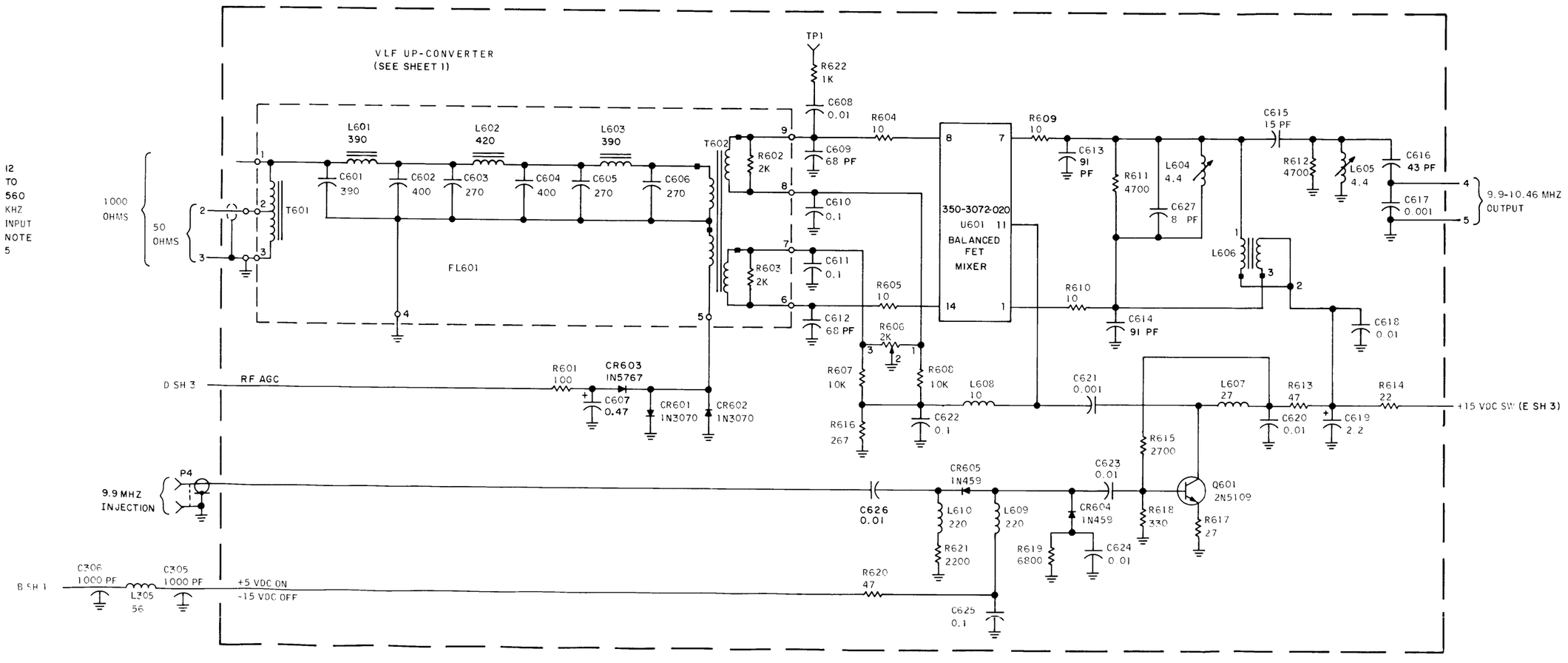
RF Module A6 (790-1048-020), Schematic Diagram
Figure 14 (Sheet 2 of 2)



1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS, AND ALL DIODES ARE TYPE 1N450.
2. R25 IS A TEST SELECT COMPONENT SEE TABLE OF VALUES IN PARTS LIST.
3. VLF UP-CONVERTER MAY BE JUMPERED FOR 50 OR 1000 OHM INPUT.

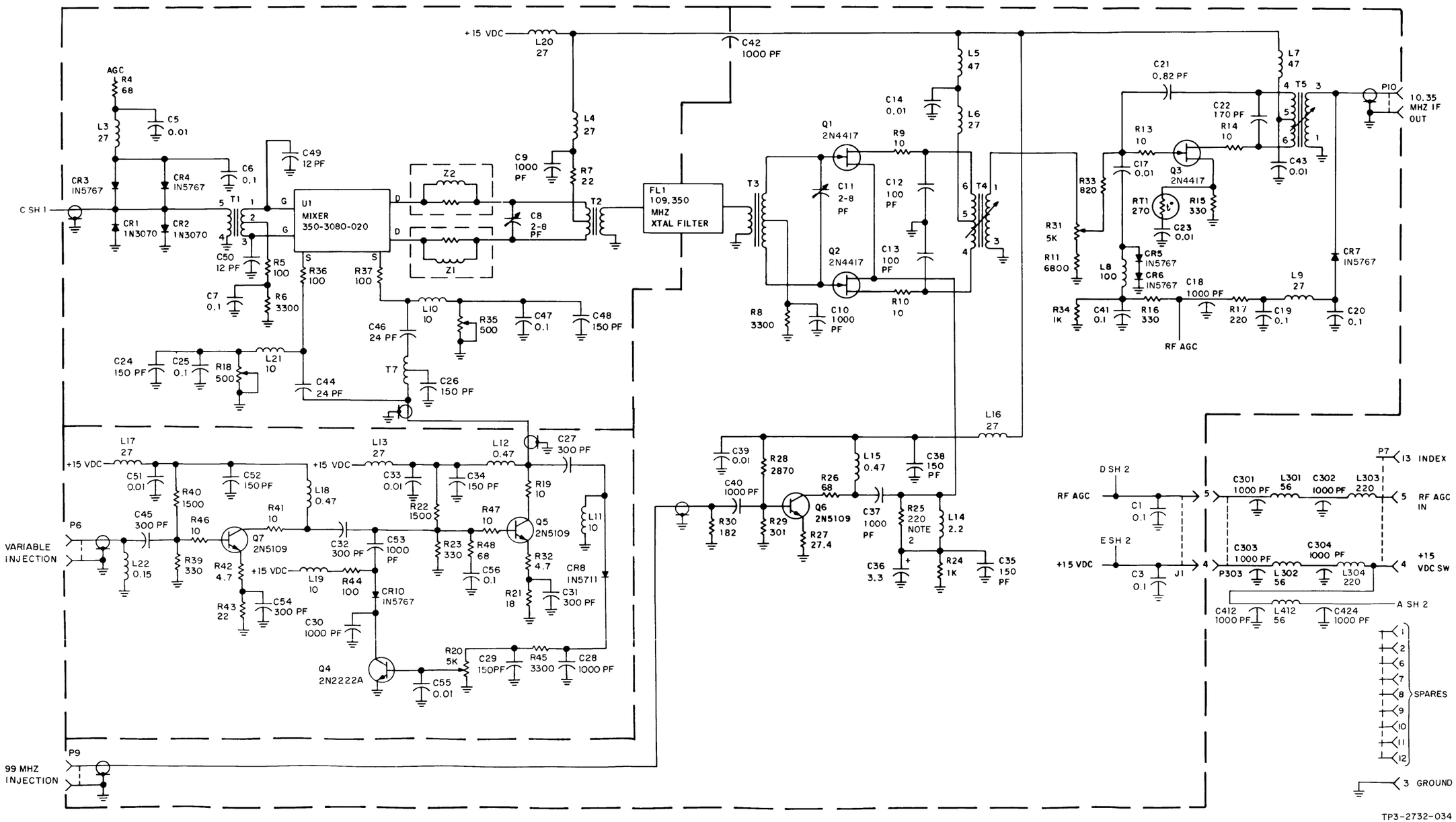
TP3-2732-034

RF Module A6, (790-1048-021), Schematic Diagram
Figure 15 (Sheet 1 of 3)



TP3-2732-034

RF Module A6 (790-1048-021), Schematic Diagram
Figure 15 (Sheet 2 of 3)

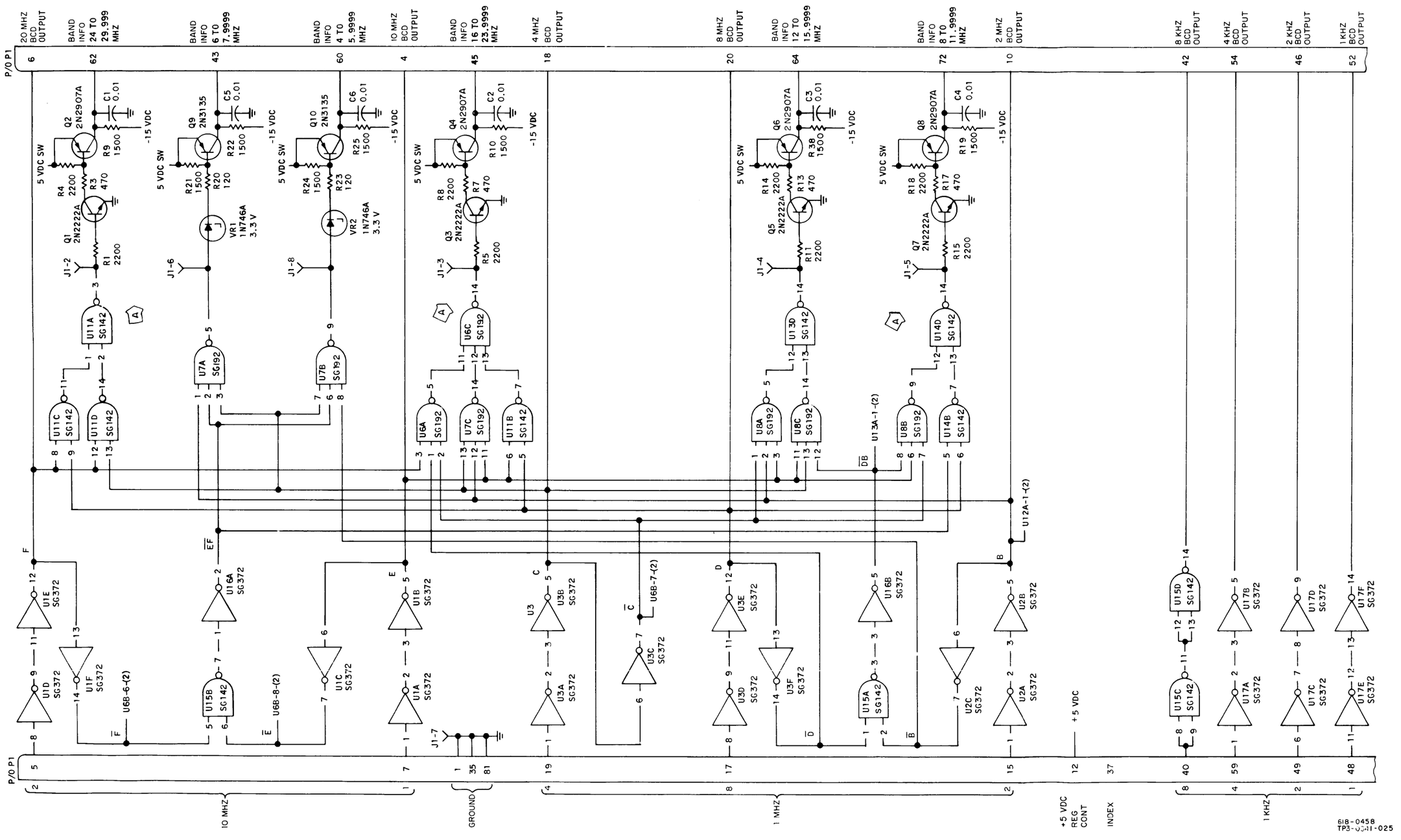


RF Module A6 (790-1048-021), Schematic Diagram
Figure 15 (Sheet 3 of 3)

SCHEMATIC CHANGES

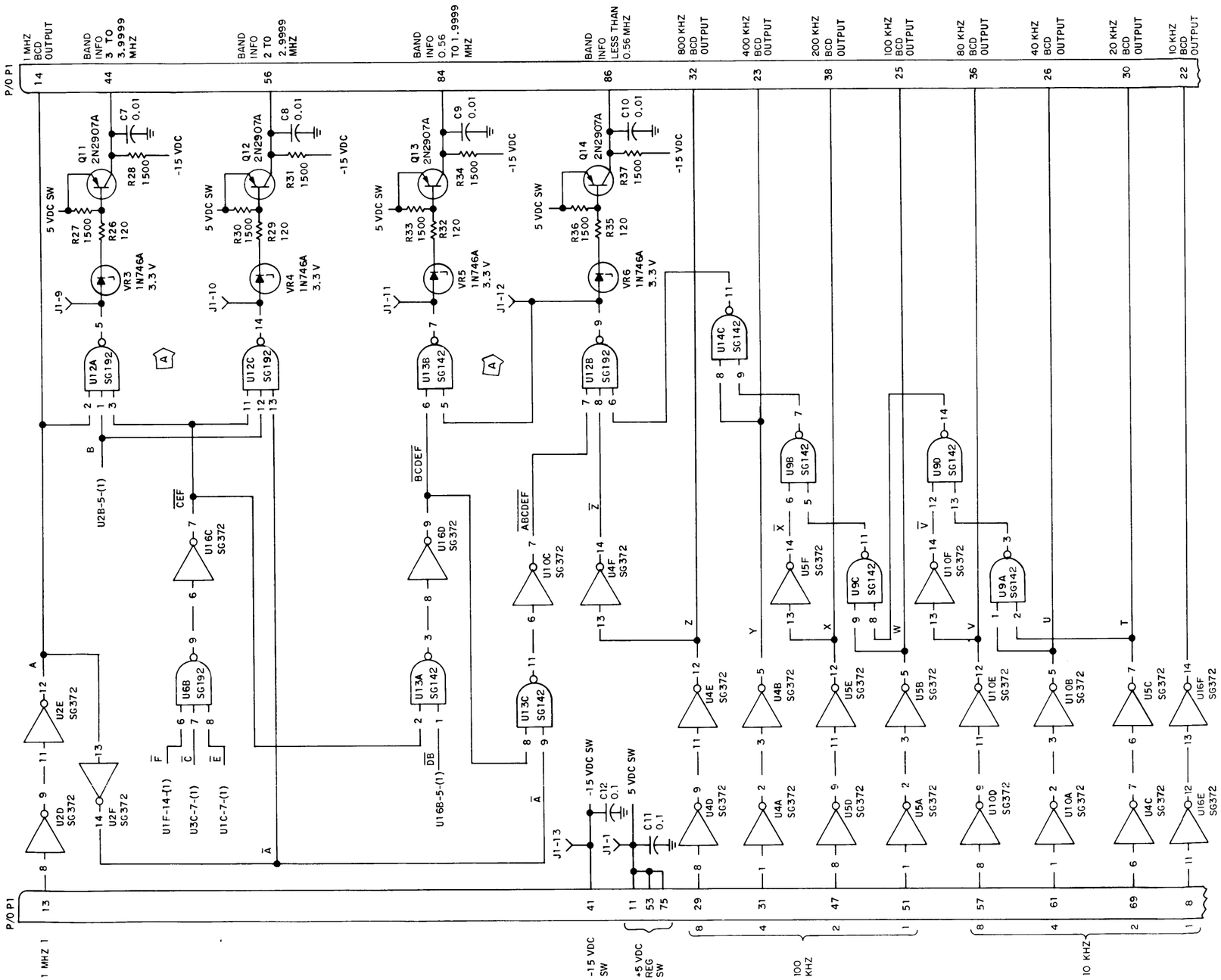
REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	Q2, Q4, Q6, Q8 through Q14 changed to 2N2907A's. R2, R6, R12, and R16 deleted.		72256
B	Microcircuits U1 through U17, SG373 types changed to SG372's, SG143 types changed to SG142's, and SG193 types changed to SG192's.		73046

Decoder/Driver Card A7 (778-2928-003), Schematic Diagram
Figure 16 (Sheet A)



618-0458
TP3-0511-025

Decoder/Driver Card A7 (778-2928-003), Schematic Diagram
Figure 16 (Sheet 1 of 2)

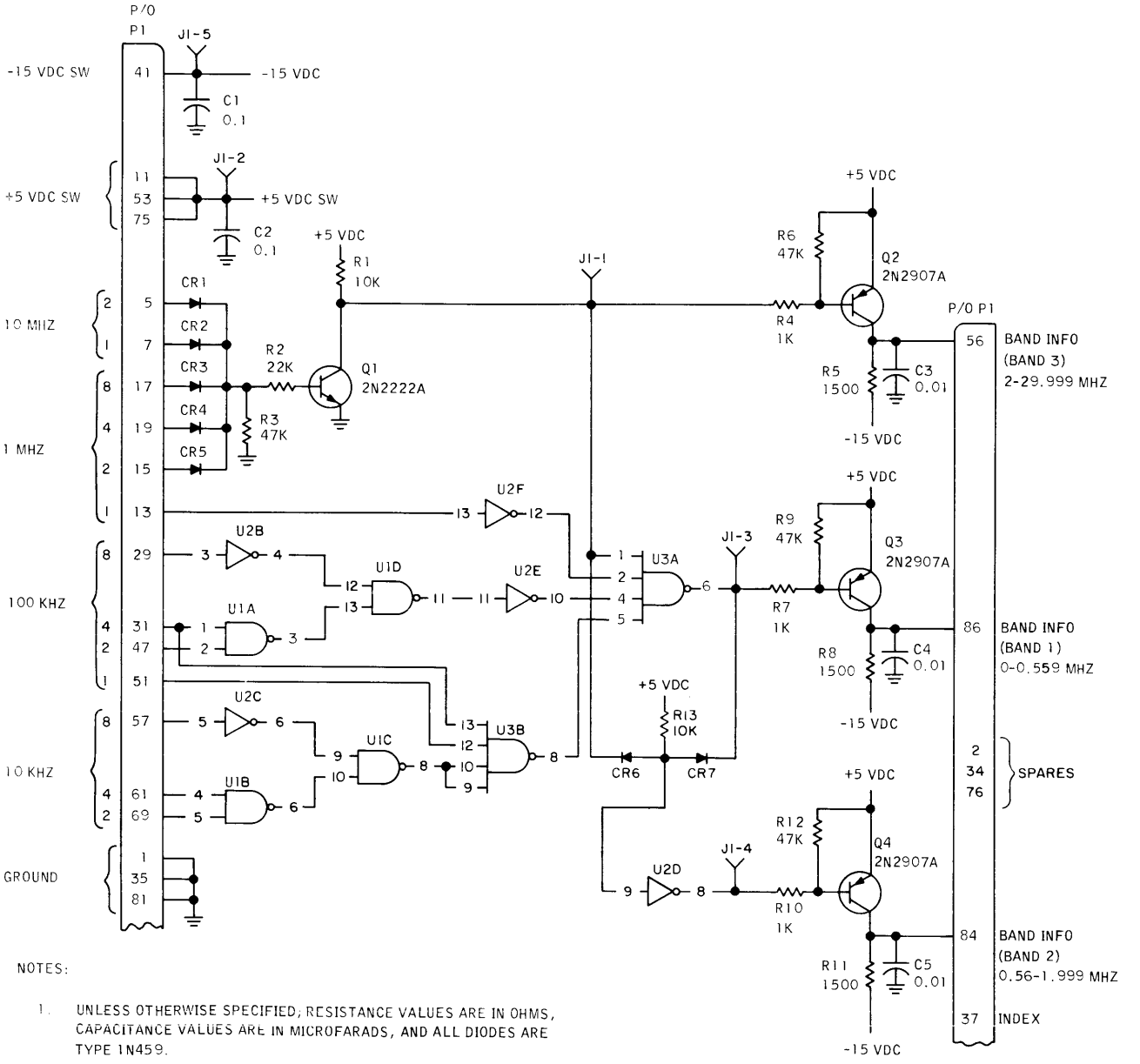


NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. UNLESS OTHERWISE SPECIFIED; MICROCIRCUIT PIN NO. 4 IS 5 VDC AND PIN 10 IS GROUND, EXCEPT U6 THROUGH U14 PIN NO. 4 IS 5 VDC SWITCHED.
3. SWITCHED VOLTAGE FUNCTIONS ARE:
   5 VDC SW=ON
   -15 VDC SW=OFF

618-0458
TP3-0341-025

Decoder/Driver Card A7 (778-2928-003), Schematic Diagram
Figure 16 (Sheet 2 of 2)

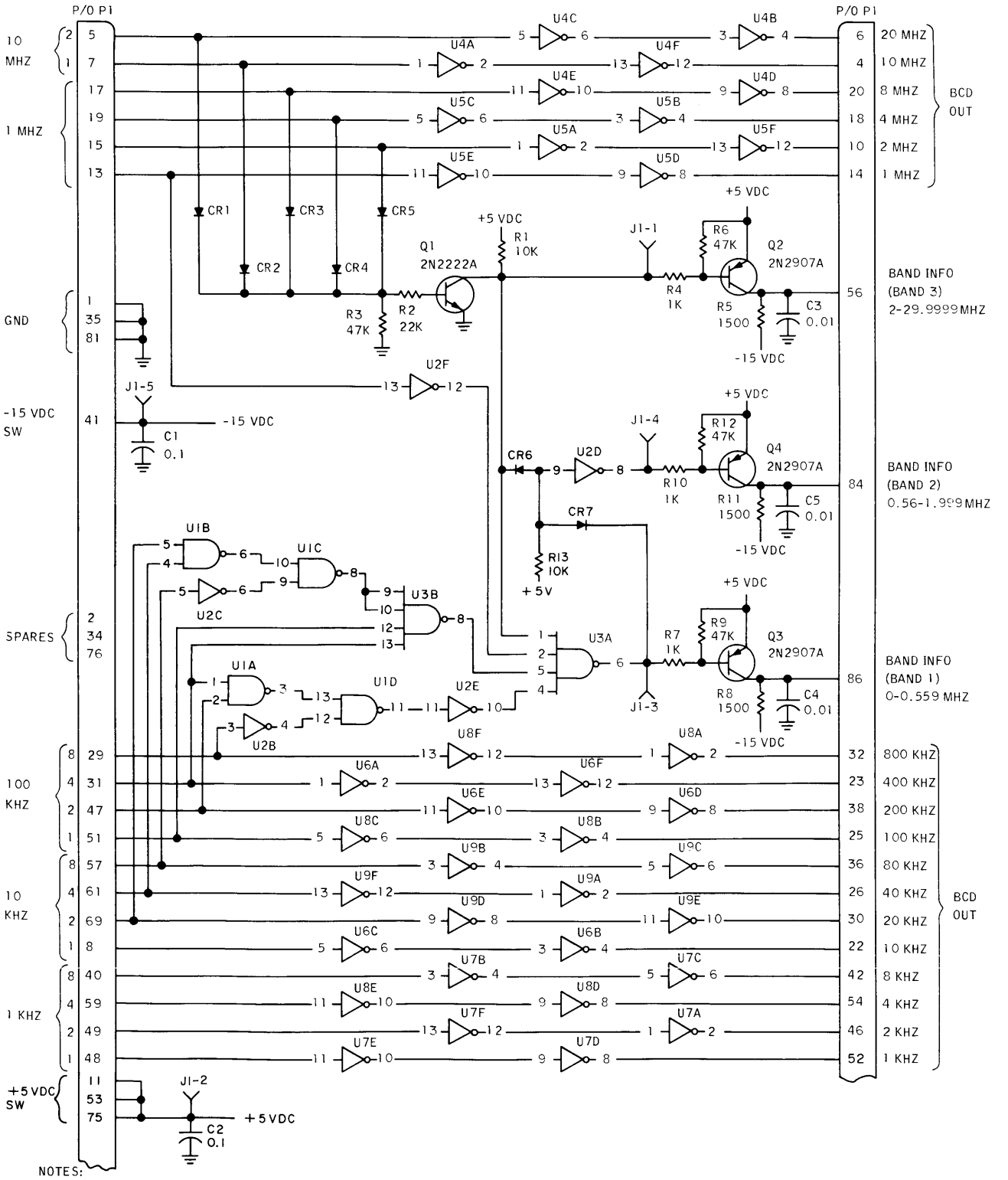


NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND ALL DIODES ARE TYPE 1N459.
2. UNLESS OTHERWISE SPECIFIED; MICROCIRCUIT PIN 14 IS +5 VDC AND PIN 7 IS GROUND.
3. MICROCIRCUIT TYPES; U1 DM7400N, U2 DM7404N, U3 DM7420N.

621-3135
TP3-1851-014

Decoder/Driver Card A7 (608-9087-001), Schematic Diagram
Figure 17



NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND DIODES ARE TYPE 1N459.
2. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN; MICROCIRCUIT PIN 14 IS +5 VDC AND PIN 7 IS GROUND.
3. MICROCIRCUIT TYPES ARE: U1-DM7400N, U2 AND U4 THROUGH U9-DM7404N, U3-DM7420N.

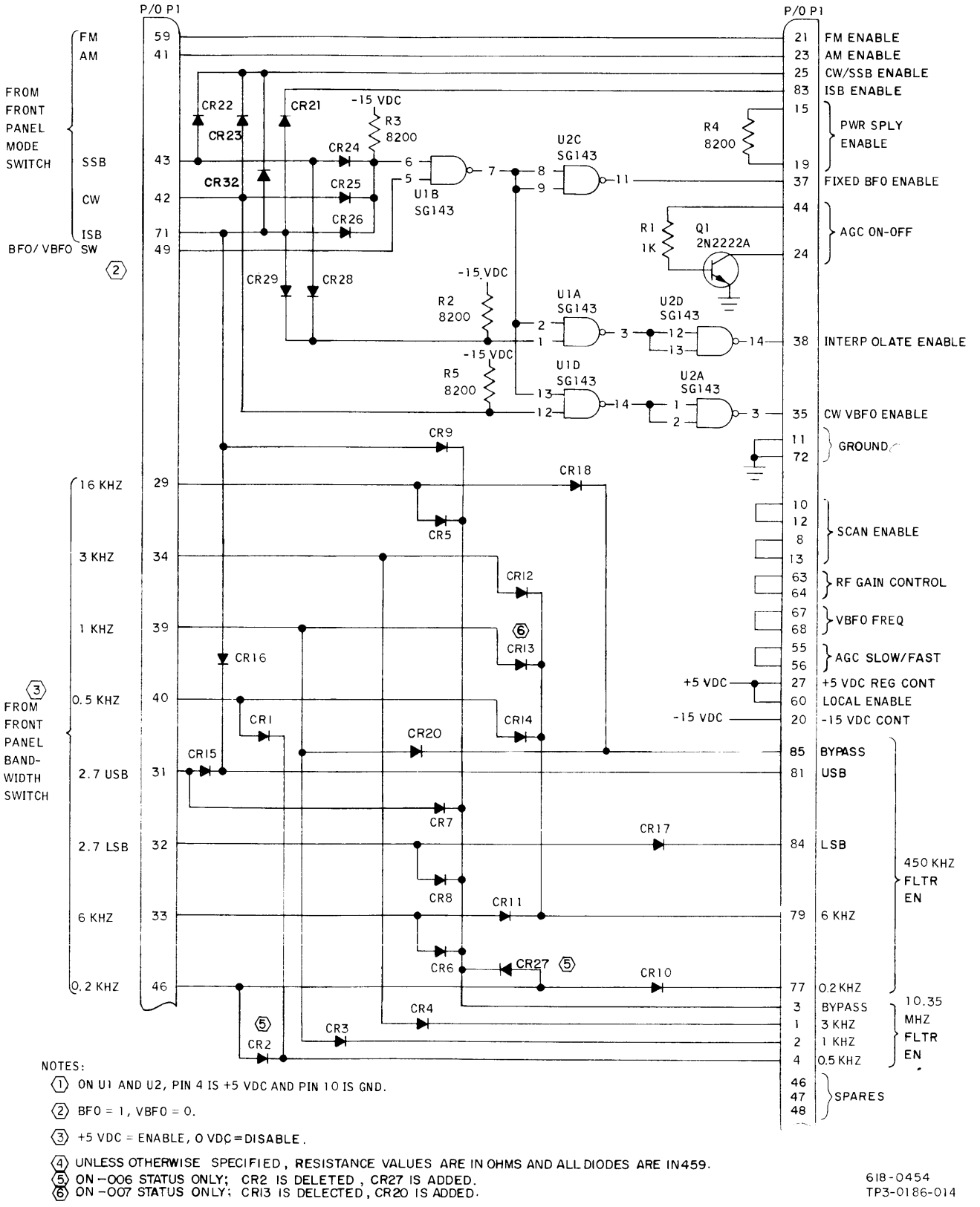
621-3134
TP3-2076-014

Decoder/Driver Card A7 (608-9121-001), Schematic Diagram
Figure 18

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
	Correct error on schematic. CR32 added.		All
	CR27 and note 5 added for -006 status. CR20 and note 6 added for -007 status.		Na

Interconnect Card A8 (778-2924-004, -006, -007), Schematic Diagram
Figure 19 (Sheet A)



NOTES:

(1) ON U1 AND U2, PIN 4 IS +5 VDC AND PIN 10 IS GND.

(2) BFO = 1, VBFO = 0.

(3) +5 VDC = ENABLE, 0 VDC = DISABLE.

(4) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS AND ALL DIODES ARE IN459.

(5) ON -006 STATUS ONLY; CR2 IS DELETED, CR27 IS ADDED.

(6) ON -007 STATUS ONLY; CR13 IS DELECTED, CR20 IS ADDED.

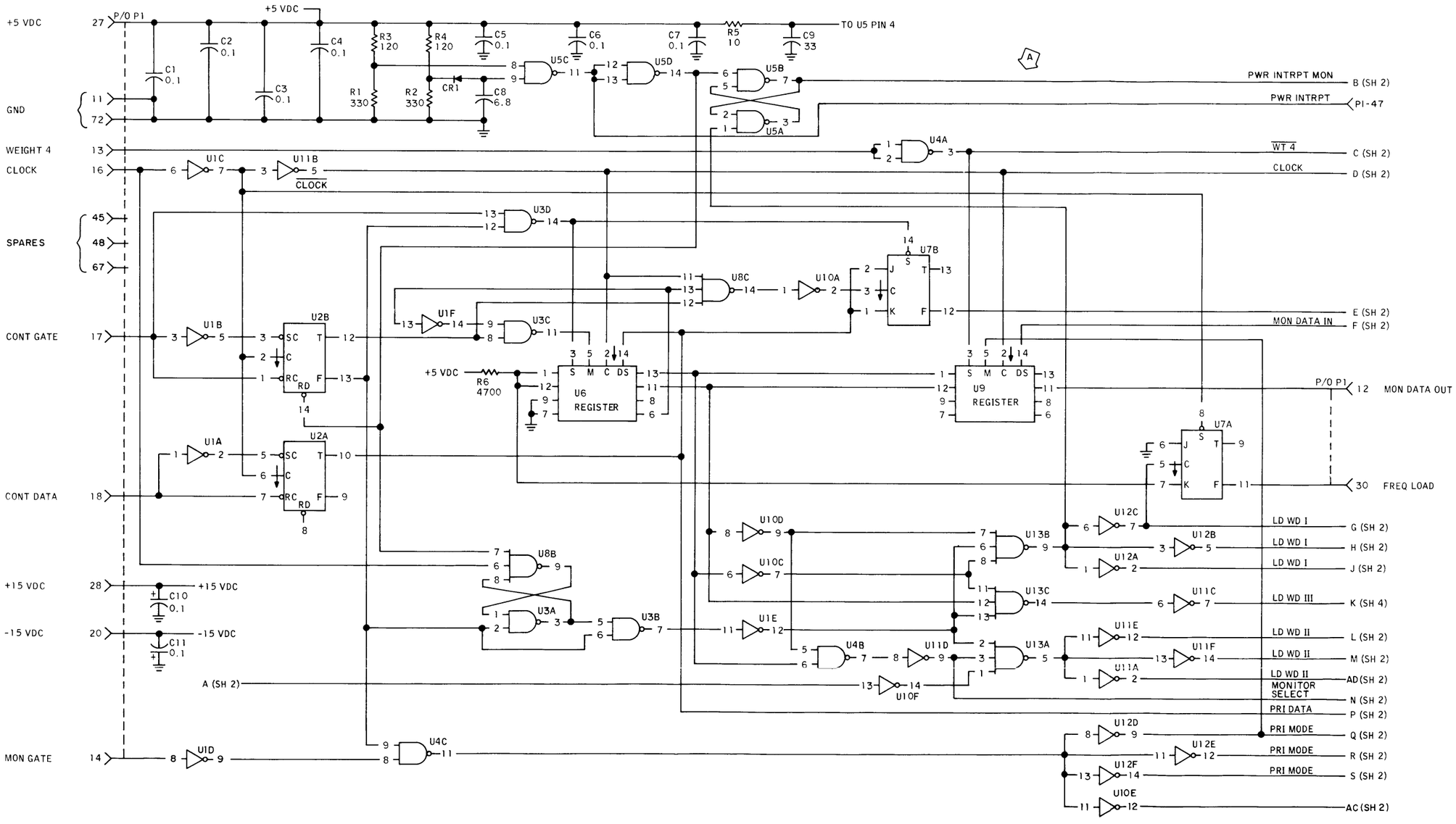
618-0454
TP3-0186-014

Interconnect Card A8 (778-2924-004, -006, -007), Schematic Diagram
Figure 19

SCHEMATIC CHANGES

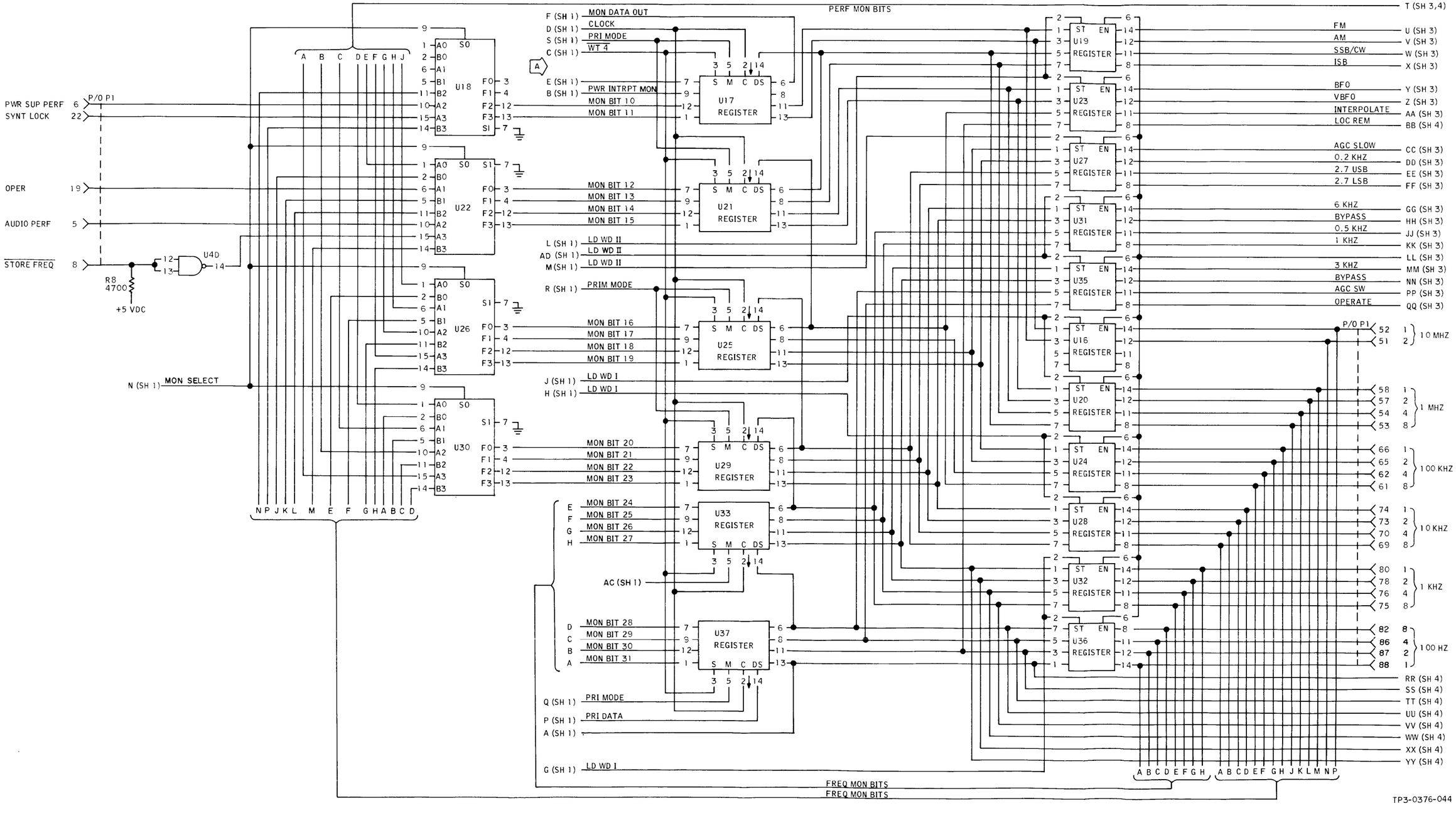
REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	Corrected preliminary schematic, added power interrupt monitor circuit. CR43 added. R14, R17 through R23 changed to 2200 ohms. R15 and R16 changed to 1 kΩ.		All
B	R35 and R37 changed to test select components to improve the VBFO frequency output.		73036

DCFE Card A8 (624-5744-001) (Optional), Schematic Diagram
Figure 20 (Sheet A)

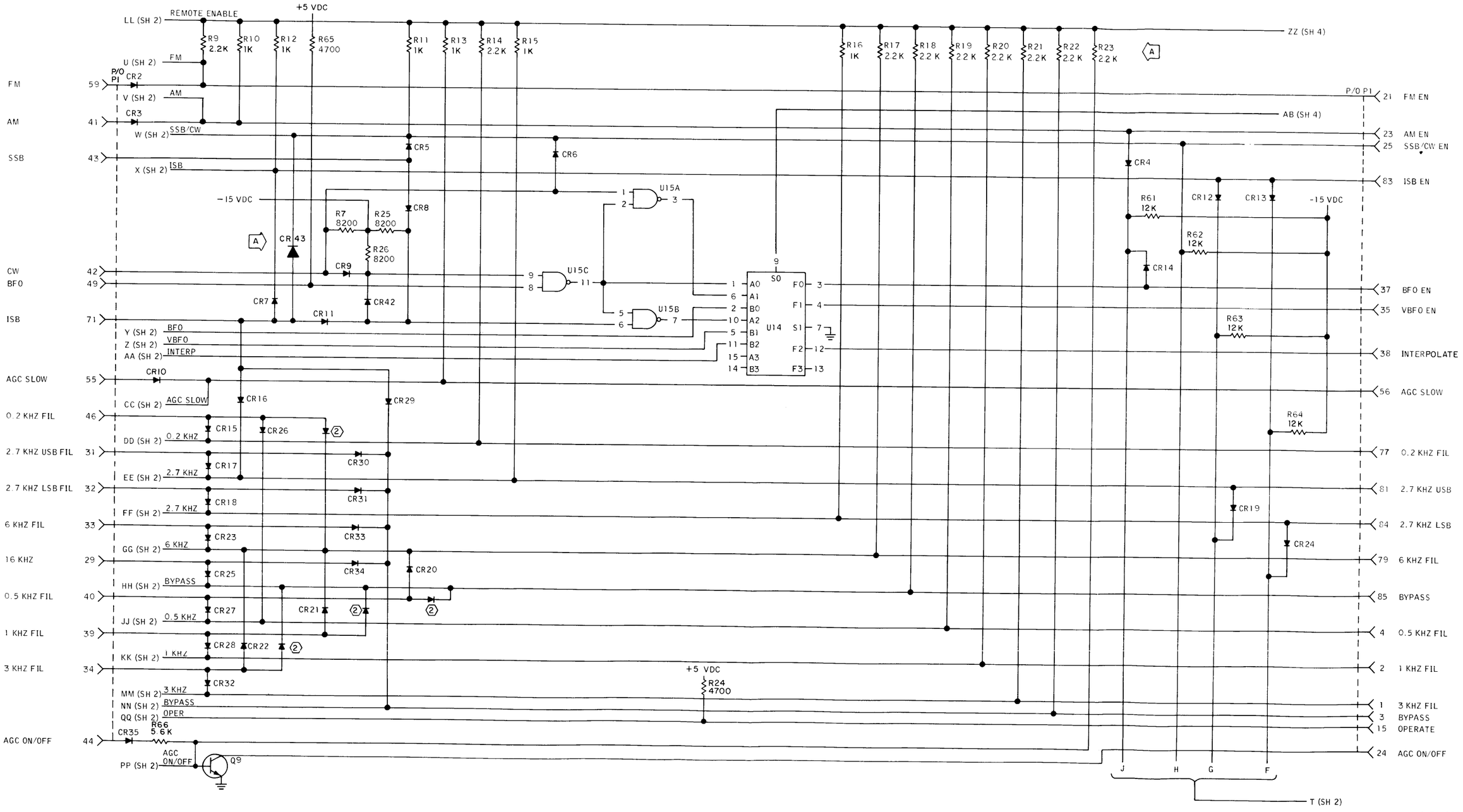


TP3-0376-044

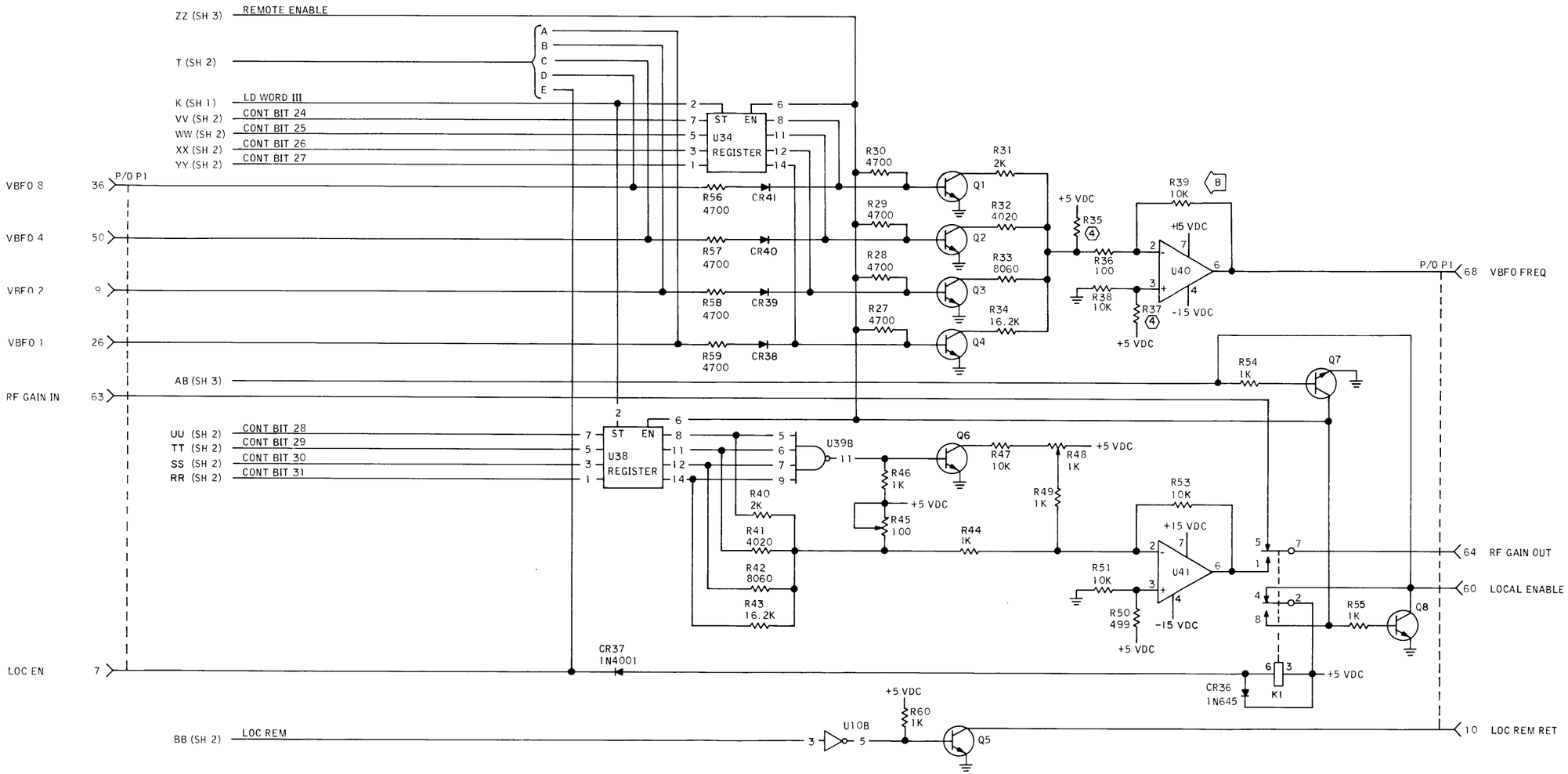
DCFE Card A8 (624-5744-001) (Optional), Schematic Diagram
Figure 20 (Sheet 1 of 4)



DCFE Card A8 (624-5744-001) (Optional), Schematic Diagram
Figure 20 (Sheet 2 of 4)



DCFE Card A8 (624-5744-001) (Optional), Schematic Diagram
Figure 20 (Sheet 3 of 4)



NOTES:

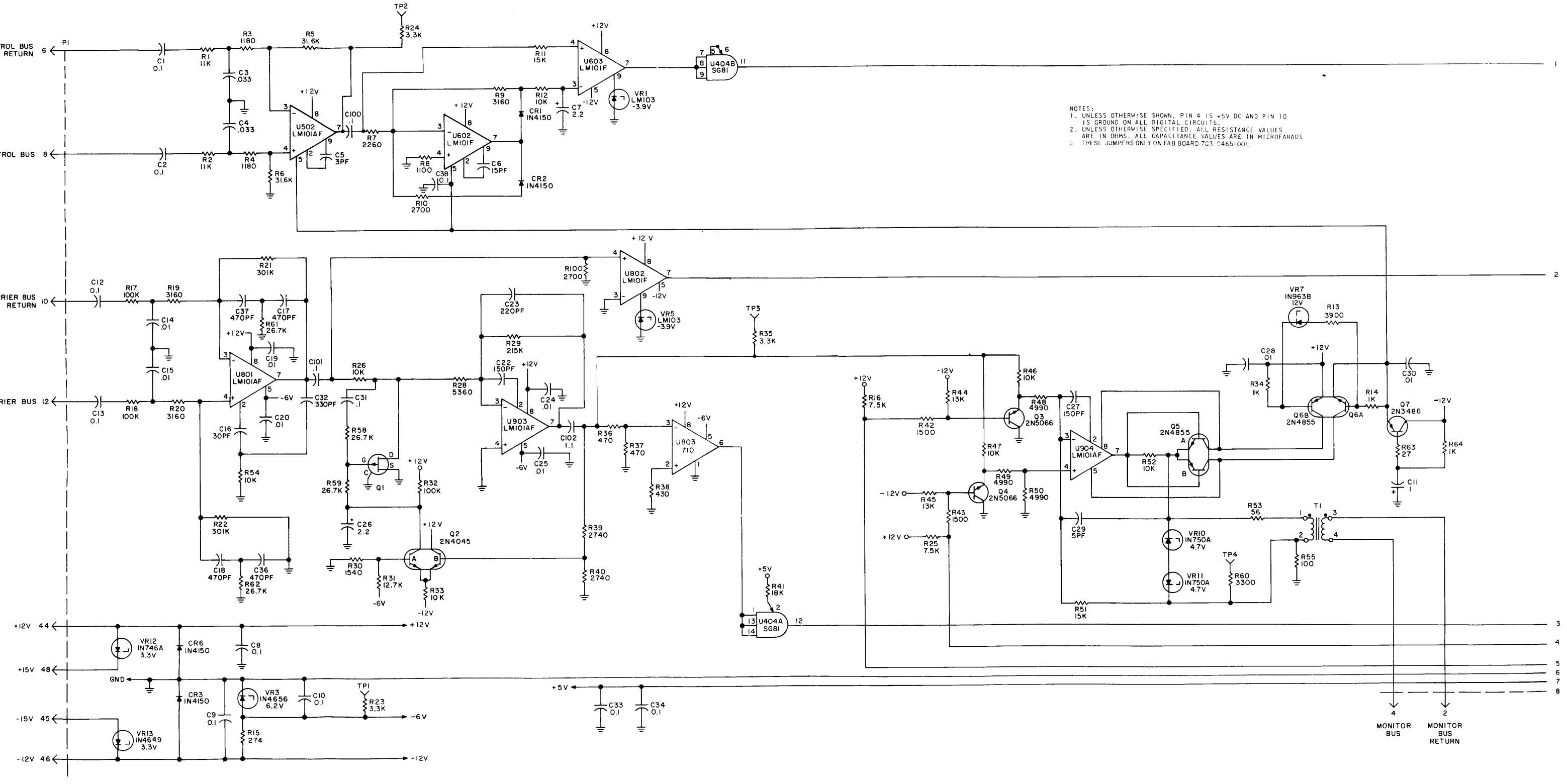
1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS. DIODES ARE IN 1N459, AND TRANSISTORS ARE 2N2222A.
2. THESE DIODES MAY BE INSTALLED AT USERS OPTION. HOLES ARE PROVIDED.
3. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN NO. 4 IS +5 VDC AND PIN 10 IS GROUND.
4. R35 AND R37 ARE TEST SELECT COMPONENTS, SEE PARTS LIST FOR TABLE OF VALUES.

TABLE I: MICROCIRCUIT TYPES:

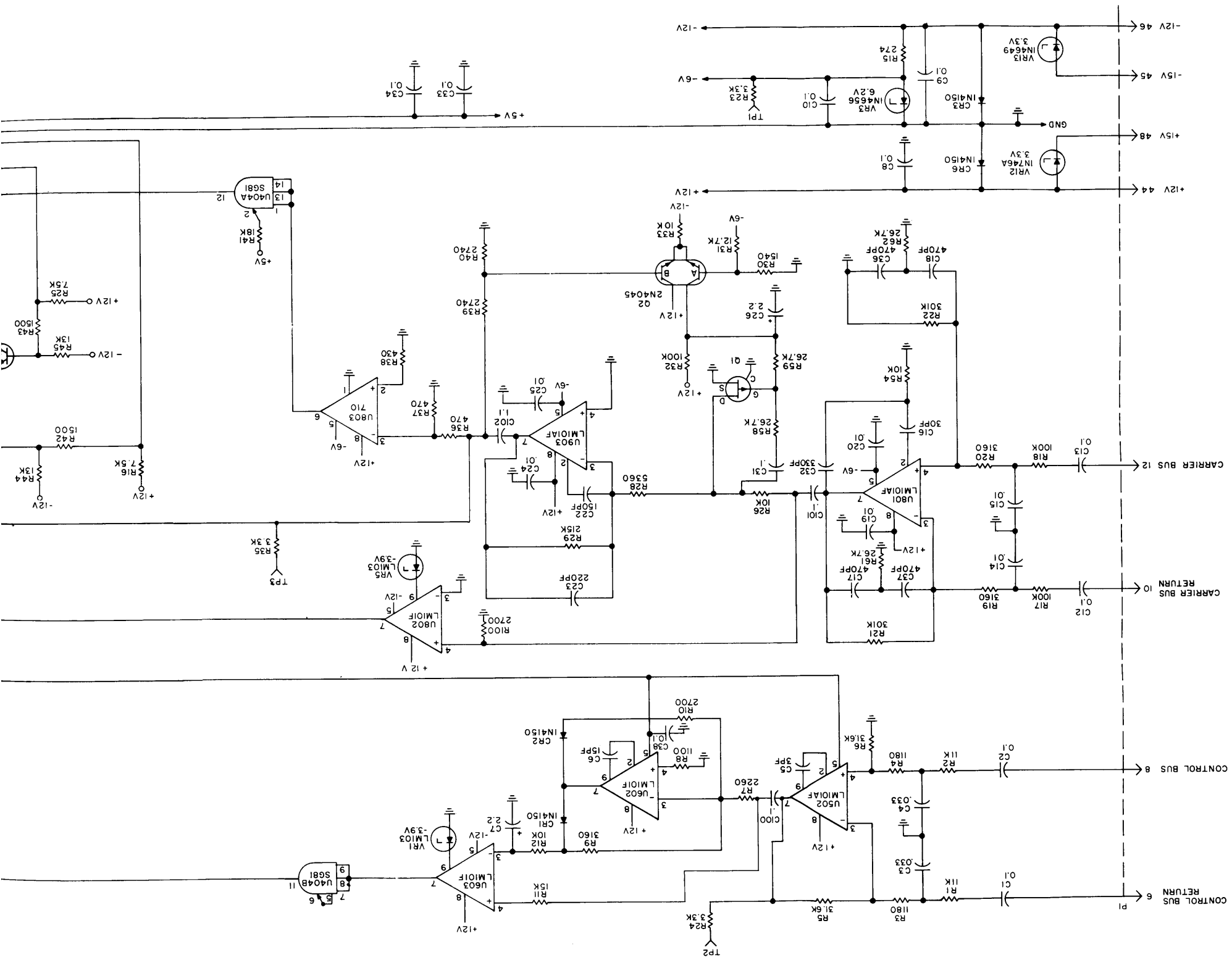
TENS	UNITS									
	0	1	2	3	4	5	6	7	8	9
0		SG373	8424J	SG143	SG143	SG143	SS226	SF103	SG193	SS226
1	SG373	SG372	SG372	SG193	8266	SG143	SM63	SS226	8233R	SM63
2	SM63	SS226	8233R	SM73	SM63	SS226	8233R	SM63	SM63	SS226
3	8233R	SM63	SM63	SS226	SM63	SM63	SM63	SS226	SM63	SG43
4	UA741	UA741								

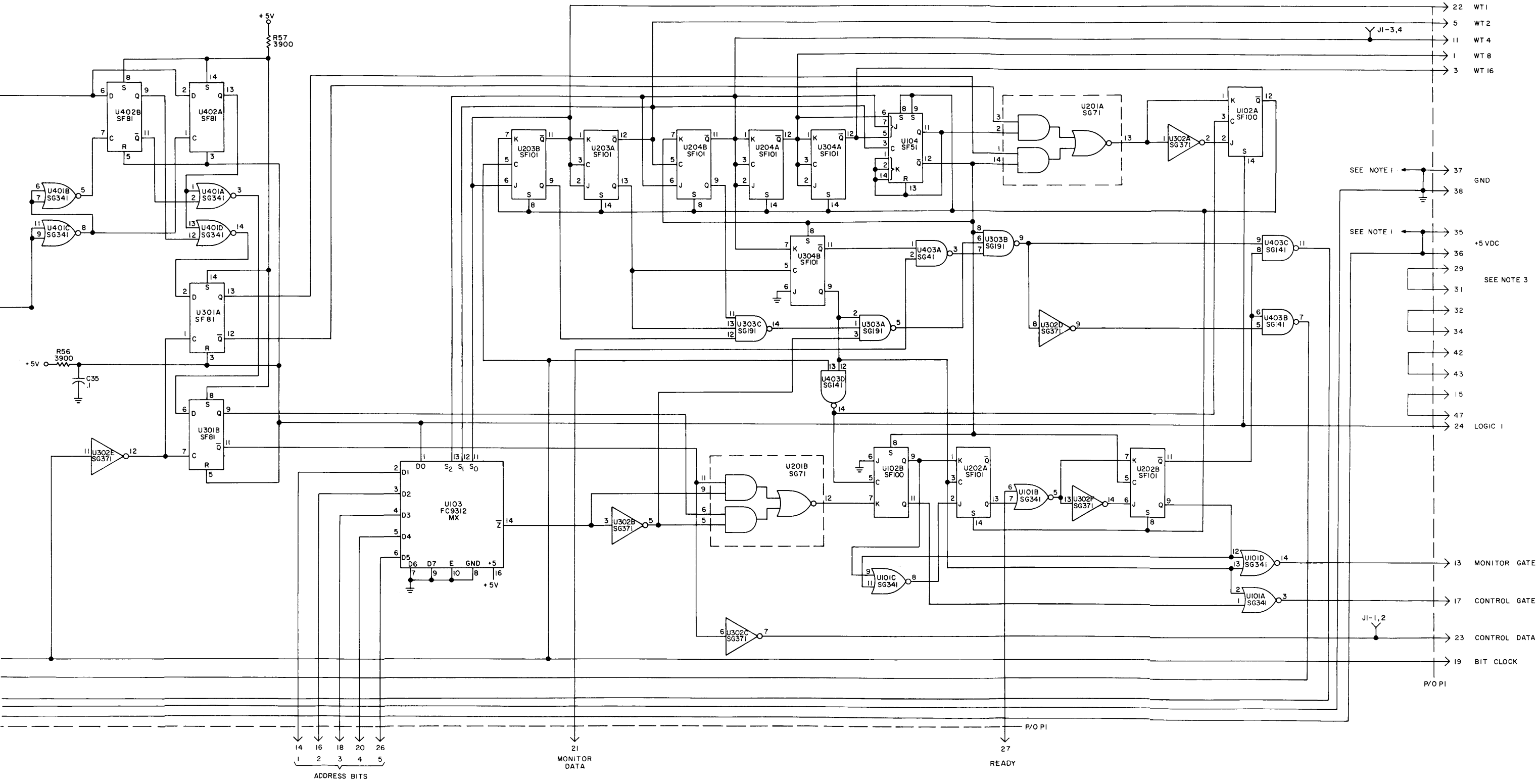
TP3-0376-044

DCFE Card A8 (624-5744-001) (Optional), Schematic Diagram
Figure 20 (Sheet 4 of 4)



DCU Card A9 (793-9414-001) (Optional), Schematic Diagram
Figure 21 (Sheet 1 of 2)


+5V
-12V
-6V
GND
+15V 48
+12V 44
-12V 46
-15V 45
CARRIER BUS 12
CARRIER BUS RETURN 10
CONTROL BUS 8
CONTROL BUS RETURN 6
P1
TP1
TP2
TP3
VR12 IN746A 3.3V
VR13 IN4649 3.3V
VR3 IN4656 6.2V
VR5 LM103 -3.9V
VR1 LM103 -3.9V
CR3 IN4150
CR6 IN4150
CR1 IN4150
CR2 IN4150
C8 0.1
C9 0.1
C10 0.1
C33 0.1
C34 0.1
R15 274
R23 3.3K
R35 3.3K
U404A SG81
U404B SG81
R41 18K
R43 150Ω
R45 13K
R25 7.5K
R42 150Ω
R44 13K
R16 7.5K
R40 274Ω
R39 274Ω
R38 430
R37 470
R36 470
U803 710
C102 .1
C25 .01
C24 .01
U903 LM101AF
C22 150PF
R28 536Ω
R29 215K
220PF C23
R100 270Ω
U802 LM101F
R33 10K
R31 12.7K
R30 154Ω
Q2 2N4045
C26 2.2
R32 100K
Q1
R59 26.7K
R58 26.7K
C31 .1
C32 330PF
R26 10K
C101 .1
U901 LM101AF
C18 470PF
R62 26.7K
C36 470PF
R22 30K
R54 10K
C16 30PF
C20 .01
C19 .01
C15 .01
C14 .01
C17 470PF
C37 470PF
R61 26.7K
R21 30K
R20 316Ω
R18 100K
C13 0.1
R19 316Ω
R17 100K
C12 0.1
C38 .01
R8 110Ω
C6 15PF
U602 LM101F
R7 226Ω
C100 .1
U502 LM101AF
C5 3PF
R6 31.6K
R4 118Ω
R2 11K
C2 0.1
C4 .033
C3 .033
R3 118Ω
R5 31.6K
R24 3.3K
R11 15K
U603 LM101F
R12 10K
R9 316Ω
C7 2.2
C1 0.1
R1 11K



DCU Card A9 (793-9414-001) (Optional), Schematic Diagram
Figure 21 (Sheet 2 of 2)

ADDRESS BITS

1 2 3 4 5

14 16 18 20 26

MONITOR DATA

21

8 7 6 5 4 3 2 1

+5V

R56 390Ω

C35 .1

U30IB SF8I

U30IA SF8I

U40IA SG34I

U40ID SG34I

U40IC SG34I

U40IB SG34I

U40IC SG34I

U30IB SF8I

U40IA SF8I

U40IB SF8I

U40IC SF8I

U40ID

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
None	Corrected schematic errors to reflect production configuration.		All

DCU Card A9 (624-5781-001) (Optional), Schematic Diagram
Figure 22 (Sheet A)

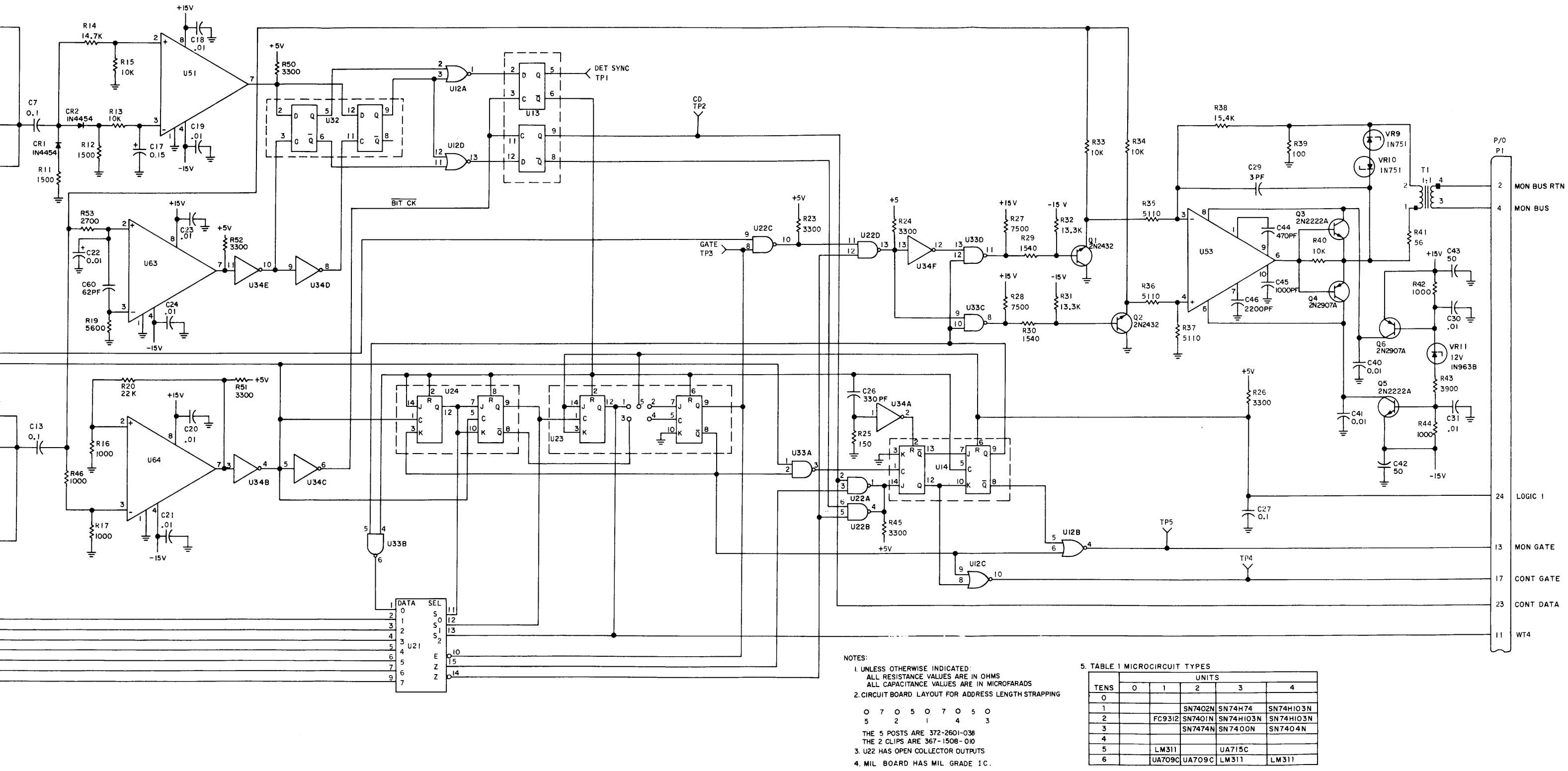
NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN; MICROCIRCUIT PIN NO 14 IS +5 VDC AND PIN NO. 7 IS GROUND EXCEPT SF101 AND SF103. PIN NO. 10 IS +5 VDC AND PIN NO. 4 IS GND.

TENS	UNITS				
	0	1	2	3	4
0					
1			7402N	7474J	SF103
2		9312	7401N	SF103	SF101
3			7474J	7400N	7404N
4					
5		LM301		LM301	
6		709C	709C	LM301	LM301

TP3-2222-014

DCU Card A9 (624-5781-001) (Optional), Schematic Diagram
Figure 22



NOTES:

1. UNLESS OTHERWISE INDICATED:
   ALL RESISTANCE VALUES ARE IN OHMS
   ALL CAPACITANCE VALUES ARE IN MICROFARADS
2. CIRCUIT BOARD LAYOUT FOR ADDRESS LENGTH STRAPPING

   O 7 O 5 O 7 O 5 O
   5 2 1 4 3

   THE 5 POSTS ARE 372-2601-038
   THE 2 CLIPS ARE 367-1508-010
3. U22 HAS OPEN COLLECTOR OUTPUTS
4. MIL BOARD HAS MIL GRADE IC.

5. TABLE 1 MICROCIRCUIT TYPES

TENS	UNITS 0	1	2	3	4
0					
1			SN7402N	SN74H74	SN74H103N
2		FC9312	SN7401N	SN74H103N	SN74H103N
3			SN7474N	SN7400N	SN7404N
4					
5		LM311		UA715C	
6		UA709C	UA709C	LM311	LM311

774-7843

DCU Card A9 (774-7842-001) (Optional), Schematic Diagram
Figure 23

NOTES:
1. UNLESS OTHERWISE INDICATED
ALL RESISTANCE VALUES ARE
ALL CAPACITANCE VALUES AR
2. CIRCUIT BOARD LAYOUT FOR A
O 7 O 5 O 7 O 4
5 2 1
THE 5 POSTS ARE 372-2601-0
THE 2 CLIPS ARE 367-1508-0
3. U22 HAS OPEN COLLECTOR OUT
4. MIL BOARD HAS MIL GRAD

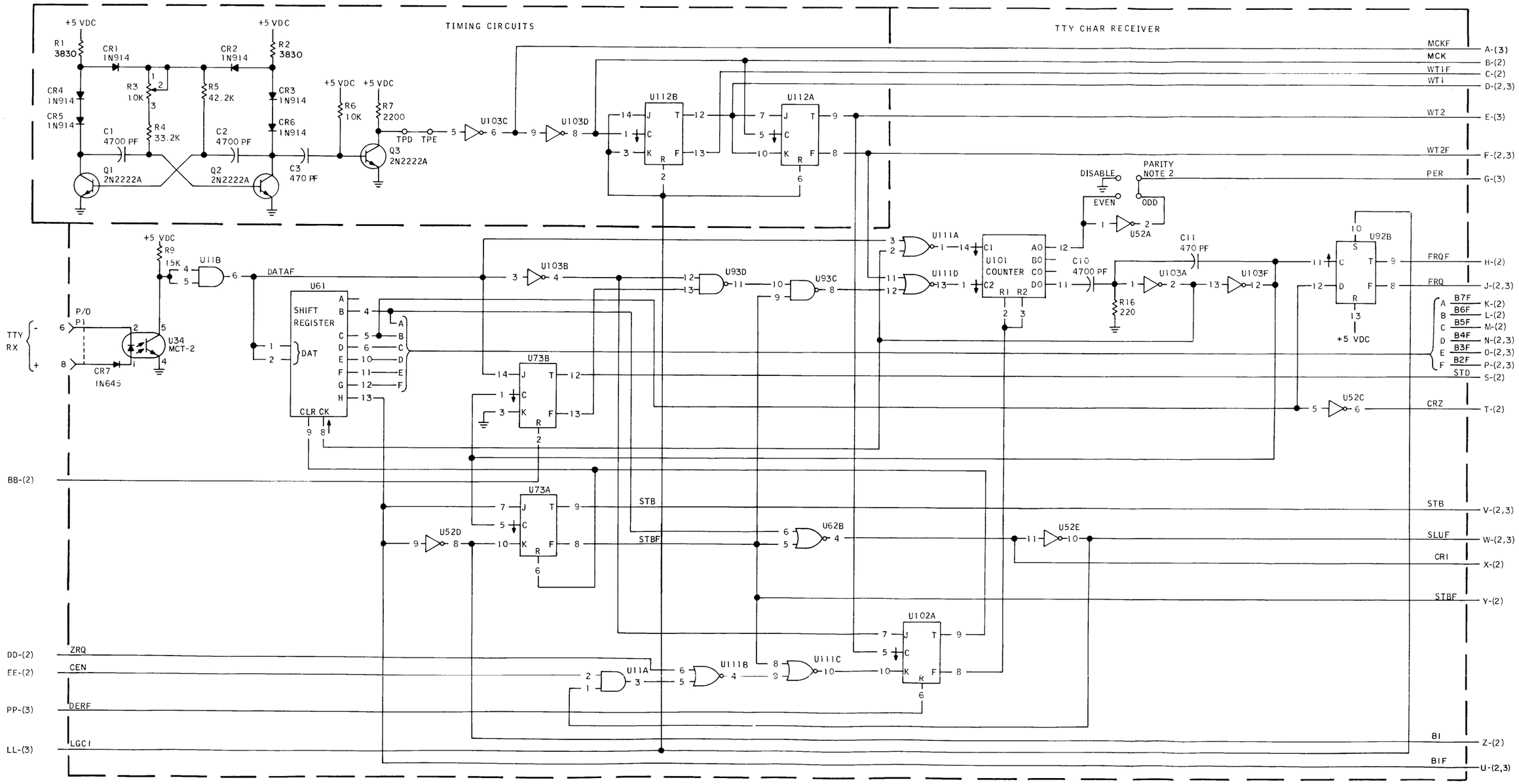
P1/O
CONT BUS RTN 6
CONT BUS 8
+15V 48
+15V 44
GND 37
GND 38
-15V 45
-15V 46
MON DATA 21
BIT CK 19
CARR BUS RTN 10
CARR BUS 12
+5V 35
+5V 36
-15V 29
31
32
34
42
43
15
47
ADDRESS BIT 1 2 3 4 5 6 7
&TRAPPING

C1 0.1 R1 14.7K
C2 0.1 R2 14.7K
C3 .01 C4 .01
C5 10PF C6 3PF
R3 100 R4 100
R5 100K R54 1500
C7 0.1 R11 1500
CR1 IN4454 CR2 IN4454
C17 0.15 R12 1500
R13 10K R15 10K
C19 .01 C18 .01
U61 U62 U63 U64 U51
C8 0.1 R6 26.1K
C9 0.1 R7 26.1K
C10 .01 C11 .01
C12 10PF C25 3PF
R8 100 R9 100
R10 100K R55 1500
C13 0.1 R17 1000
R16 1000 R46 1000
C21 .01 C20 .01
R20 22K R51 3300
C15 0.1 C16 0.1 C32 0.1
CR3 IN4454 CR4 IN4454
C22 0.01 C60 62PF
R52 3300 R53 2700
C24 .01 R19 5600
C23 .01 R50 3300
U21 U22 U23 U24
U52 U53 U54
U12A U12B U12C U12D
U13 U32
U22A U22B U22C U22D
U33A U33B
U34A U34B U34C U34D U34E U34F
R45 3300 R23 3300 R24 3300
C26 330PF R25 150
U14
DATA SEL
GATE TP3
CD TP2
DET SYNC TP1
BIT CK

SCHEMATIC CHANGES

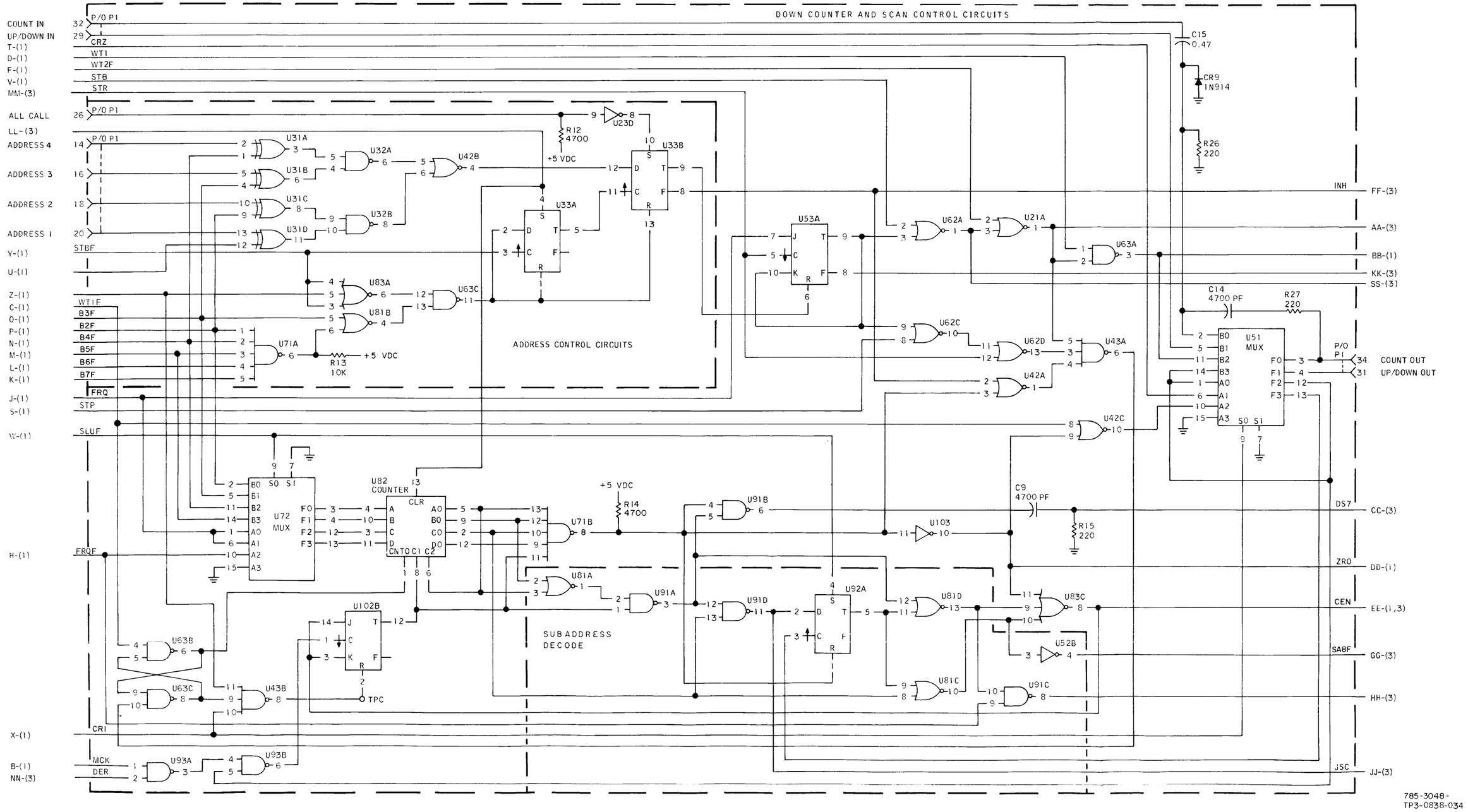
REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
None	Update preliminary schematic to reflect production configuration.		All

TCU Card A9 (783-9480-001) (Optional), Schematic Diagram
Figure 24 (Sheet A)



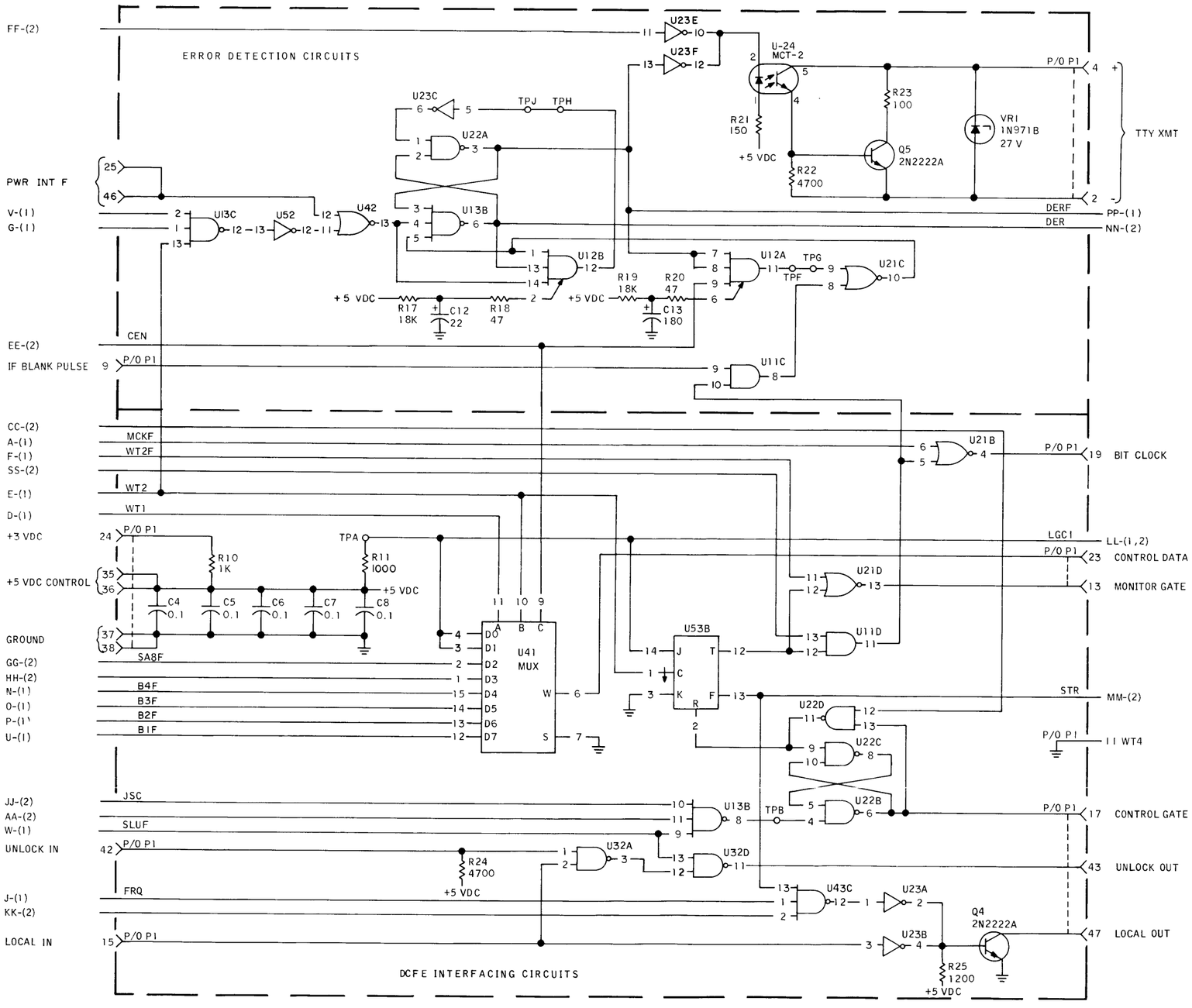
785-3048-
TP3-0838-034

TCU Card A9 (783-9480-001) (Optional), Schematic Diagram
Figure 24 (Sheet 1 of 3)



785-3048-TP3-0838-034

TCU Card A9 (783-9480-001) (Optional), Schematic Diagram
Figure 24 (Sheet 2 of 3)



NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. PARITY MAY BE DISABLED OR CONNECTED FOR EVEN PARITY BY ADDING JUMPER TO COMMON PIN AND BREAKING CIRCUIT TO ODD PARITY PIN.
3. UNLESS OTHERWISE SPECIFIED, ALL MICROCIRCUITS HAVE PIN 14 CONNECTED TO +5 VDC AND PIN 7 CONNECTED TO GROUND; EXCEPT:
   SN7493 - PIN 5 TO +5 VDC, PIN 10 TO GROUND
   S8266B - PIN 16 TO +5 VDC, PIN 8 TO GROUND
   SN74151 - PIN 16 TO +5 VDC, PIN 8 TO GROUND
   SN7473 - PIN 4 TO +5 VDC, PIN 11 TO GROUND
   SG83 - PIN 4 TO +5 VDC, PIN 10 TO GROUND

MICROCIRCUIT TYPES

TENS	UNITS				
	0	1	2	3	4
0					
1		SN7408	SG83	SN7410	
2		SN7402	SN7400	MC836P	MCT-2
3		SN7486	SN7400	SN7474	MCT-2
4		SN74151	SN7402	SN7410	
5		S8266B	SN7404	SN7473	
6		SN74164	SN7402	SN7400	
7		S8415A	S8266B	SN7473	
8		SN7402	SN74197	SN7427	
9		SN7400	SN7474	SN7400	
10		SN7493	SN74H103	SN7404	
11		SN7402	SN7473		

785-3048-TP3-0838-034

TCU Card A9 (783-9480-001) (Optional), Schematic Diagram
Figure 24 (Sheet 3 of 3)

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
None	Corrected schematic errors to reflect production configuration.		All

Auto Scan Control Card A9 (783-9368-001) (Optional), Schematic Diagram
Figure 25 (Sheet A)

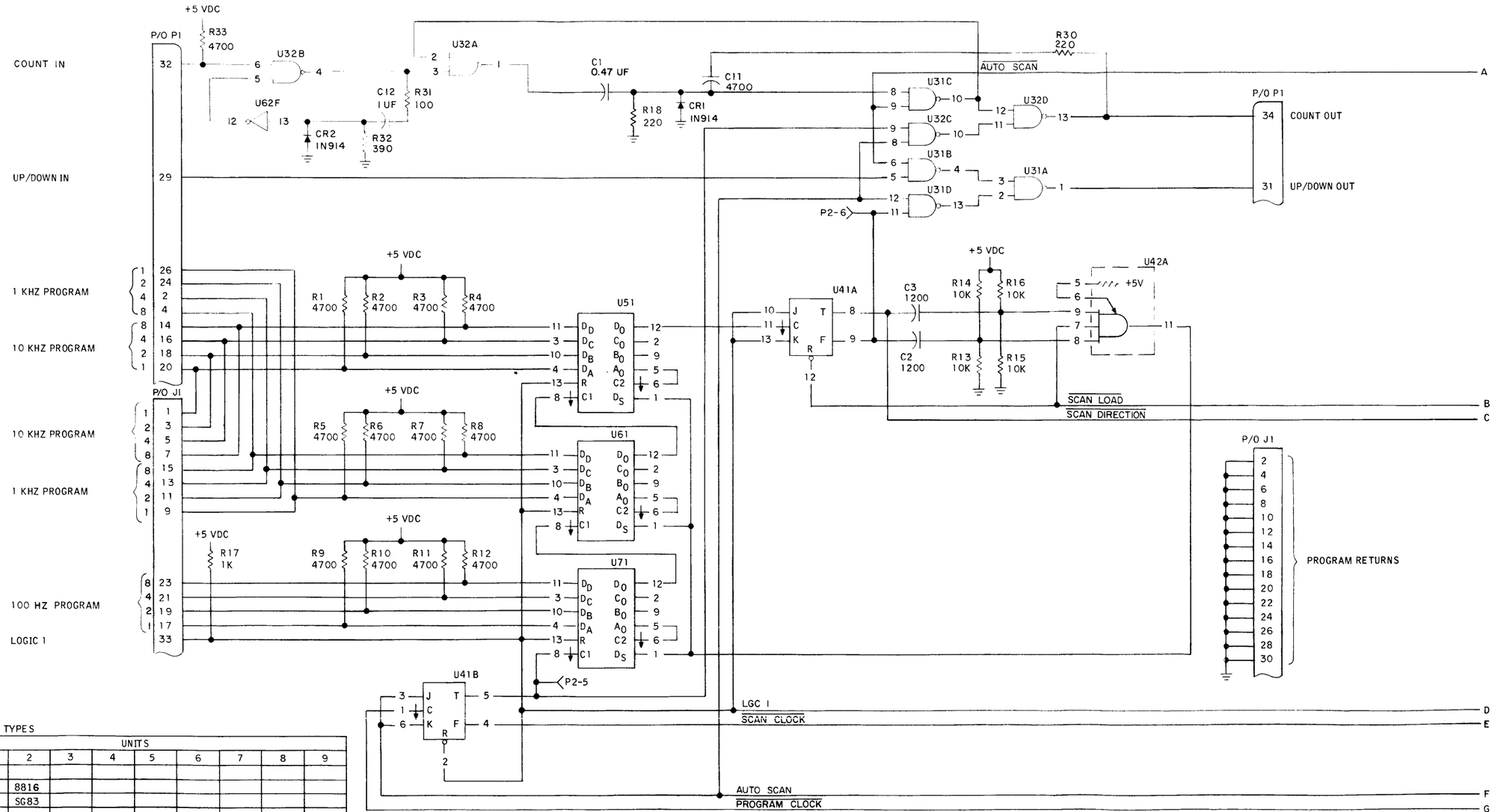


TABLE 1: MICROCIRCUIT TYPES

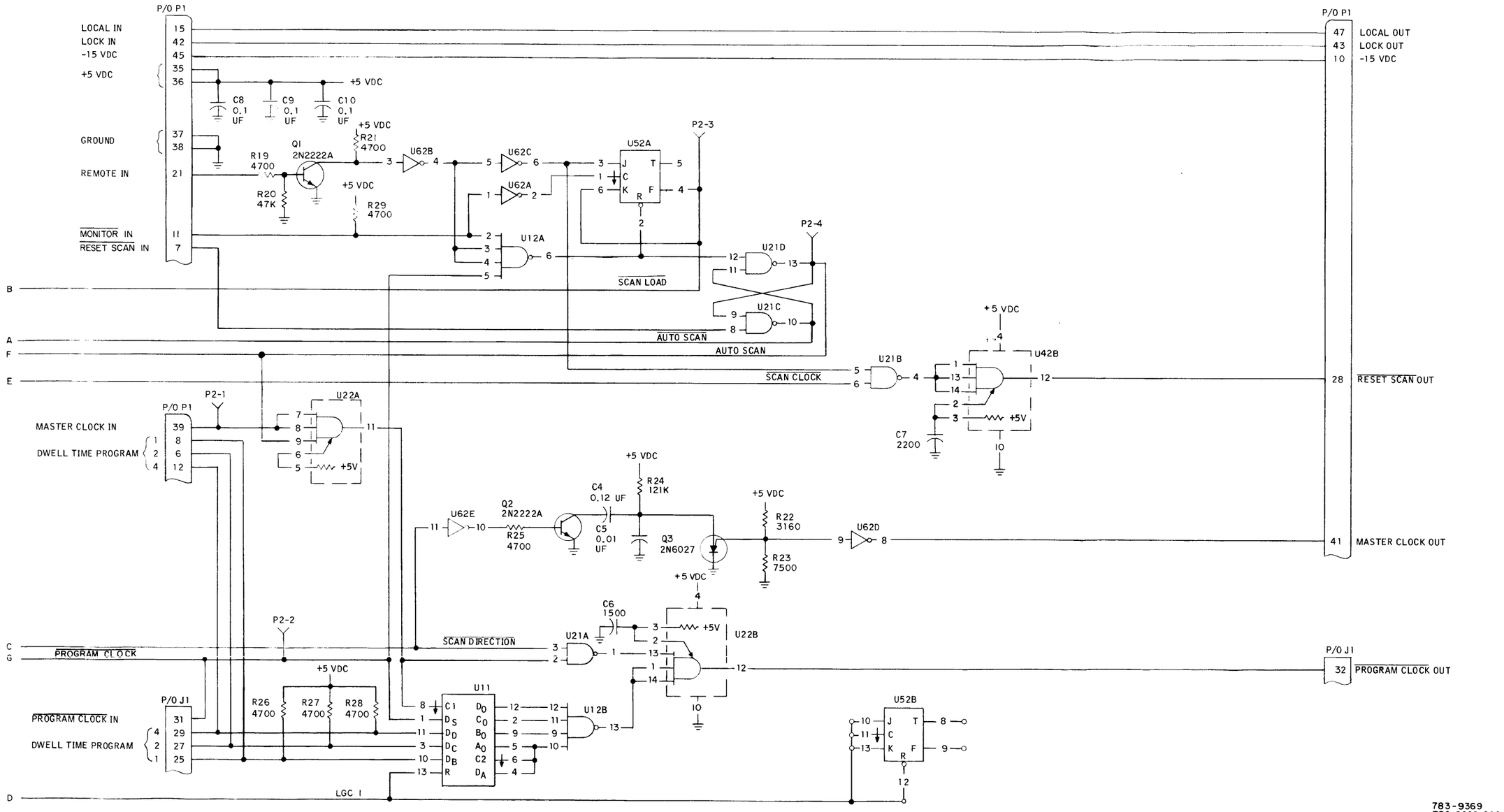
TENS	UNITS 0	1	2	3	4	5	6	7	8	9
0										
1		8281	8816							
2		8880	SG83							
3		8880	8880							
4		8822	SG83							
5		8280	8822							
6		8280	8890							
7		8280								
8										
9										

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, AND CAPACITANCE VALUES ARE IN PICOFARADS.
2. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN MICROCIRCUIT PIN 14 IS CONNECTED TO +5VDC AND PIN 7 IS CONNECTED TO GROUND.

783-9369
TP2-9602-024

Auto Scan Control Card A9 (783-9368-001) (Optional), Schematic Diagram
Figure 25 (Sheet 1 of 2)



783-9369
TP2-9602-024

Auto Scan Control Card A9 (783-9368-001) (Optional), Schematic Diagram
Figure 25 (Sheet 2 of 2)

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	C18 changed to .01 μF to improve the input level from the loop 2 mixer.		72056

Synthesizer Divider Card A10 (793-9334-002), Schematic Diagram
Figure 26 (Sheet A)

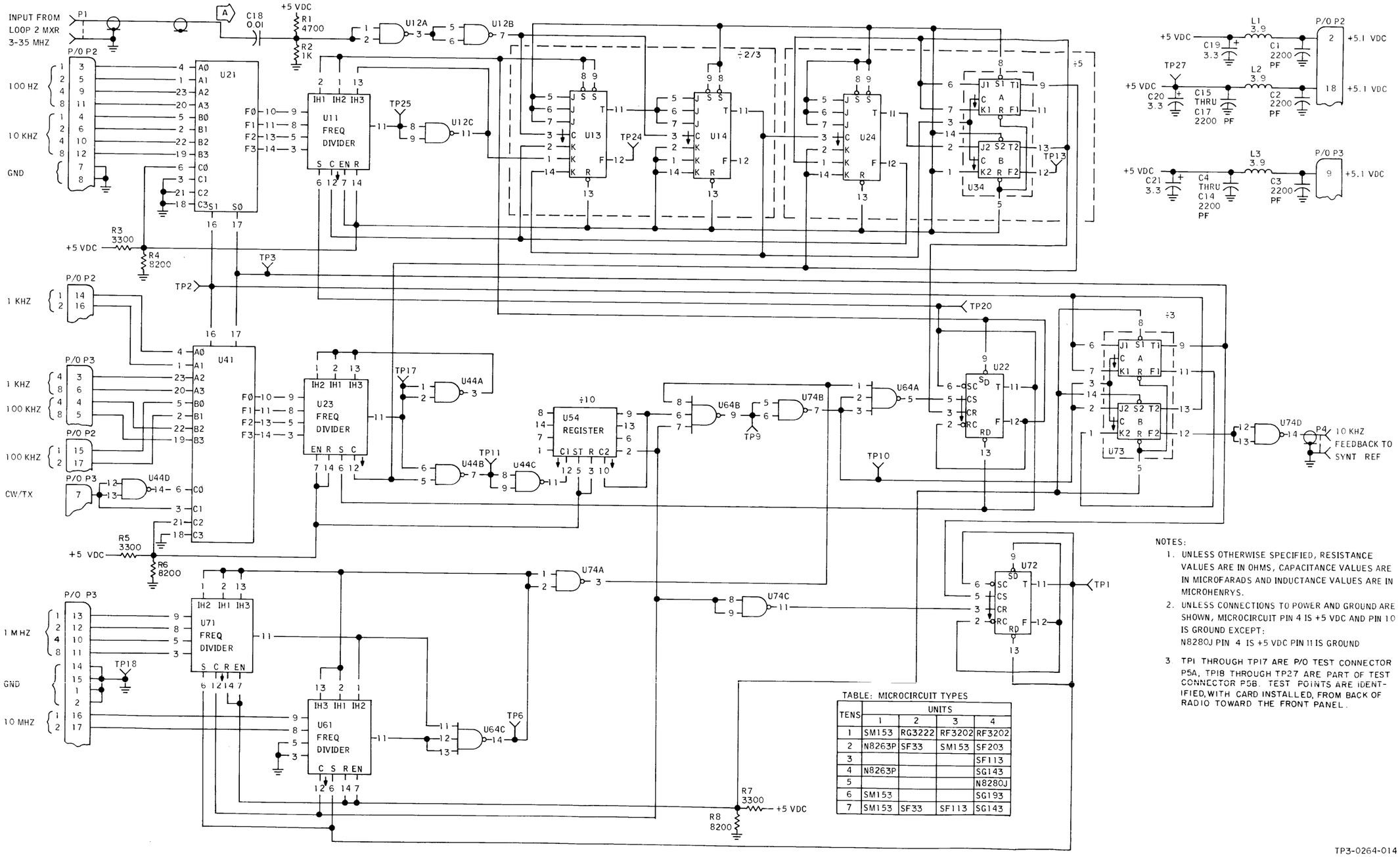


TABLE: MICROCIRCUIT TYPES

TENS	UNITS			
	1	2	3	4
1	SM153	RG3222	RF3202	RF3202
2	N8263P	SF33	SM153	SF203
3				SF113
4	N8263P			SG143
5				N8280J
6	SM153			SG193
7	SM153	SF33	SF113	SG143

NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN 4 IS +5 VDC AND PIN 10 IS GROUND EXCEPT:
   N8280J PIN 4 IS +5 VDC PIN 11 IS GROUND
3. TP1 THROUGH TP17 ARE P/O TEST CONNECTOR P5A, TP18 THROUGH TP27 ARE PART OF TEST CONNECTOR P5B. TEST POINTS ARE IDENTIFIED, WITH CARD INSTALLED, FROM BACK OF RADIO TOWARD THE FRONT PANEL.

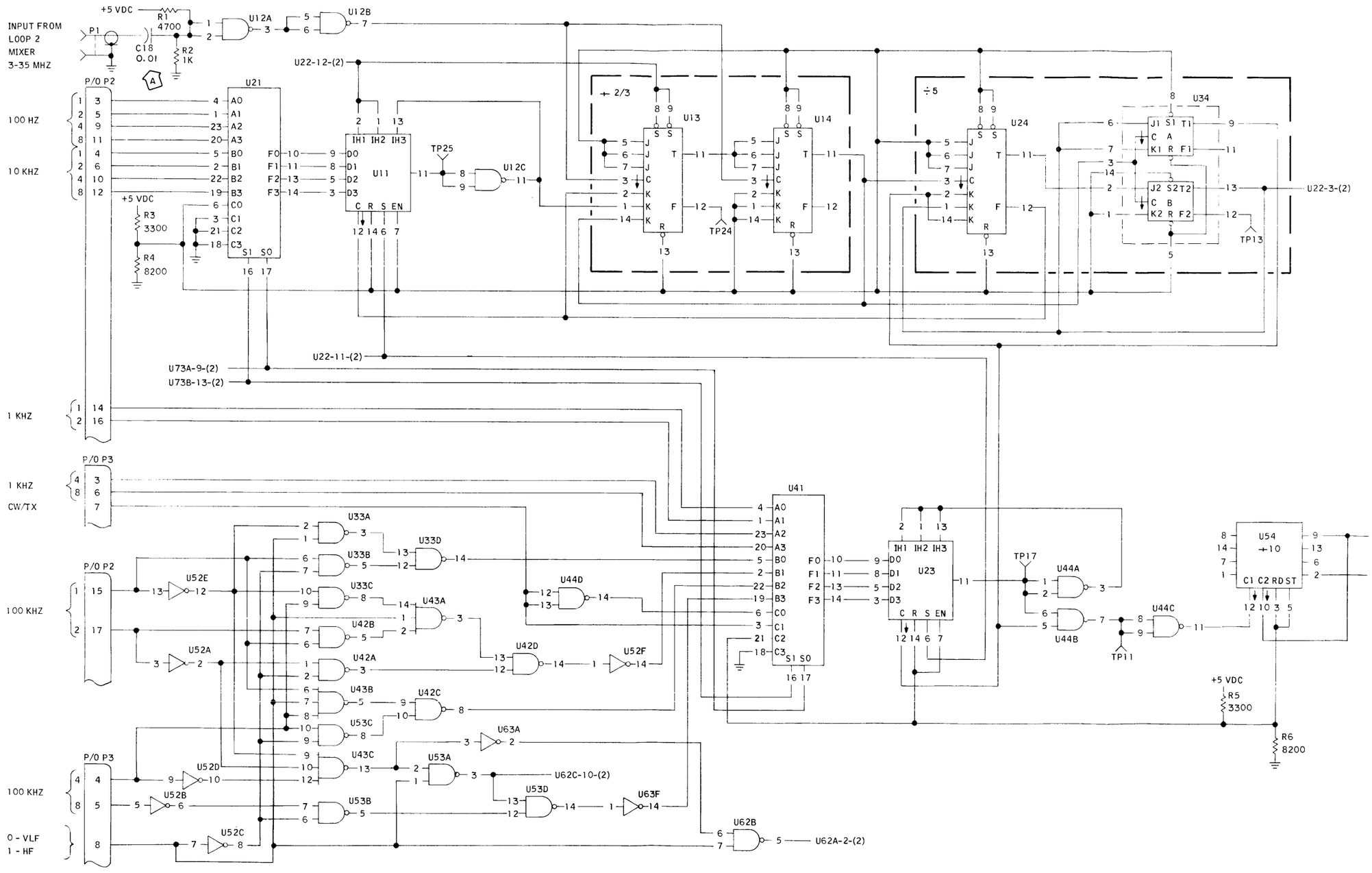
TP3-0264-014

Synthesizer Divider Card A10 (793-9334-002), Schematic Diagram
Figure 26

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
	Updated preliminary schematic. Added wiring change to vlf/hf input.		All
A	C18 changed to .01 μF to improve the input level from loop 2 mixer.		72056

VLF Synthesizer Divider Card A10 (793-9334-006), Schematic Diagram
Figure 27 (Sheet A)



TP3-0263-024

VLF Synthesizer Divider Card A10 (793-9334-006), Schematic Diagram
Figure 27 (Sheet 1 of 2)

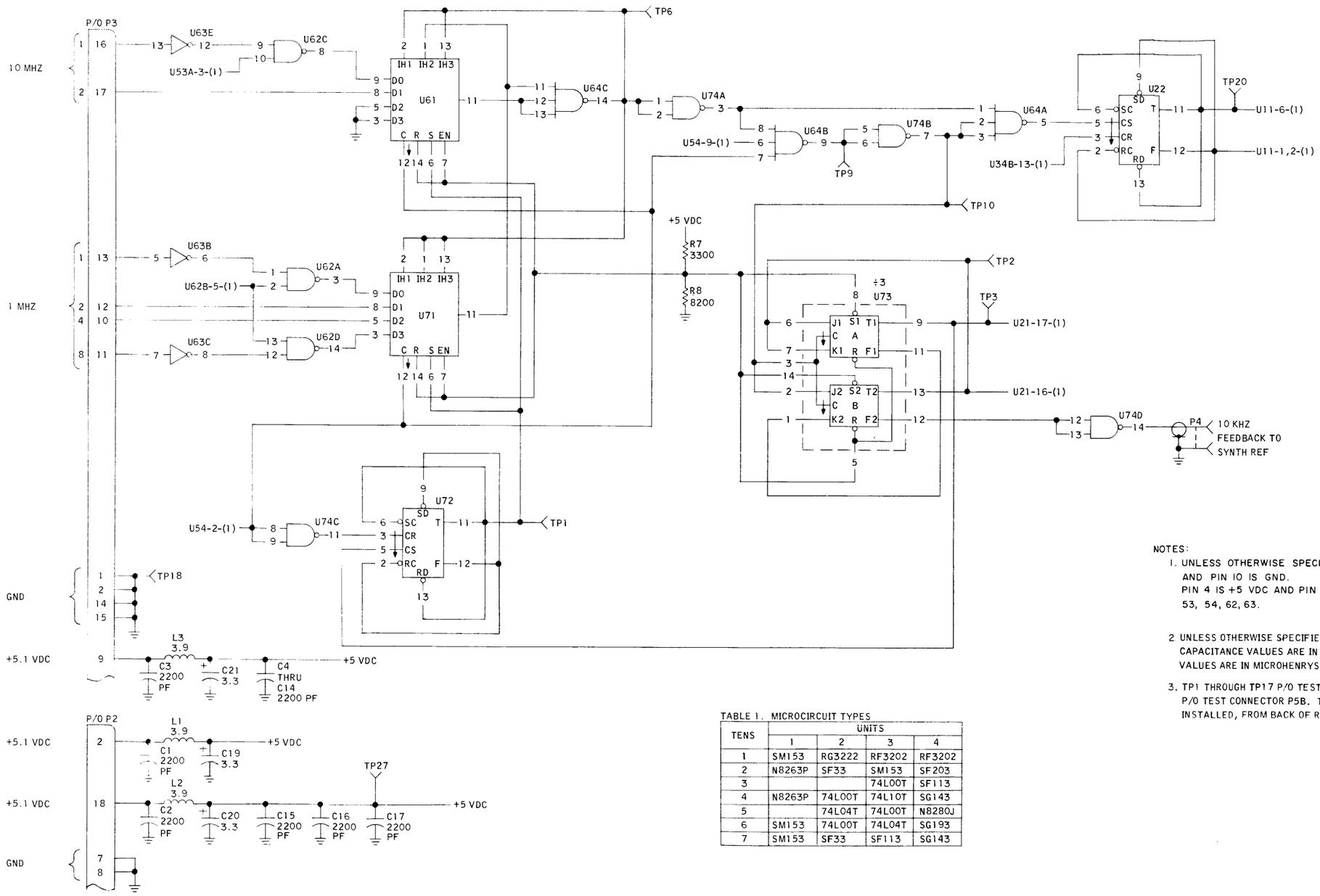


TABLE 1. MICROCIRCUIT TYPES

TENS	UNITS			
	1	2	3	4
1	SM153	RG3222	RF3202	RF3202
2	N8263P	SF33	SM153	SF203
3			74L00T	SF113
4	N8263P	74L00T	74L10T	SG143
5		74L04T	74L00T	N8280J
6	SM153	74L00T	74L04T	SG193
7	SM153	SF33	SF113	SG143

NOTES:

1. UNLESS OTHERWISE SPECIFIED, MICROCIRCUIT PIN 4 IS +5 VDC AND PIN 10 IS GND.
   PIN 4 IS +5 VDC AND PIN 11 IS GND ON: U21, 33, 41, 42, 43, 52, 53, 54, 62, 63.

2. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.

3. TP1 THROUGH TP17 P/O TEST CONNECTOR P5A; TP18 THROUGH TP27 P/O TEST CONNECTOR P5B. TEST POINTS ARE IDENTIFIED, WITH CARD INSTALLED, FROM BACK OF RADIO TOWARD THE FRONT PANEL.

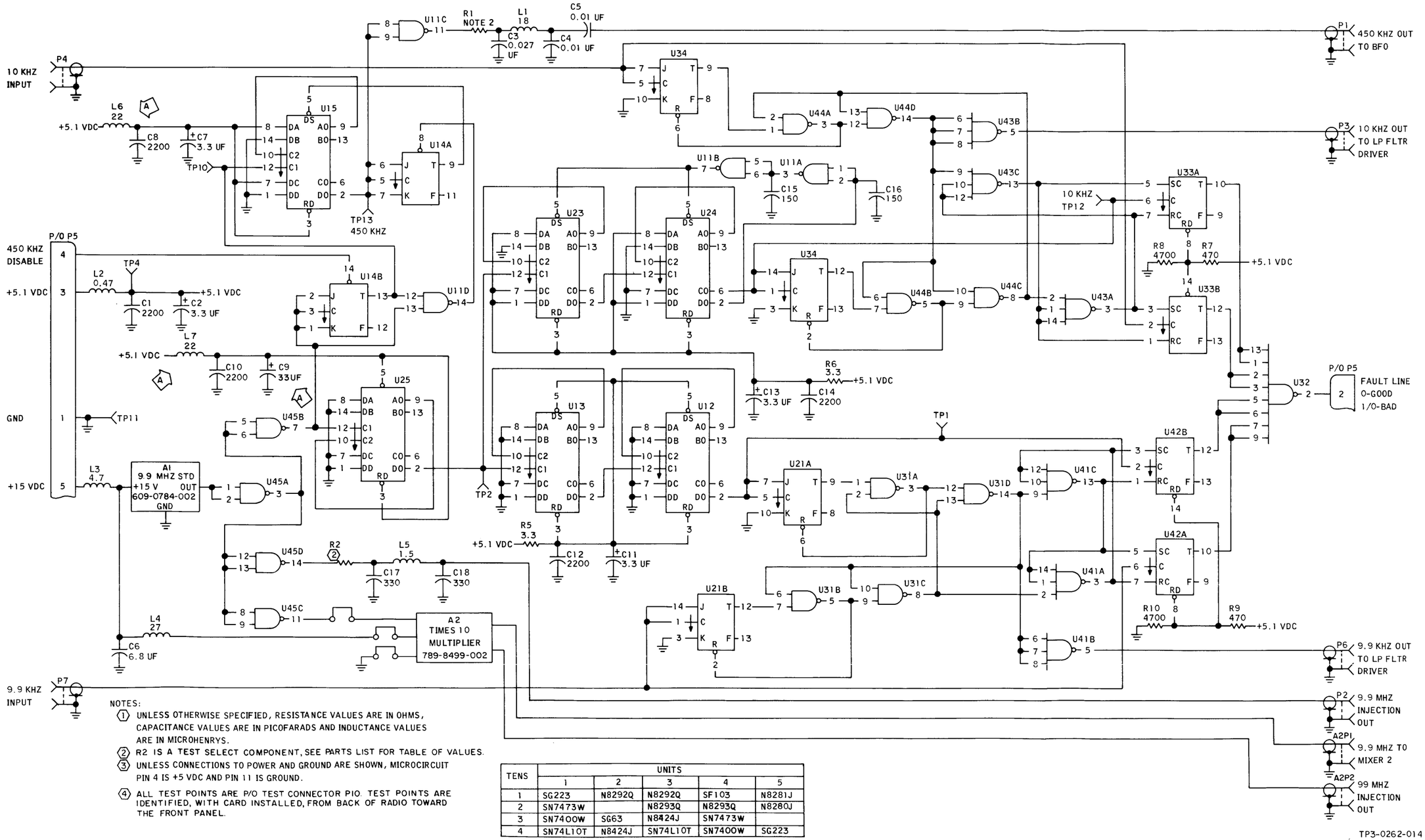
TP3-0263-024

VLF Synthesizer Divider Card A10 (793-9334-006), Schematic Diagram
Figure 27 (Sheet 2 of 2)

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	C9 changed to 33 μF. R3 and R4 deleted. L6 and L7 (22 micro-henrys) added. Provides improved filtering.	Number 1	72246

Synthesizer Reference Card A11 (793-9333-002), Schematic Diagram
Figure 28 (Sheet A)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN PICOFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. R2 IS A TEST SELECT COMPONENT, SEE PARTS LIST FOR TABLE OF VALUES.
3. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN 4 IS +5 VDC AND PIN 11 IS GROUND.
4. ALL TEST POINTS ARE P/O TEST CONNECTOR P10. TEST POINTS ARE IDENTIFIED, WITH CARD INSTALLED, FROM BACK OF RADIO TOWARD THE FRONT PANEL.

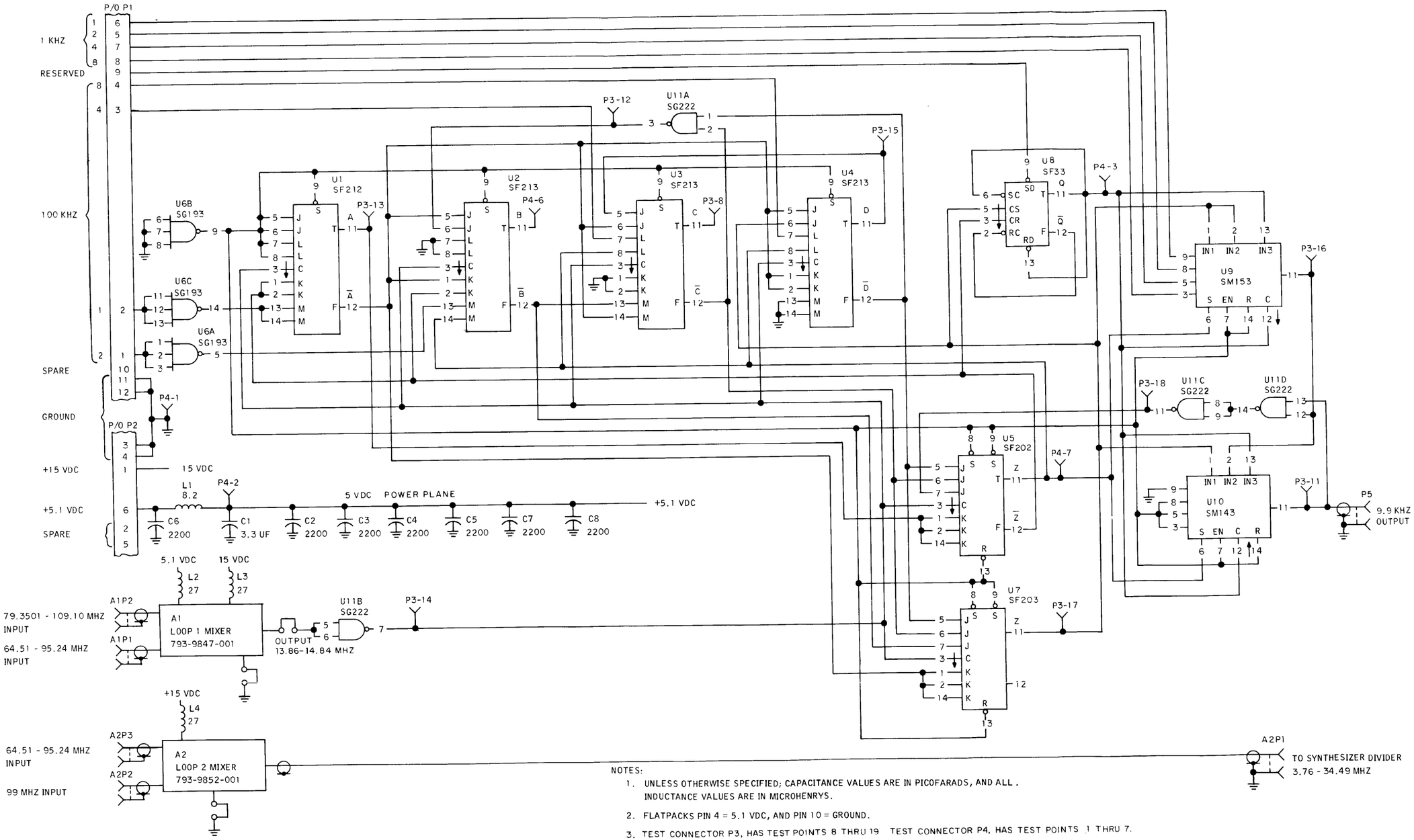
TENS	UNITS				
	1	2	3	4	5
1	SG223	N8292Q	N8292Q	SF103	N8281J
2	SN7473W		N8293Q	N8293Q	N8280J
3	SN7400W	SG63	N8424J	SN7473W	
4	SN74L10T	N8424J	SN74L10T	SN7400W	SG223

Synthesizer Reference Card A11 (793-9333-002),
Schematic Diagram
Figure 28

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY

Synthesizer Mixer Card A12 (793-9332-002), Schematic Diagram
Figure 29 (Sheet A)



NOTES:

1. UNLESS OTHERWISE SPECIFIED; CAPACITANCE VALUES ARE IN PICOFARADS, AND ALL INDUCTANCE VALUES ARE IN MICROHENRYS.
2. FLATPACKS PIN 4 = 5.1 VDC, AND PIN 10 = GROUND.
3. TEST CONNECTOR P3, HAS TEST POINTS 8 THRU 19 TEST CONNECTOR P4, HAS TEST POINTS 1 THRU 7. TEST POINTS ARE IDENTIFIED, WITH CARD INSTALLED FROM BACK OF RADIO TOWARD FRONT PANEL.

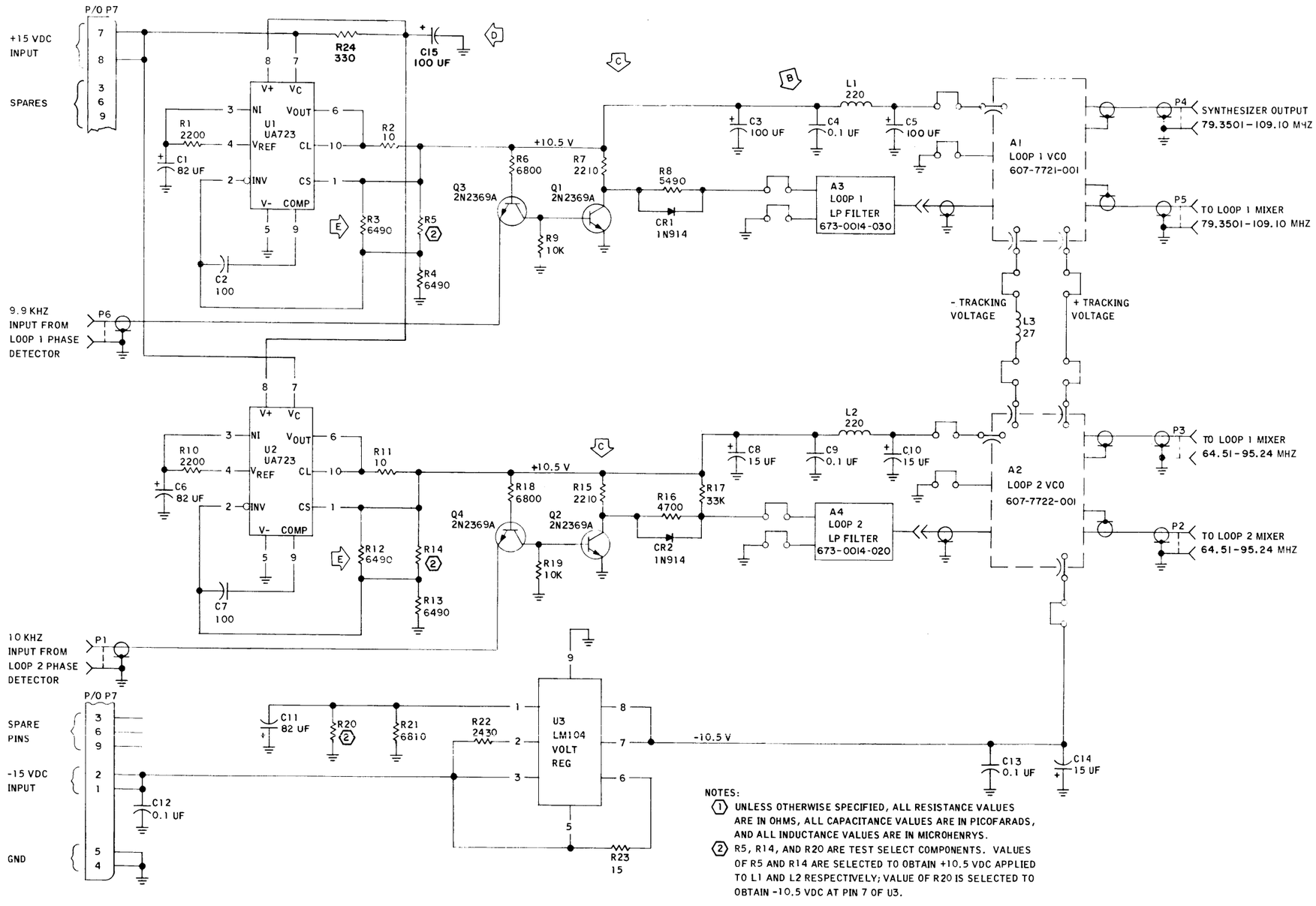
TP3-3491-014

Synthesizer Mixer Card A12 (793-9832-002), Schematic Diagram
Figure 29

SCHEMATIC CHANGES

REVISION IDENTIFICATION	DESCRIPTION OF REVISION AND REASON FOR CHANGE	SERVICE BULLETIN	EFFECTIVITY
A	Updated schematic to include sealed subassemblies part numbers.		All
B	C3 and C5 changed to 100 μF.		72246
C	R7 and R15 changed to 2.21 kΩ; R8 changed to 5.49 kΩ.		73126
D	Added C15 (100 μF) and R24 (330 ohms).		73236
E	R3 and R12 changed to 6.49 kΩ.		73253

Synthesizer VCO Card A13 (793-9331-003), Schematic Diagram
Figure 30 (Sheet A)



NOTES:

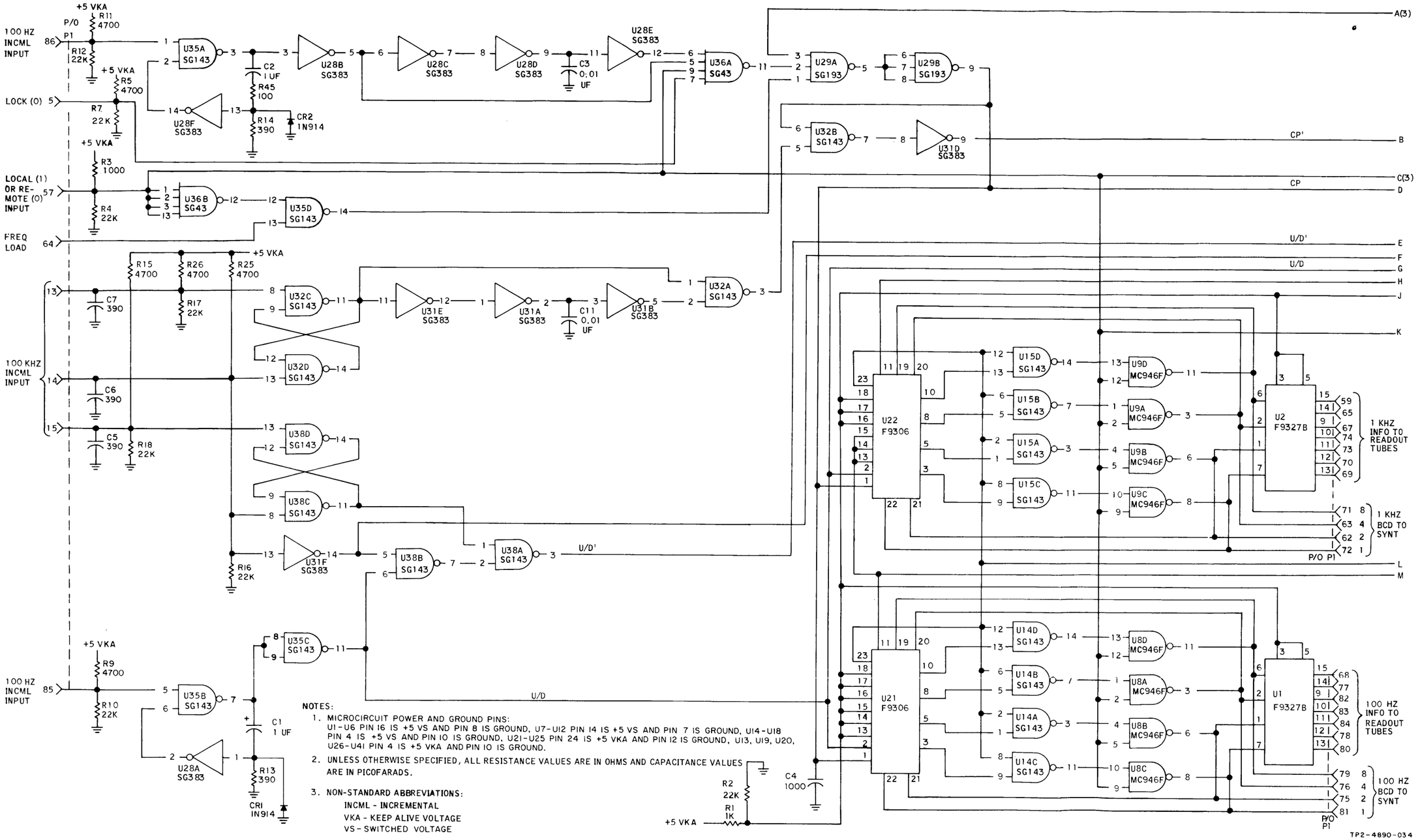
(1) UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN PICOFARADS, AND ALL INDUCTANCE VALUES ARE IN MICROHENRYS.

(2) R5, R14, AND R20 ARE TEST SELECT COMPONENTS. VALUES OF R5 AND R14 ARE SELECTED TO OBTAIN +10.5 VDC APPLIED TO L1 AND L2 RESPECTIVELY; VALUE OF R20 IS SELECTED TO OBTAIN -10.5 VDC AT PIN 7 OF U3.

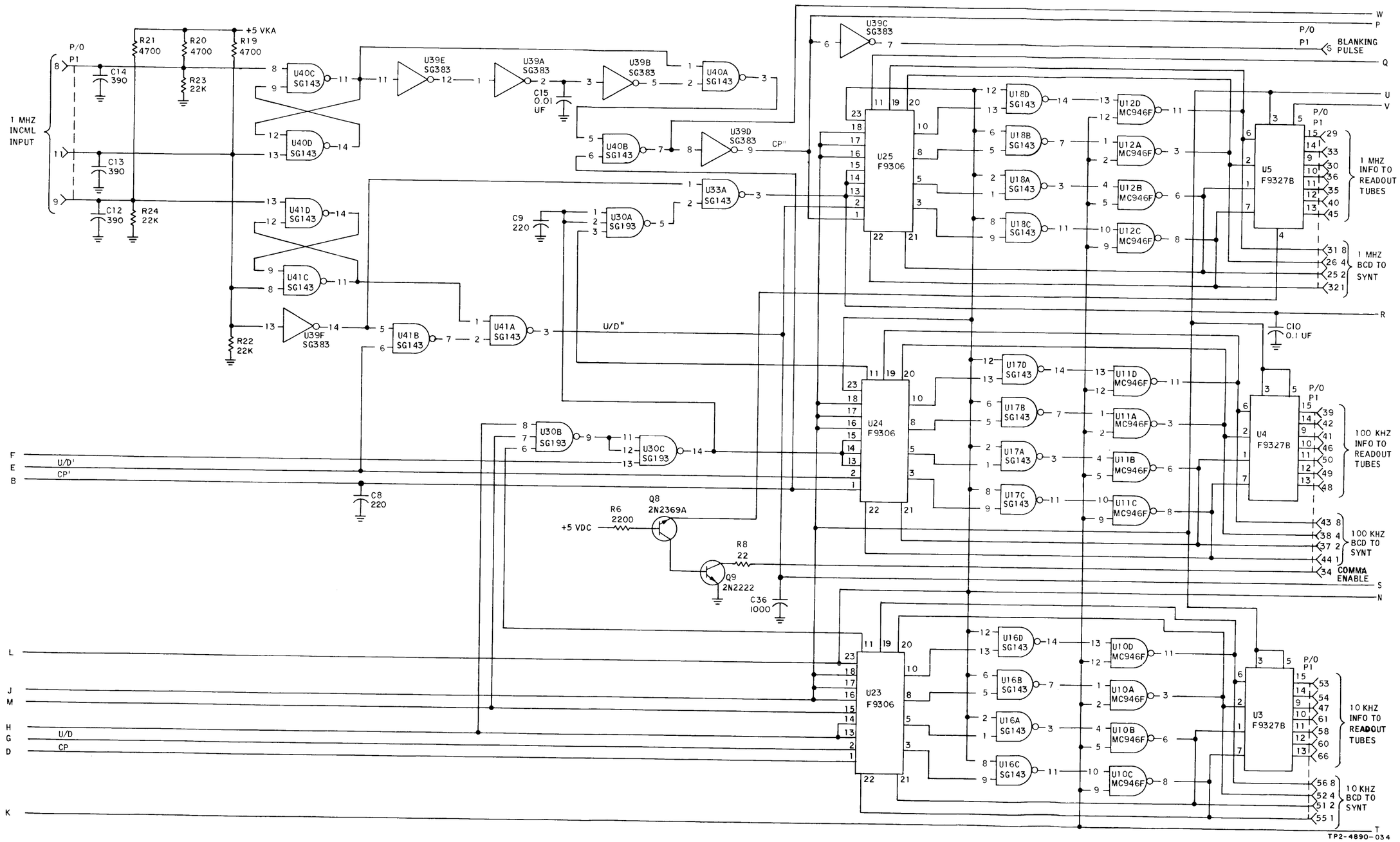
783-9500-002
TP3-0258-024

Synthesizer VCO Card A13 (793-9331-003), Schematic Diagram
Figure 30

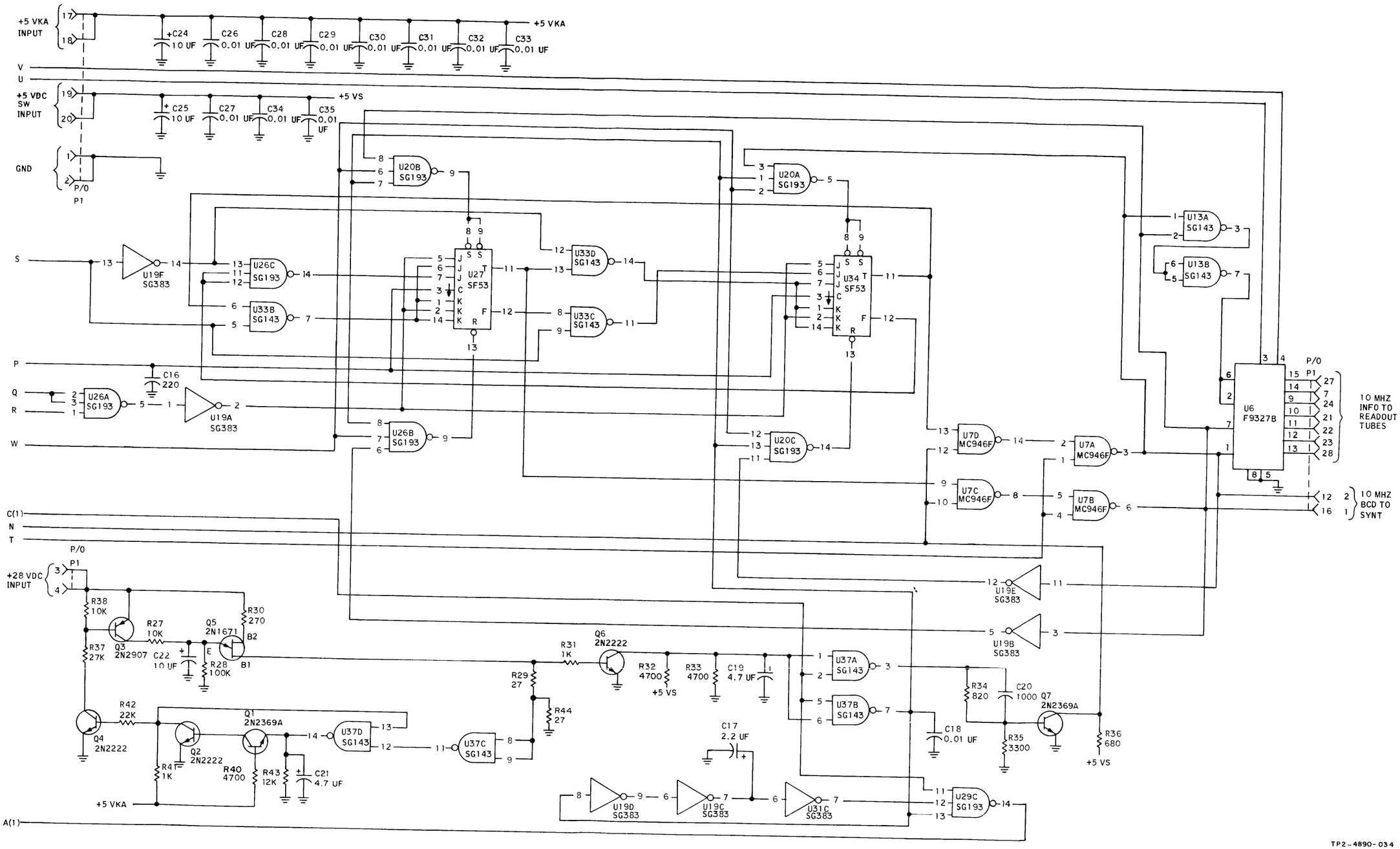
Revised 1 April 1973



Frequency Control Card A14 (783-9283-001), Schematic Diagram
Figure 31 (Sheet 1 of 3)



Frequency Control Card A14 (783-9283-001), Schematic Diagram
Figure 31 (Sheet 2 of 3)



Frequency Control Card A14 (783-9283-001), Schematic Diagram
Figure 31 (Sheet 3 of 3)

651S-1
GENERAL PURPOSE HF RECEIVER

PUB NO.	NOTE	DATE	SUBJECT
IB 1-72		03/01/72	Subassembly Interchangeability
SB 1		10/01/72	Reduction of 450-kHz Leakage From Synthesizer Reference Board A11
SB 2		06/06/73	Reduction of Noise Level
SB 3		07/15/73	Add Keep-Alive Frequency Memory Function
SB 4		07/15/73	Extend Comma and Decimal Lamp Life in Frequency Display
SB A		11/01/73	Change DCFE Filter Switching Diode
SB 5	1	12/15/74	Minimize TCU Circuit Card Response to Data Link Noise and Failure
SB 6	2	03/01/75	Reduce Intermodulation Level
SB 7		02/07/75	Reduce Internal Spurious Signals
SB 8		12/27/74	Allow Remote Control Operation With RS-232C Serial Control Interface Card A9
SB 9		02/15/75	Increase Life of Display Tubes
SB 10	2	12/31/75 Revised 08/02/76, 04/01/77	Replacing Display Tubes With LED Plug-in Assemblies
SB 11		Not issued	
SB B		11/15/74	KAV
SB C		01/15/78	Supply KAV Power to DCFE
SB 12		05/01/78 Revised 07/01/78	Replacing Nonprocurable Integrated Circuits
SB 13		10/01/80	Replace Nonprocurable Parts
SB 14		11/01/80	Reduce 100-kHz Sidebands
SB 15		05/01/81	Prevent Invalid Monitor Responses from the HF Receiver

NOTE:

1. Also applicable to 651S-1A.
2. Also applicable to 651S-1A and 651S-1B.

COLLINS

INFORMATION BULLETIN

COLLINS RADIO COMPANY

SUBJECT 651S-1 GENERAL PURPOSE HF RECEIVER, CPN 522-4836-002 THRU -015, AND -019, SUBASSY INTERCHANGEABILITY

DATE Mar 1/72

FROM LIGHTWEIGHT HF COMMUNICATIONS PRODUCT LINE

INFORMATION BULLETIN 1-72

The purpose of this information bulletin is to disseminate information on interchangeability of subassemblies used in subject radio. The attached table lists all subassemblies, Collins part number, and interchangeability.

When an order is received for a subassembly no longer in production, Collins will automatically substitute the latest subassembly that is interchangeable with the old one.

Subassembly Interchangeability

SUBASSEMBLY	COLLINS PART NO	REMARKS
Power supply Regulator card A1	778-2949-001	Only production part number (the last three digits of part no indicate the status of equipment/subassembly)
Audio card A2	778-2948-002, -003	Not interchangeable, production part number -002 includes squelch, -003 no squelch
ISB card A3	778-2952-001	Only production part number
If amplifier card A4	778-2951-001, -003	Not interchangeable, production part number -001 is standard, -003 allows fast reaction to AGC
Filter card A5A1	797-3571-001, -002, -003, -004	Not interchangeable, different bandwidth and/or frequency requirements
Filter card A5A2	797-3585-002, -003 -004, -005 -006, -007 -008, -009	Not interchangeable, different bandwidth and/or frequency requirements
Rf module A6	790-1048-003, -008, -009, -010	Production part numbers -003 and -008 are interchangeable with each other; -009 and -010 are not interchangeable
Decoder/driver card A7	778-2928-002, -003	Interchangeable

Subassembly Interchangeability (Cont)

SUBASSEMBLY	COLLINS PART NO	REMARKS
Interconnect card A8	778-2924-002, -003, -004, -005, -006	Not interchangeable
DCFE card A8	793-9402-001, -002	Not interchangeable
DCFE card A8	624-5744-001	Only production part number, not interchangeable with 793-9402-001, -002
DCU card A9	793-9414-001	Only production part number
TCU card A9	783-9480-001	Only production part number
SCAN card A9	783-9368-00	Only production part number
Synthesizer divider card A10	793-9334-001, -002, -006	Production part numbers -001 and -002 are interchangeable with each other; -006 is not interchangeable
Synthesizer reference card A11	793-9333-001, -002	Interchangeable
Synthesizer mixer card A12	793-9332-001, -002	Interchangeable
Synthesizer vco card A13	793-9331-002, -003	Interchangeable
Frequency control card A14	783-9283-001	Only production part number

COLLINS | SERVICE BULLETIN

1 November 1973

FROM: Telecommunications Group

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-004)
651S-1A GENERAL PURPOSE HF RECEIVER (622-1062-001)
DCFE CARD A8 (624-5744-001)

SERVICE BULLETIN A

SUBJECT: Change DCFE Filter Switching Diode

This modification is applicable to all DCFE cards supplied to the US Coast Guard under contract DOT-CG-23014A.

The purpose of this modification is to change the DCFE switching to allow proper operation of the receiver in the narrow shift radioteletypewriter (NSRT) bandwidth. The 10.35 MHz filters must be bypassed when the offset NSRT filter is used.

Future DCFE cards incorporating this change will be manufactured under Collins part number 624-5744-002.

Parts may be ordered at no charge from Collins Radio Company, Service Parts Department Cedar Rapids, Iowa 52406. The order should include the part number of the item and reference 651S-1 service bulletin A.

No special tools or equipment are required. Estimated time to perform this modification is 0.2 man-hour.

MODIFICATION PROCEDURE

a. Remove the DCFE card from the receiver.

b. Locate, note position of anode, unsolder and remove diode CR26. Discard old diode, as its leads are too short for new mounting. Refer to figure 2.

c. Install and solder the anode end of the new diode in the same position as the anode of the original diode. Refer to figure 1.

d. Slide sleeving on the cathode lead of the new diode. Wrap the lead on the cathode lead of diode CR34 and solder.

e. Mark circuit card "RWK-002" to indicate that it is electrically the same as the new part number 624-5744-002.

SERVICE BULLETIN A

MATERIAL INFORMATION

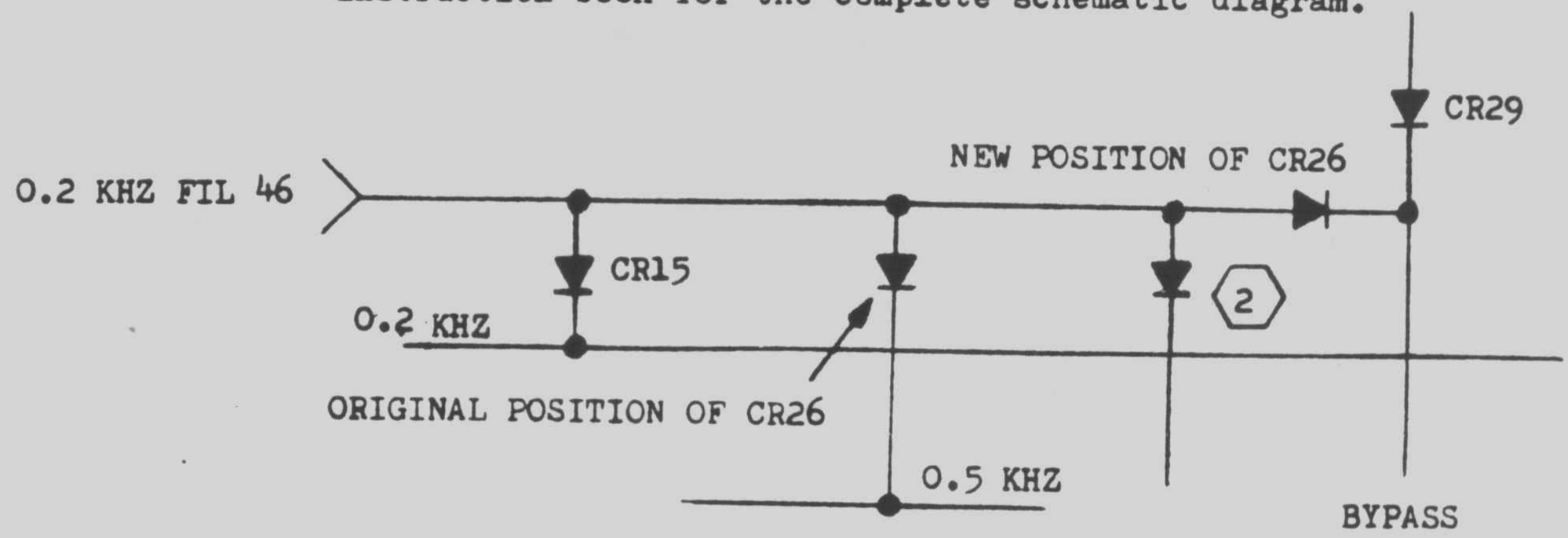
The following parts are required to perform this modification.

NEW COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION	REPLACED COLLINS PART NUMBER	INSTRUCTIONS DISPOSITION
353-0206-000	1		Diode 1N459	353-0206-000	discard
152-2483-000	0.1 ft		Sleeving	-	-

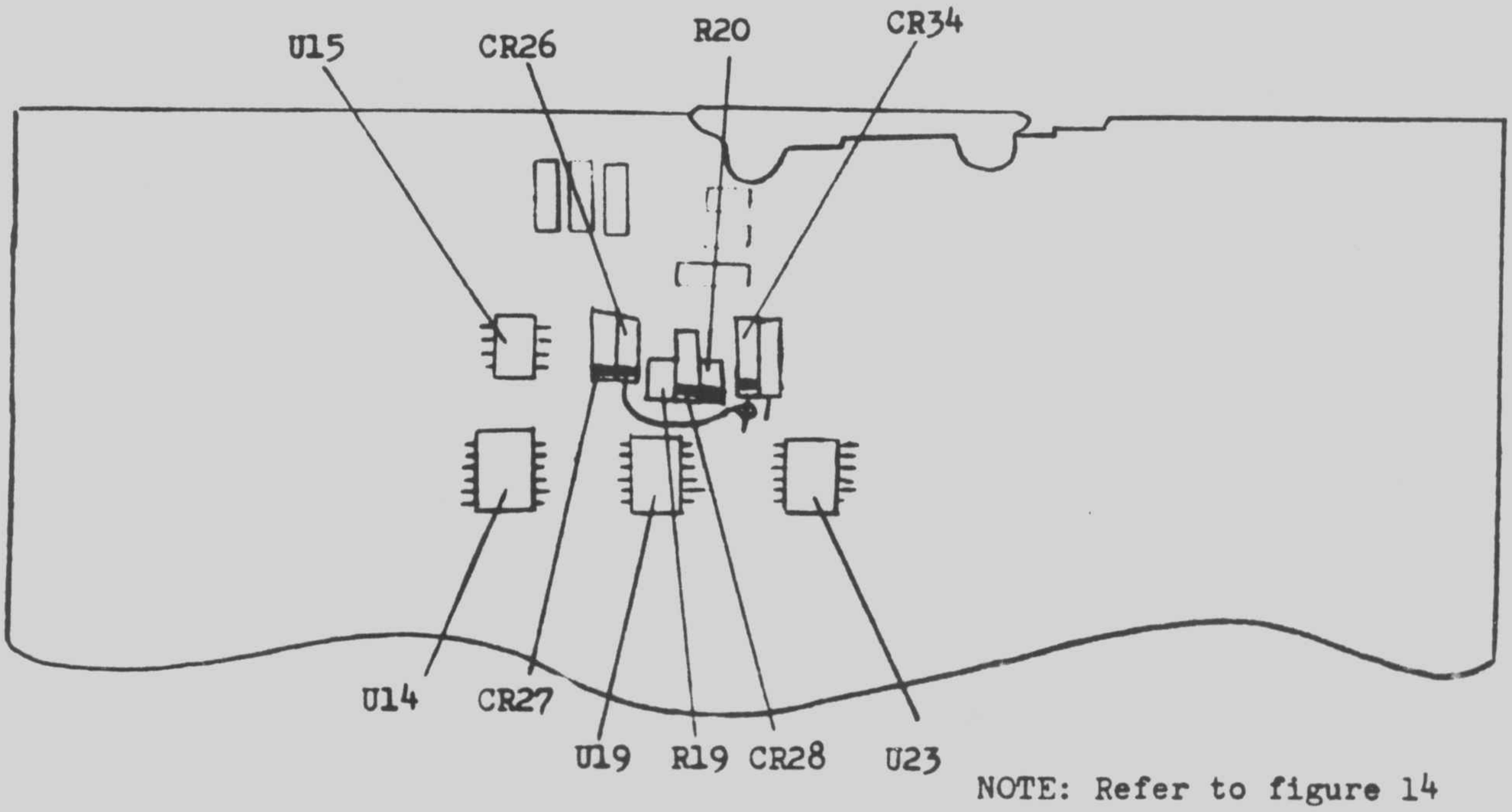
SERVICE BULLETIN

SERVICE BULLETIN A

NOTE: Refer to figure 20 of the diagrams section in the 651S-1/1A instruction book for the complete schematic diagram.



Partial Schematic Diagram of the DCFE Card
Figure 1



NOTE: Refer to figure 14 of the parts list section of the 651S-1/1A instruction book for complete parts location.

Location of CR26
Figure 2

COLLINS | SERVICE BULLETII

K. L. Roland 137-138

15 November 1974

FROM: Telecommunications Equipment Group Product Management

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-199)
TELETYPEWRITER CONVERTER UNIT (TCU)
CIRCUIT CARD A9 (783-9480-001, -002)

SERVICE BULLETIN B

SUBJECT: Frequency keep-alive operation with TCU

This modification is applicable to 651S-1 receivers (522-4836-199) containing both the frequency keep-alive and TCU remote control options. This bulletin will not be incorporated into production units.

The purpose of this modification is to permit operation of the TCU logic from the 5-Vdc keep-alive supply.

The keep-alive option does not normally work when the TCU is used because the TCU logic gives false frequency change pulses when it loses power in local operation mode. This change prevents such pulses. The problem does not exist when the remote control is in operation because the receiver frequency may be retransmitted immediately by the 514S-1 control.

Interchangeability is affected as follows. A modified TCU will not operate in an unmodified receiver chassis. A DCU remote control card A9 (793-9414-001) will be damaged if plugged into a modified receiver. After modification, the current drain from the external keep-alive battery will increase from 0.8 to 1.4 amperes.

Estimated time to perform this modification is 2 man-hours.

The modification parts (as listed in the material information paragraph) are available for shipment within 30 days after receipt of order at a price of $2.53 (price is subject to change without notice; minimum order price is $25.00). Parts may be ordered from Collins Radio Group, Service Parts Department, Cedar Rapids, Iowa 52406. All orders should specify part numbers and reference 651S-1 service bulletin B.

No special tools or equipment are required.

Refer to parts list section of the 651S-1/1A General Purpose HF Receiver Instruction Book for assistance in locating parts.

This modification will not be incorporated into the 651S-1/1A instruction book.

SERVICE BULLETIN B

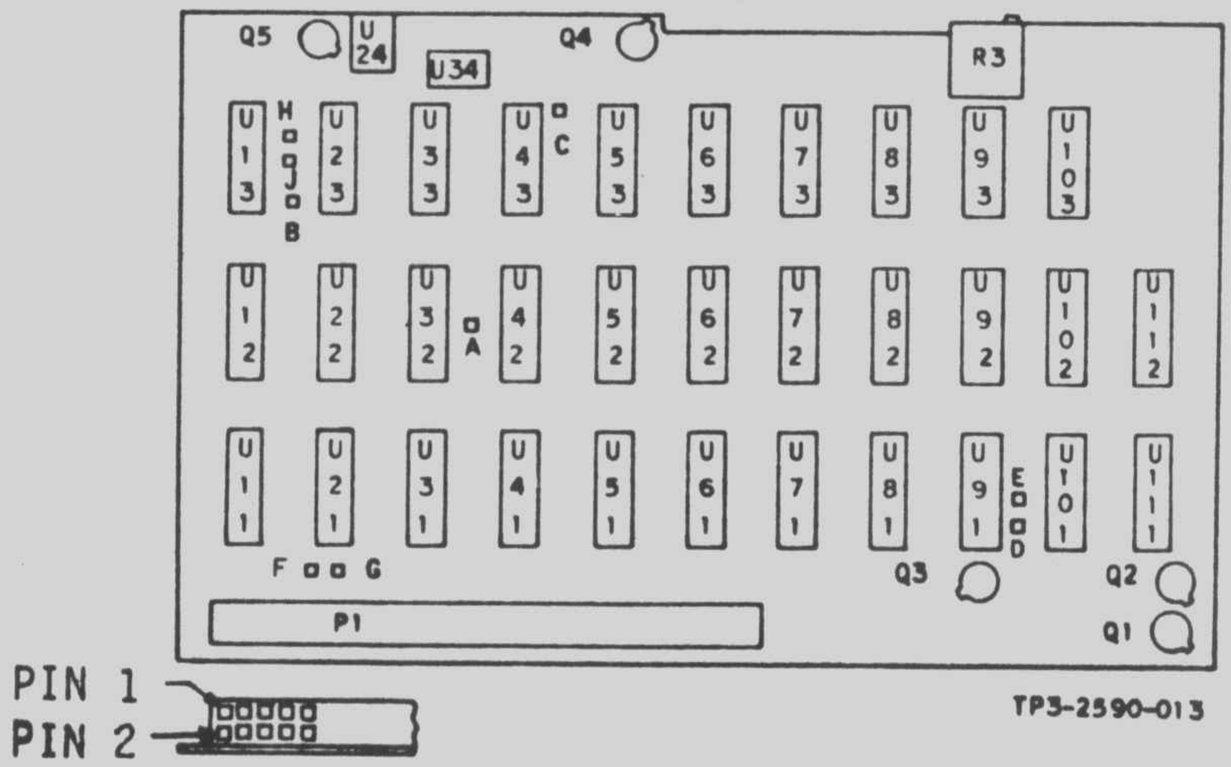
MODIFICATION PROCEDURE

a. Remove the dust cover by removing two retaining screws at the rear and sliding the cover from the unit.
b. Remove the screws and the cover from the top left module compartment.
c. Remove TCU card A9 from the receiver.
d. Remove connector sockets 35 and 36 from connector shell and card as follows: (figure 1):
   1. On the back of the card, suck the solder from the holes occupied by sockets 35 and 36.
   2. Using a scribe, or a similar tool, carefully remove the contacts from the holes and slide the contacts out of the blue-line connector.
e. On the back of the card, solder one end of a jumper (428-4821-000) in the hole where socket 35 was located.
f. Wrap and solder the other end of the jumper around the contact lead of socket 22.
g. Mark "SB B" on the TCU card near the part number.
h. On the bottom of the 651S-1 chassis sideboard, connect a jumper (428-4821-000) from J1-17 (mates with A14 connector) to J30-22 (mates with A9 connector). Refer to figure 2.
i. On keep-alive voltage regulator circuit assembly TB501, remove diodes CR501 and CR502. Refer to the 651S-1/1A instruction book (part 2) parts list, figure 27, for parts location.
j. Install new diodes CR501 and CR502 (353-3718-040) in the spaces where the old diodes were located and with the same orientation as the old diodes.
k. Mark information chart (280-3778-010) with "SB B" and apply to chassis near name-plate.
l. Reassemble receiver in the reverse of steps a, b, and c check for proper operation.

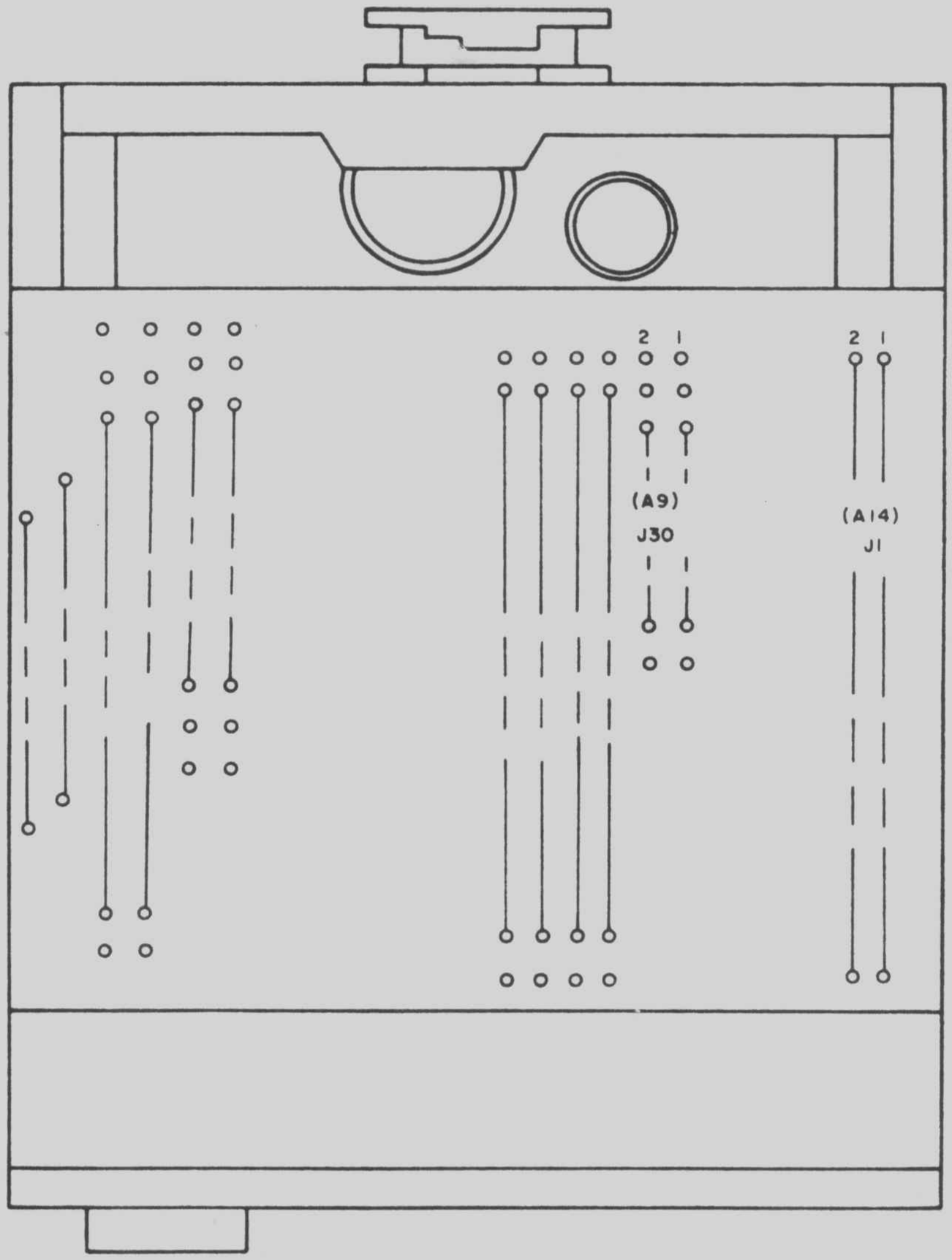
MATERIAL INFORMATION

The following parts are required to modify one 651S-1.

COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
280-3778-010	1	$0.30	Chart, information
353-3718-040	2	1.11	Diode, 1N5550
428-4821-000	0.5 ft	0.01	Wire, bus, #28



TCU Circuit Card A9
Figure 1



651S-1 Sideboard, Bottom View, Connector Locations
Figure 2

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-XXX)

DEVICE CONTROL FUNCTIONAL ELEMENT (DCFE)

CIRCUIT CARD AS (624-5744-001)

SERVICE BULLETIN C

SUPPLY KAV POWER TO DCFE

This service bulletin is applicable to 651S-1 units in certain installations that require keep-alive power for the DCFE card. 651S-1 Service Bulletin B must be installed prior to installing this bulletin. Interchangeability is affected as follows: A modified DCFE card will not operate in an unmodified chassis. A modified chassis will accept either modified or unmodified DCFE cards. A DCU card must not be used in a modified chassis as noted in 651S-1 Service Bulletin B.

This service bulletin will not be incorporated into production units.

The purpose of this modification is to allow the DCFE card to operate on 5-volt power from the keep-alive power bus in the receiver. This permits retention of mode information during power interruptions.

This modification consists of inspecting and possibly replacing one resistor and rerouting 5-volt power to the DCFE circuit card.

The modification parts are itemized in the material information paragraph. Contact Collins Groups/Rockwell International, Service Parts Department, Cedar Rapids, Iowa 52406, for price and availability of parts.

Estimated time required is 1 man-hour.

No special tools or equipment are required.

This service bulletin references the 651S-1 General Purpose HF Receiver Instruction Book, Collins part number (CPN) 523-0764052.

This bulletin will not be incorporated into the instruction book.

MODIFICATION PROCEDURE

NOTE: Refer to the 651S-1 instruction book maintenance section, CPN 523-0764056, for disassembly/assembly procedures.

A. Remove all power to the receiver.

B. Remove the DCFE circuit card A8, CPN 624-5744-001, from the receiver.

C. Disconnect +5-volt power by removing contact P1-27 from the blue line connector on the card. Refer to figure 1.

D. On the back of the card, connect a #26 insulated bus wire (422-4008-000) from the vacated hole at P1-27 to spare contact P1-48.

E. Mark "KAV OPERATION" near the part number on the card.

F. On the receiver sideboard, connect a #26 insulated bus wire (422-4008-000) from XA8-48 to XA9-22 to provide keep-alive power to A8. Refer to figure 2.

G. Reinstall DCFE card in receiver.

NOTE: Refer to 651S-1 instruction book parts list section, CPN 523-0764057, for parts location in steps H and I. Figure and item numbers are in parentheses.

H. Inspect the wire from TB106-1 (40-64) to power switch S104 (39-30). If the wire is #26 copperweld, replace it with #22 red stranded (439-4032-000).

I. Inspect resistor R506 (27-1) on the keep-alive regulator assembly. If it is not 1800 ohms, replace it with an 1800 ohm resistor (745-0758-000).

J. Reassemble the receiver.

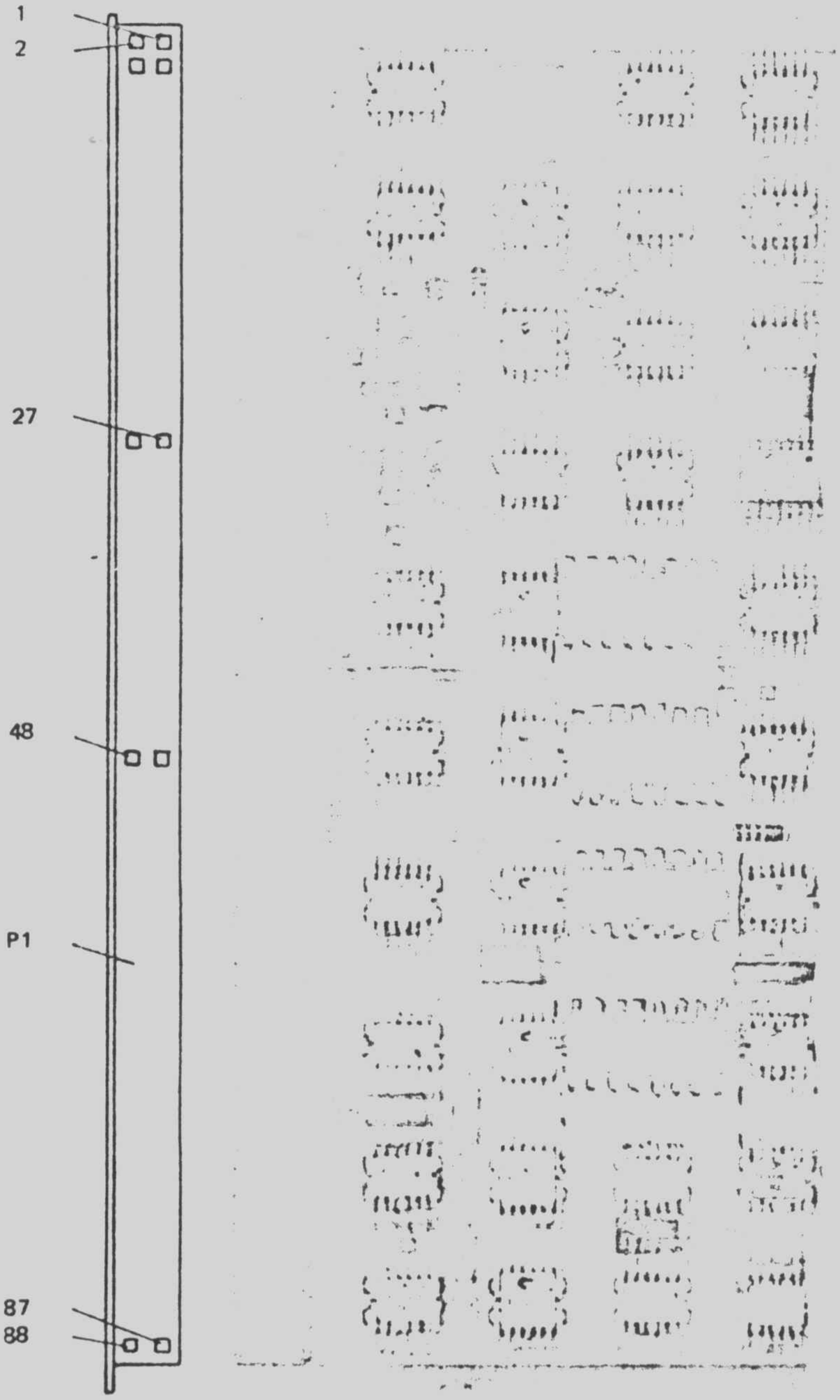
K. Mark SB C on the information chart.

L. Perform the simple test in the front of the 651S-1 instruction book maintenance section to ensure that the receiver is operating satisfactorily.

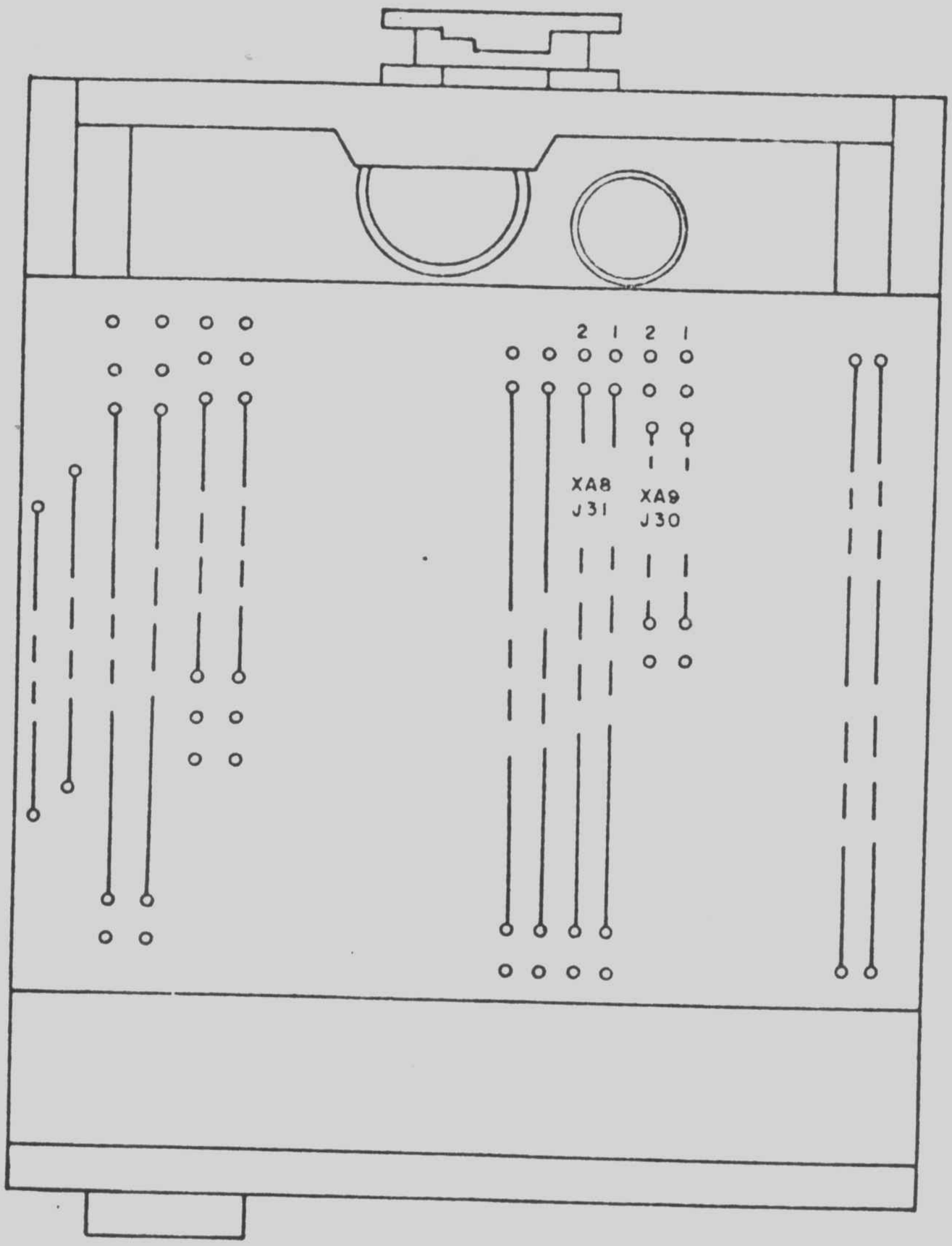
MATERIAL INFORMATION

The parts listed below are required to modify one 651S-1.

COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
422-4008-000	305 mm (1 ft)		Wire, bus, insulated, #26 AWG
439-4032-000	1830 mm (6 ft)		Wire, stranded, red, #22 AWG
745-0758-000	1		Resistor, 1800 ohms, R506



P/O DC FE Circuit Card A8, Connector Pin Locations
Figure 1



651S-1 Sideboard, Bottom View, Connector Locations
Figure 2

Collins
Rockwell International

SERVICE BULLETIN

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-XXX)
651S-1A GENERAL PURPOSE HF RECEIVER (622-1062-001)
651S-1B GENERAL PURPOSE HF RECEIVER (622-1165-XXX)
INDICATOR HOUSING ASSEMBLY (606-9707-002)

SERVICE BULLETIN NO 10

REPLACING DISPLAY TUBES WITH LED PLUG-IN ASSEMBLIES

This modification is applicable to all 651S-1/1 ( ) General Purpose HF Receivers with serial number 5000 and below.

Production cut-in: None. A single display board will replace the individual display tubes in production units serial number 5000 and above.

The purpose of this modification is to replace the display tubes in the 651S-1 with plug-in LED assemblies.

This modification consists of replacing the six display tubes with plug-in LED assemblies, replacing six current limiting resistors with jumper wires, removing the comma and decimal point assemblies, and moving the location for a meter mounting screw.

INTERCHANGEABILITY INFORMATION

A brief description of display configurations for the 651S-1/1A is as follows:

651S-1/1( ) SERIAL NUMBER	DISPLAY	FREQUENCY CONTROL CARD A14
5000 and below	Tube	783-9283-001 or 601-3363-001
5000 and below SB No 10 installed	LED Plug-In Assembly	783-9283-001 or 601-3363-001
5001 and above	LED Board	601-3363-002

CAUTION: A DISPLAY TUBE WILL BE RUINED IF IT IS INSERTED IN A 651S-1/1( ) MODIFIED BY SB NO 10.

An LED plug-in assembly will not operate in a 651S-1/1( ) with serial number 5000 and above or one that isn't modified by SB No 10. An incorrect Frequency Control Card A14 will cause the frequency display to operate incorrectly.

Frequency Control Cards A14, 601-3363-001 and 601-3363-002 use the same printed circuit board. Both cards provide the "keep alive" function. One card status may be converted to the other card status by changing the display driver components (integrated circuits), handle, and card markings as follows:

COMPONENT	601-3363-001	601-3363-002
U26, U28, U30, U32, U34, U36, U38	Use SN 7406 (351-7632-010)	Use SN 7407 (351-7633-010)
Handle	CPN 601-3538-001	CPN 635-0703-001

Estimated time to perform this modification is 1 man-hour.

Modification kit, Collins part number 635-4887-001 (as itemized in the material information paragraph), is required to perform the subject modification. Contact Collins Radio Group/Rockwell International, Finished Goods Department, Cedar Rapids, Iowa 52406 for price and availability. All requests should specify the kit part number and reference 651S-1 Service Bulletin No 10.

No special tools or equipment required.

The next revision to the diagrams section (523-0764058) and the parts list section (523-0764057) of the 651S-1/1(1A) General Purpose HF Receiver Instruction Book (523-0764052) will cover the changes included in this bulletin.

MODIFICATION PROCEDURE

A. Disconnect all external cables and wiring. Remove two screws from rear of unit and slide cover from the unit.

CAUTION: SUPPORT CENTER OF THE CHASSIS AND FRONT PANEL WHILE REMOVING SCREWS IN STEP B.

NOTE: Refer to figures in the parts list section (523-0764057) of the 651S-1/1( ) Instruction Book (523-0764052, Part 2) for the location of components in the following procedures.

B. Remove four screws on each of the two tie (side) plates (39, PL figure 1) that hold the front panel assembly to the main chassis. Carefully swing the front panel from the main chassis and lay the unit on its left side.

C. Remove the six display tubes (25, 26, 27, 28, 29, 30, PL figure 1).

D. Remove all knobs from the front panel.

E. Remove marking plate (38, PL figure 1) by removing the three nuts at rear of front panel assembly.

F. Release tuning switch S109 (17, PL figure 39) by removing four screws from the face of the front panel and carefully position to the side.

G. Drill a new 0.125-inch hole 0.25 inch to the right of the original screw on the bracket (3, PL figure 39) through the bracket and indicator housing (73, PL figure 39). Remove the screw and pressed-in nut from the bracket.

H. Remove the upper screw and loosen the lower screw from the nut strip (136, PL figure 39). Swing the nut strip away from the meter assembly.

I. From the face of the front panel, remove the six mounting screws from the indicator housing (73, PL figure 39) and the two screws from the meter bracket (13, PL figure 39). Carefully pull the indicator housing and meter assembly away from the front panel.

J. Unsolder and remove the six resistors R172, R164, R156, R148, R140, and R132 (108, 112, 116, 120, 124, 127, PL figure 39).

K. Install a bus wire (428-4824-000) in the locations where the six resistors were removed (pin 6 of the tube sockets).

L. Unsolder the wires connected to lamp blocks DS104 and DS105 (76 and 78, PL figure 39) and remove the lamp blocks. Wires removed from the same terminal must remain connected to each other. Tape the ends of the wires.

M. Insert the LED plug-in, with decimal point (635-4586-001), in the fourth tube socket from the right (V104) as viewed from the front.

N. Insert the five LED plug-ins (635-4586-002) in the remaining tube sockets.

O. Replace the indicator housing (73, PL figure 39) in the front panel assembly and secure with the six mounting screws. Apply caution label (637-1743-001) to indicator housing.

P. Mount bracket assembly (3, PL figure 39) with the meter in place, and attach to the indicator housing, using new hole with screw (343-0133-000), lockwasher (310-0279-000), and nut (313-0132-000). Secure the nut strip (136, PL figure 39) to the front panel assembly with the two screws removed in step H.

Q. Mount tuning switch S109 (17, PL figure 39) on chassis and secure with four screws.

R. Place marking plate (38, PL figure 1) in front panel assembly and secure with the three nuts.

S. Replace all knobs on the front panel.

T. Perform the following procedures if the unit is modified by 651S-1/1A Service Bulletin No 9.

(1) Refer to figure 1. Unsolder blue wire connected on one standoff terminal on TB103 and connect and solder to J56-4.

(2) Unsolder and discard the 3.3-ohm resistor.

U. Mount the front panel assembly to the main chassis and secure with four screws on each of the two tie (side) plates (39, PL figure 1).

V. Mark information chart with SB 10.

W. Slide cover back on unit and replace two screws on rear of unit.

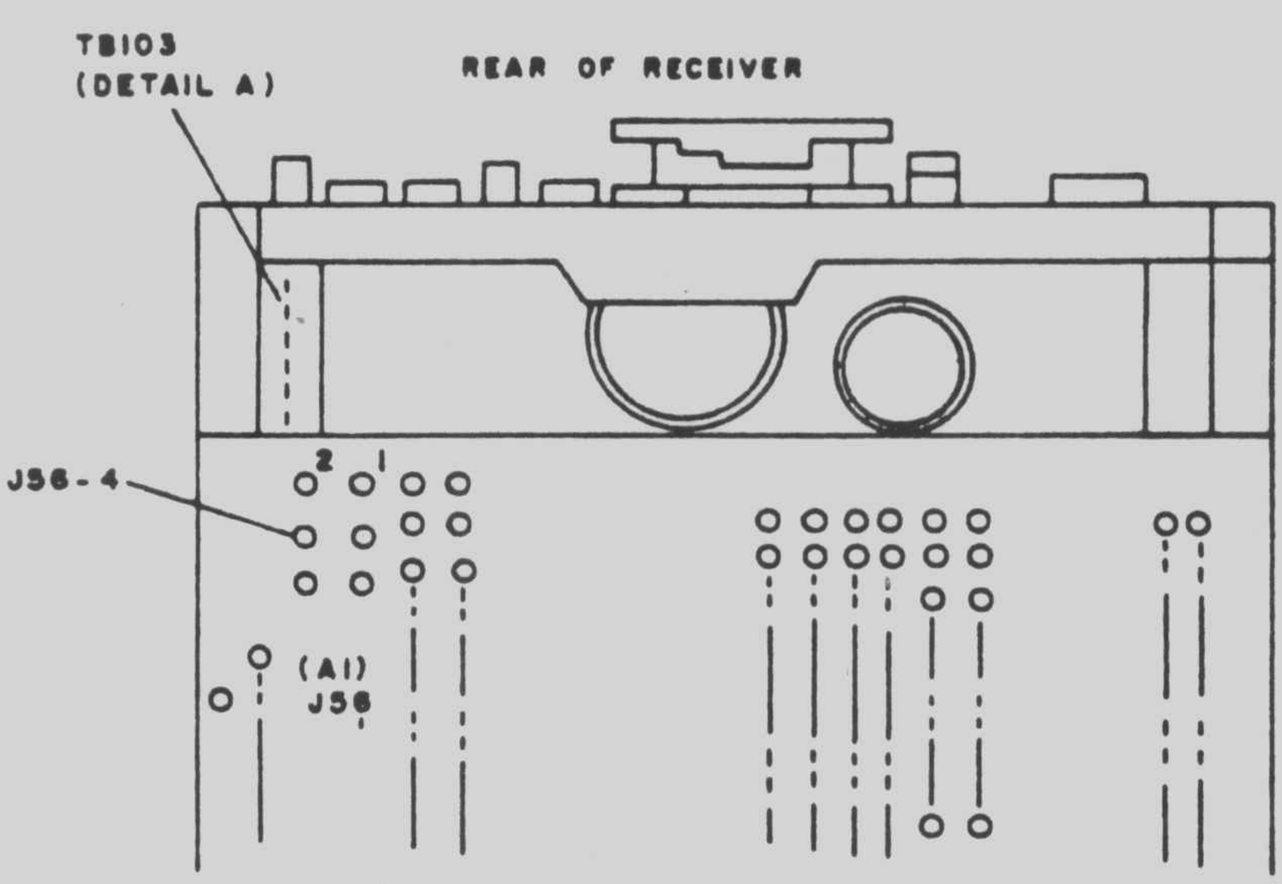
X. Reconnect external cables and wires and check that display lights properly.

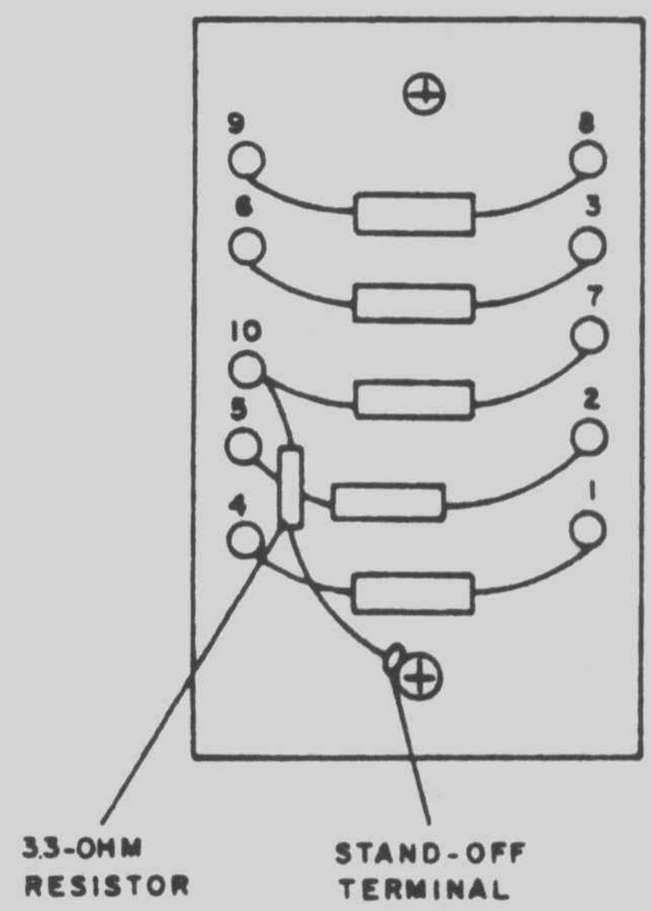
NOTE: Schematic modifications are shown in figure 2. Figure 3 is the schematic for the LED plug-in assembly.

MATERIAL INFORMATION

Modification kit 635-4887-001 is required to modify one 651S-1/1( ) and is itemized below.

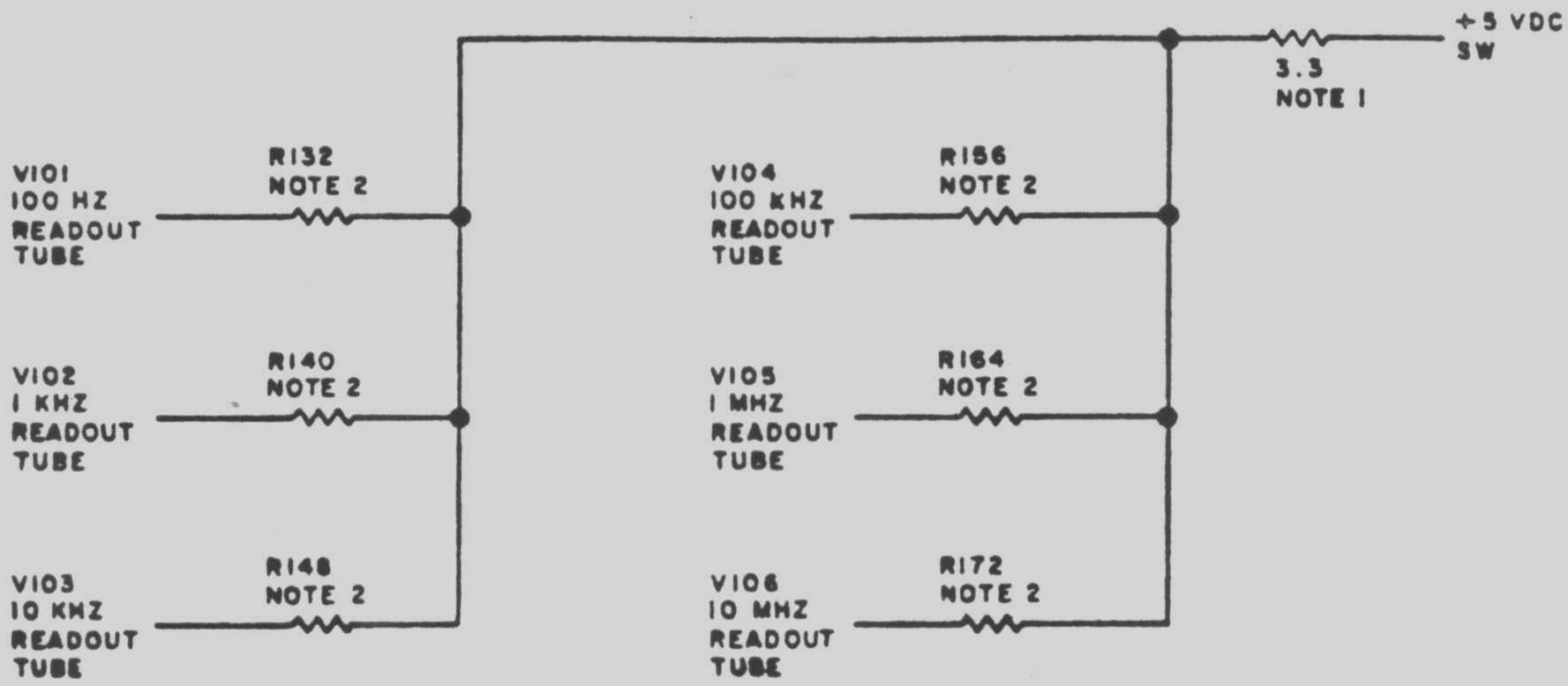
COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
310-0279-000	1		Washer, split lock
313-0132-000	1		Nut, 4-40 hex
343-0133-000	1		Screw, 4-40 x 0.25
428-4824-000	305 mm (1 ft.)		Wire, AWG #22
635-4856-001	1		LED plug-in assembly (with decimal point) DS104
635-4856-002	5		LED plug-in assembly (without decimal point) DS101, DS102, DS103, DS105, DS106.
637-1743-001	1		Label, caution
280-3778-010	1		Chart, information

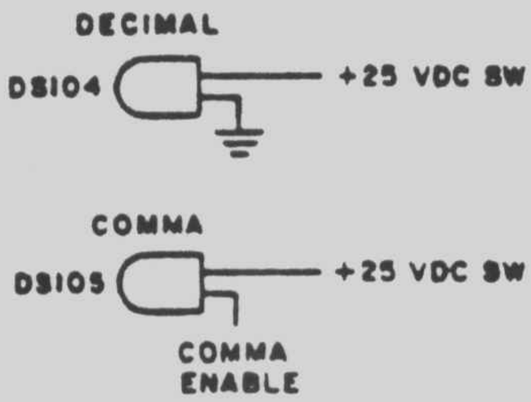




DETAIL A (TB103)

651S-1/1 ( ) Chassis, Partial Bottom View
Figure 1

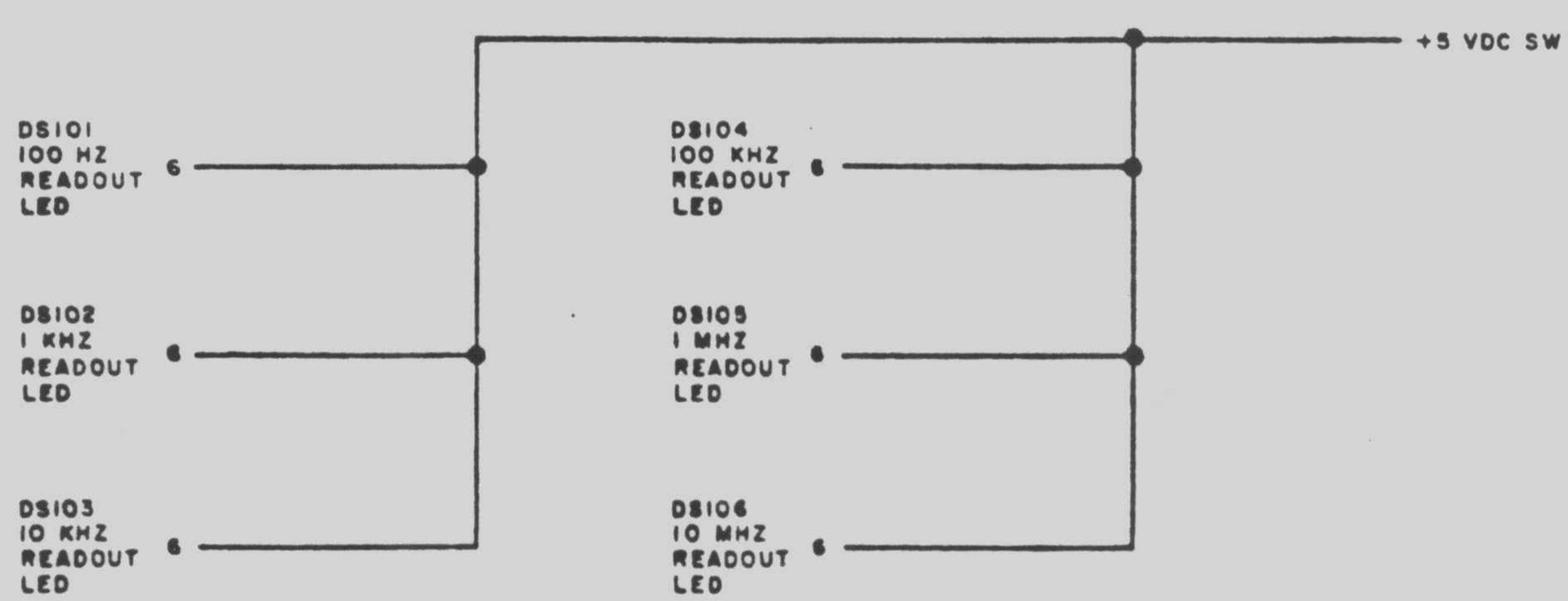




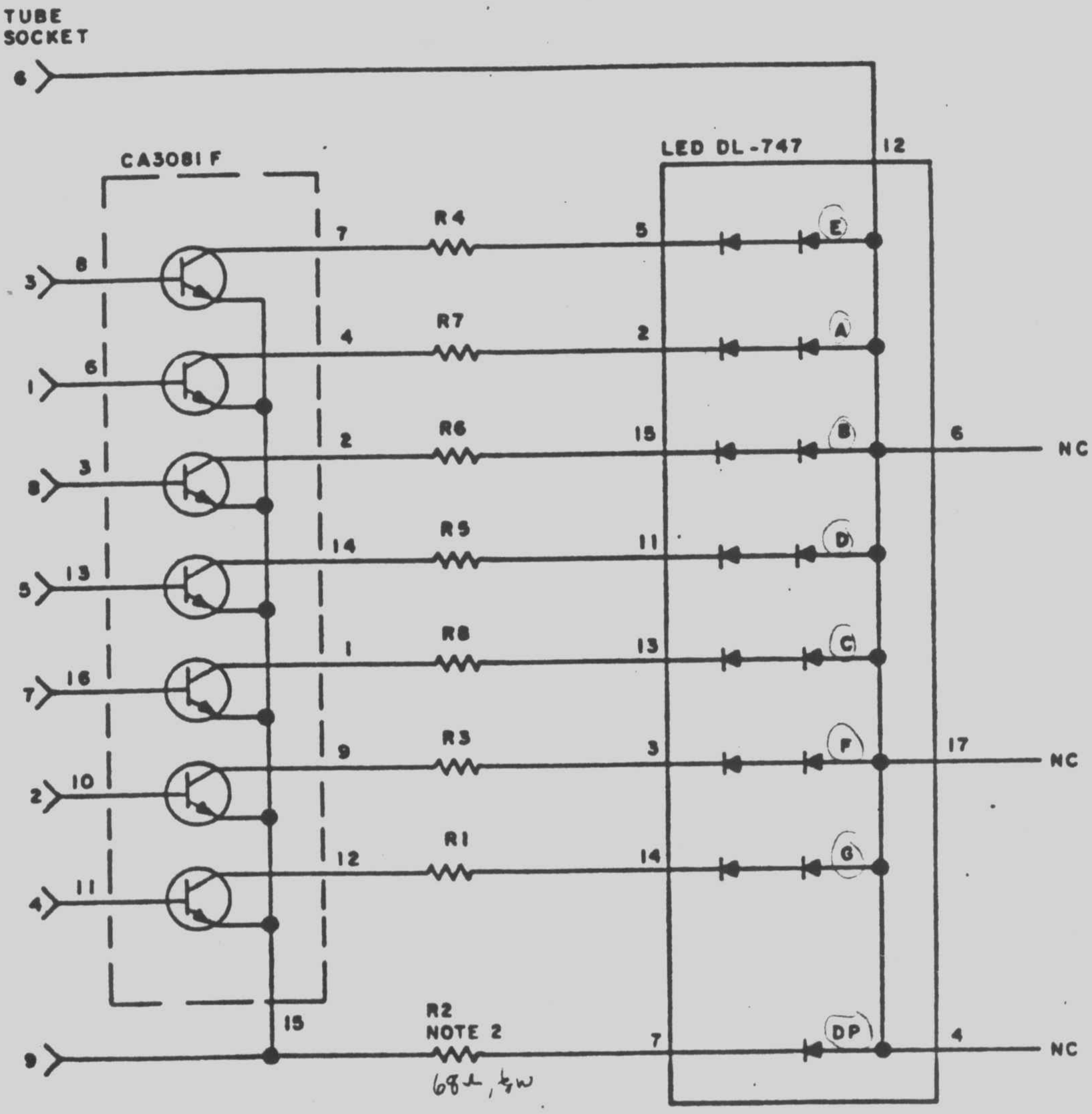
NOTES:

1. THE 3.3-OHMS RESISTOR IS ONLY ON UNITS WITH SB 9
2. R132, R140, R148, R156, R164 AND R172 ON INDICATOR HOUSING ASSEMBLY ARE:
   82 OHMS BEFORE REV G;
   100 OHMS REV G AND ABOVE.

BEFORE

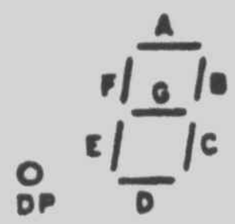


AFTER



NOTES:

1. ALL RESISTORS ARE 68 OHM, 1/8 WATT
2. RESISTOR R2 IS NOT PART OF THE 636-4856-002 LED PLUG-IN ASSEMBLY
3. SEGMENT DESIGNATIONS ARE:



April 1, 1977

REVISION 2
TO
651S-1/1A/1B SERVICE BULLETIN NO 10

Attached is a revised issue of 651S-1/1A/1B Service Bulletin No 10 titled, "Replacing Display Tubes with LED Plug-in Assemblies," dated 31 December 1975 and revised 2 August 1976.

This revision consists of the following changes:

1. Page 1: last paragraph was expanded for clarification.
2. Page 2. paragraph F; added "from the face of the front panel."
3. Page 3; paragraphs H and I were rewritten for clarification.
4. Page 3. paragraph K; corrected part number 439-4000-000 to 428-4824-000.
5. Page 3; paragraph P was expanded for clarification.
6. Page 4, parts list; corrected part number 439-4000-000 to 428-4824-000.
7. Page 4, parts list; added 280-3778-010, quantity 1, information chart.
8. Page 5; figure 1 revised for clarification.

Black bars in the margin indicate where changes were made. This revised issue replaces the entire original publication.

Collins Divisions
Cedar Rapids, Iowa 52406
(319) 395-1000
Cable COLINRAD Cedar Rapids

Rockwell International

July 1, 1978

REVISION 1
TO
651S-1/1A/1B SERVICE BULLETIN NO 12

Attached is a revised issue of 651S-1/1A/1B Service Bulletin No 12 titled, "Replacing Nonprocurable Integrated Circuits," dated 1 May 1978.

The changes are as follows:

1. Page 1, third paragraph, first sentence; change 351-7569-202 to 351-7569-020.

2. Page 1, third paragraph, third sentence rewritten for clarification.

3. Page 1, table, MODIFICATIONS REQUIRED column; change "No modification required by conversion" to "No modification required but conversion".

Black bars in the margin indicate where changes were made. This revised issue replaces the original publication.

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-XXX)
651S-1A GENERAL PURPOSE HF RECEIVER (622-1062-001)
651S-1B GENERAL PURPOSE HF RECEIVER (622-1165-001)
FREQUENCY CONTROL CARD A14 (783-9283-001)

SERVICE BULLETIN NO 12

REPLACING NONPROCURABLE INTEGRATED CIRCUITS

This service bulletin is applicable to 651S-1/1A/1B receivers equipped with Frequency Control Card A14 (783-9283-001).

When this modification is incorporated, the part number of Frequency Control Card A14 changes from 783-9283-001 to 783-9283-002. Therefore, production cut-in is 651S-1/1A/1B units that contain A14 cards with Collins part number 783-9283-002.

The component manufacturer has discontinued production of integrated circuits F9327B, Collins part number 351-7569-020. However, it will not be necessary to install this bulletin unless a failure of integrated circuits U1, U2, U3, U4, U5, or U6 (CPN 351-7569-020) on A14 card occurs. If any of these components are replaced, it is recommended that they all be replaced although it is not necessary. Receivers that still use the gas discharge type display must have service bulletin No 10 installed prior to installation of this bulletin.

A brief description of display configurations and modifications required for the 651S-1/1( ) follows:

DISPLAY TYPE	A14 CPN	MODIFICATIONS REQUIRED
Tube	783-9283-001	(1) Rework A14 to 783-9283-002 (2) Convert to plug-in LED display by installing Service Bulletin No 10
Tube	601-3363-001	No modification required but conversion to plug-in LED display per Service Bulletin No 10 is recommended.
Plug-in LED	783-9283-001	Rework A14 to CPN 783-9283-002
Plug-in LED	601-3363-001	No modification required.
LED board	601-3363-002	No modification required.

CAUTION: MODIFICATION OF FREQUENCY CONTROL CARD A14, CPN 783-9283-001, MAKES IT IMPOSSIBLE TO USE GAS DISCHARGE DISPLAY TUBES.

This modification consists of replacing six integrated circuits and the A14 circuit card handle.

Estimated time required is 1 man-hour.

The modification parts are itemized in the material information paragraph. Contact Collins Telecommunications Products Division/Rockwell International, Service Parts Department, Cedar Rapids, Iowa 52406, for price and availability of parts. All correspondence should reference 651S-1/1A/1B Service Bulletin No 12.

No special tools or equipment are required.

This service bulletin references the 651S-1/1A General Purpose HF Receiver Instruction Book maintenance section, Collins part number (CPN) 523-0764056, and parts list, CPN 523-0764057.

The next change to the 651S-1/1A instruction book maintenance section and parts list will include the change covered in this bulletin.

MODIFICATION PROCEDURE

A. Remove all power from the receiver.

NOTE: Refer to 651S-1/1A instruction book parts list section while performing this modification. Figure and item numbers are in parentheses.

B. Remove dust cover from 651S-1/1A/1B by removing two screws at rear of unit and sliding unit out of dust cover.

C. Remove card cage cover (1-8).

D. Remove Frequency Control Card A14 (1-10), CPN 783-9283-001, from the receiver.

E. Locate and note orientation (pin 1) of integrated circuits U1 (2-1), U2 (2-46), U3 (2-44), U4 (2-41), U5 (2-38), and U6 (2-33).

F. Remove U1 through U6 and replace them with new integrated circuits (351-1898-010).

G. Remove handle (2-134) and replace it with new handle (638-6356-001).

H. Reinstall A14 card into receiver.

I. Reinstall card cage cover. Be sure the magnetic shield is over the synthesizer cards, A10-A13.

J. Slide unit into dust cover and secure with two screws at rear of unit.

K. Mark SB 12 on information chart.

L. Refer to instruction book maintenance section, paragraph 4, and perform a simple test to ensure that the frequency display is working properly.

MATERIAL INFORMATION

The parts listed below are required to modify one 651S-1, 651S-1A, or 651S-1B.

COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
351-1898-010	6		Integrated circuit, 5448, U1, U2, U3, U4, U5, and U6
638-6356-001	1		Handle

Rockwell-Collins | **SERVICE BULLETIN**

Collins Telecommunications Products Division/Rockwell International

.350105

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-XXX)
651S-1A GENERAL PURPOSE HF RECEIVER (622-1062-001)
651S-1B GENERAL PURPOSE HF RECEIVER (622-1165-001)
RF MODULE A6 (790-1048-XXX)
RF MIXER (618-3258-001)
RF MIXER (606-9877-002)

SERVICE BULLETIN NO 13

REPLACE NONPROCURABLE PARTS

This service bulletin applies to 651S-1/1A/1B receivers equipped with the following rf mixer assemblies.

COLLINS PART NUMBER	APPLIES TO	PRODUCTION CUT-IN
606-9877-002	REV P and below	REV R
618-3258-001 (Q1, Q2, Q3 change)	REV S and below	REV T
618-3258-001 (A6A1U1 change)	REV T and below	REV U

The component manufacturers have discontinued production of integrated circuit U1 (350-3080-020) and transistors Q1, Q2, and Q3 (352-0756-070) in the rf mixer assemblies. This service bulletin provides a procedure for replacing these components with suitable substitutes. This modification should not be made unless the original components fail and no original spare parts are available.

Rf mixer assembly 618-3258-001 must be modified to 618-3258-002 when the original A6A1U1 (350-3080-020) is replaced by a substitute part.

Estimated time required is 2 man-hours.

The modification parts are itemized in the material information paragraph. For parts information, contact Collins Telecommunications Products Division/Rockwell International, Service Parts Department, Cedar Rapids, Iowa 52406. Reference 651S-1/1A/1B Service Bulletin No 13 in all correspondence.

No special tools or equipment are required.

This service bulletin references the 651S-1/1A General Purpose HF Receiver Instruction Book, Collins part number 523-0764052.

MODIFICATION PROCEDURE

A. Turn off all power to the receiver.

NOTE: For location of subassemblies and components, refer to the 651S-1/1A instruction book, part 2, parts list section, CPN 523-0764057. Figure and item numbers are in parentheses.

B. Remove the 651S-1 dust cover (1-1) by removing two screws on the rear of the unit. Slide the unit out of the dust cover.

C. Remove rf module assembly A6 (1-18).

NOTE: Steps D through G apply to rf modules with rf mixer assembly, CPN 606-9877-002, only.

D. Remove chassis cover (16-79).

E. Remove transistors Q1 (16-99), Q2 (16-98), and Q3 (16-108).

F. Install new transistors (352-0756-150) as follows:

NOTE: Refer to figure 1 of this bulletin while performing steps F.(1) through (5).

(1) Clip the case leads of the new transistors to a maximum length of 1.58 mm (1/16 in).

(2) Install the transistors upside down on the chassis using adhesive (005-1688-001). Q1 and Q2 must have the same vendor symbol for testing qualifications. Use insulation sleeving (152-2473-000) on all leads that cross over the transistor body.

(3) Connect Q1 source to terminal 21, drain to terminal 18, and gate to terminal 19.

(4) Connect Q2 source to terminal 21, drain to terminal 23, and gate to terminal 22.

(5) Connect Q3 source to terminal 8, drain to terminal 9, and gate to terminal 11.

G. Locate rf mixer assembly part number 606-9877-002 and mark RWK REV R near the part number.

NOTE: Steps H through Q apply to rf modules with rf mixer assembly, CPN 618-3258-001, only.

H. Remove rf mixer cover (36-1).

I. Remove transistors Q1 (37-17), Q2 (37-48), and Q3 (37-117).

NOTE: Refer to figure 2 of this bulletin while performing steps J through L.

J. Clip the case leads of the new transistors (352-0756-150) to a maximum length of 1.58 mm (1/16 in).

K. Install the transistors upside down on the chassis using adhesive (005-1688-001). Q1 and Q2 must have the same vendor symbol for testing qualifications. Use insulation sleeving (152-2473-000) on the drain leads of Q1 and Q3.

L. Connect the new transistors as shown in figure 2.

NOTE: Refer to figure 3 of this bulletin and the 651S-1/1A instruction book parts list while performing steps M through P. Refer to figure 4 for a schematic diagram which includes these changes.

M. Remove mixer U1 (350-3080-020).

N. Install new mixer U1 (351-0208-010) and connect as shown in figure 3.

O. Remove capacitors C49 (37-6) and C50 (37-5).

P. Remove capacitors C44 (37-141) and C46 (37-148) and replace them with 0.01 μF capacitors (913-4240-100).

Q. Locate rf mixer assembly part number 618-3258-001 and change it to 618-3258-002. Mark RWK REV T and RWK REV U near the part number.

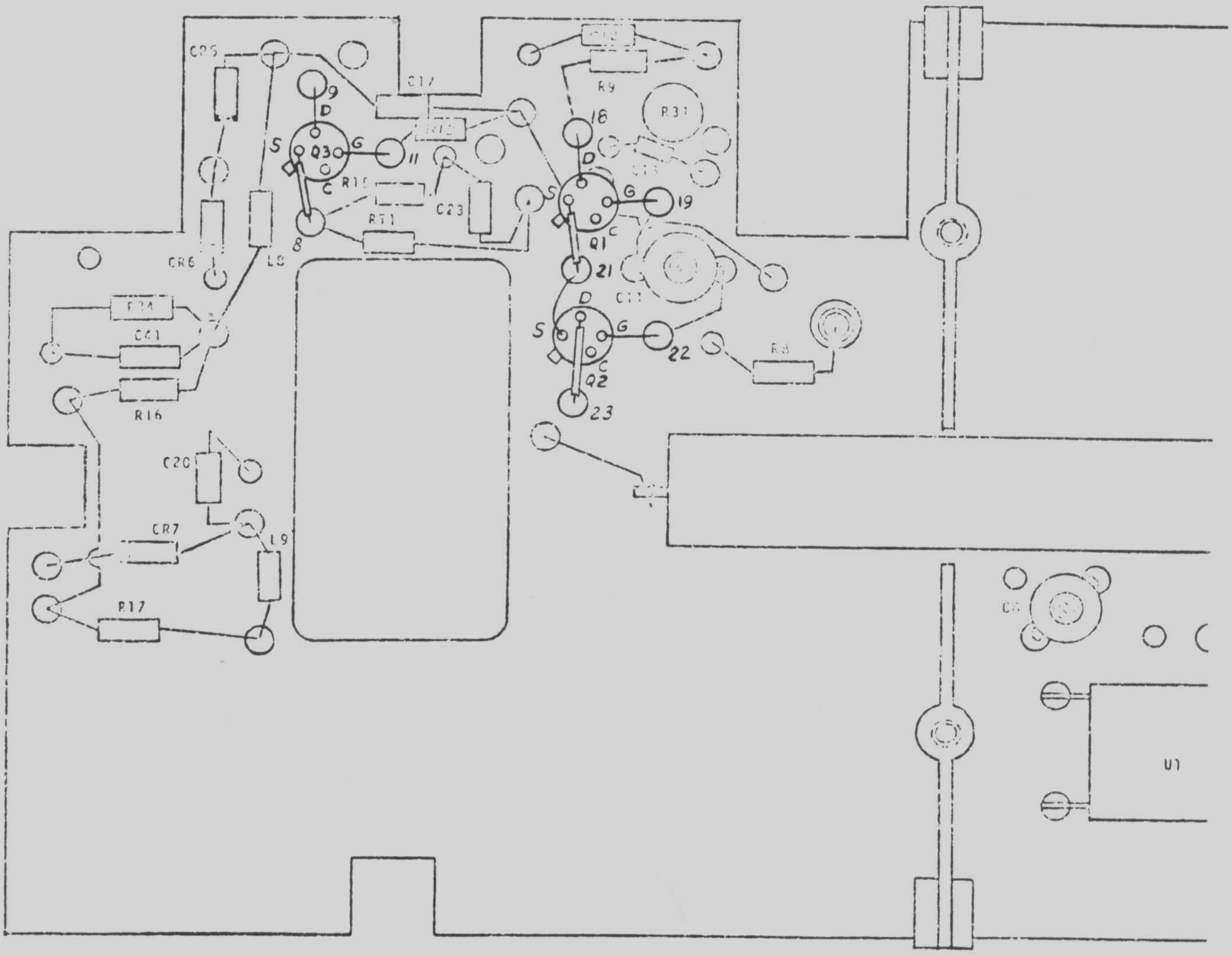
R. Reassemble the receiver in the reverse order of disassembly.

S. Mark SB 13 on the service bulletin information chart. If the receiver does not have an information chart, install a chart (280-3778-010) near the nameplate.

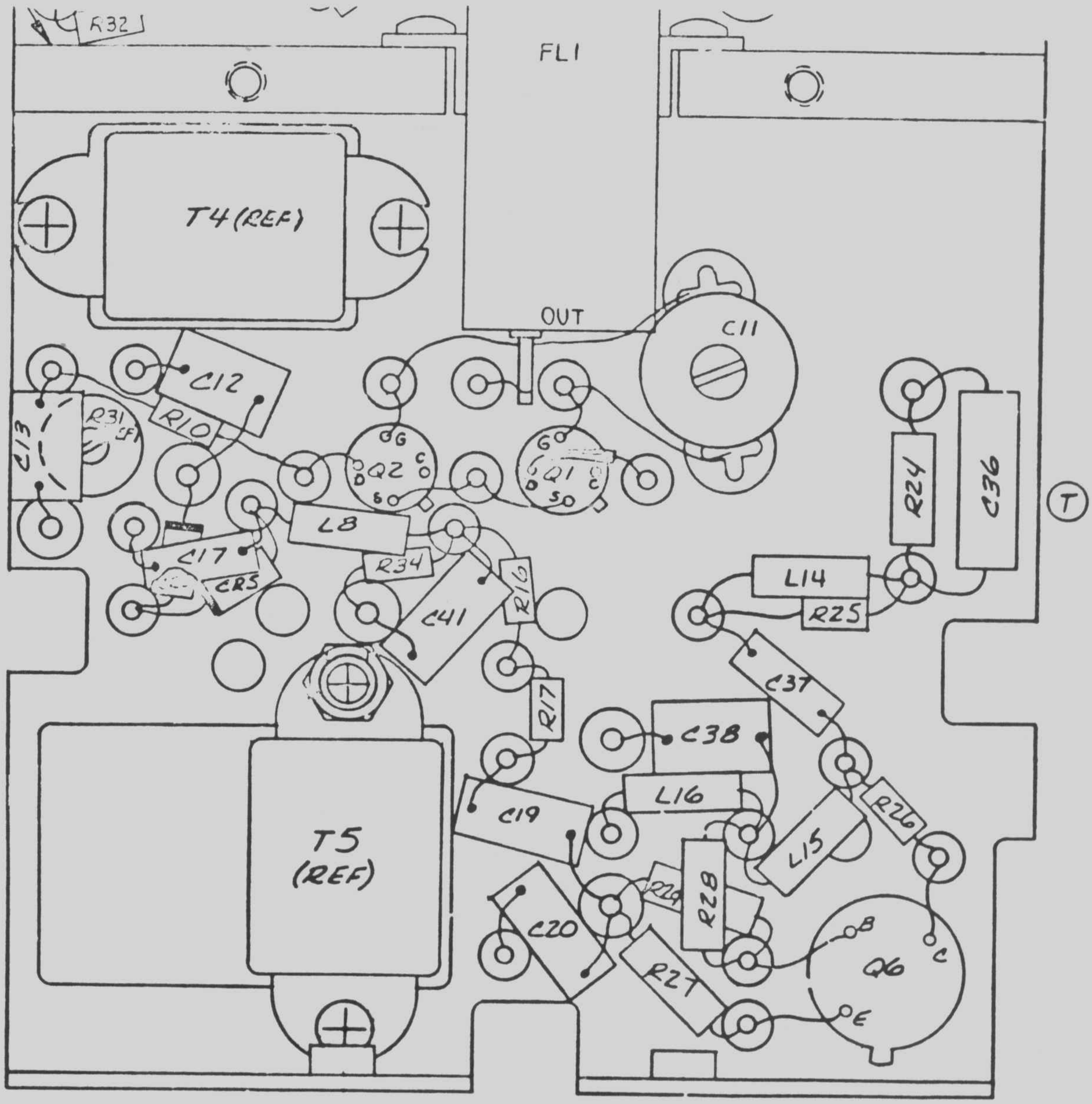
MATERIAL INFORMATION

COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
352-0756-150	3		Transistors, Q1, Q2, Q3
005-1688-001	AR		Adhesive
152-2473-000	50 mm (2 in)		Sleeving, insulation
351-0208-010	1		Integrated circuit, U1
913-4240-100	2		Capacitor, 0.01 μF, C44, C46
*280-3778-010	1		Chart, information

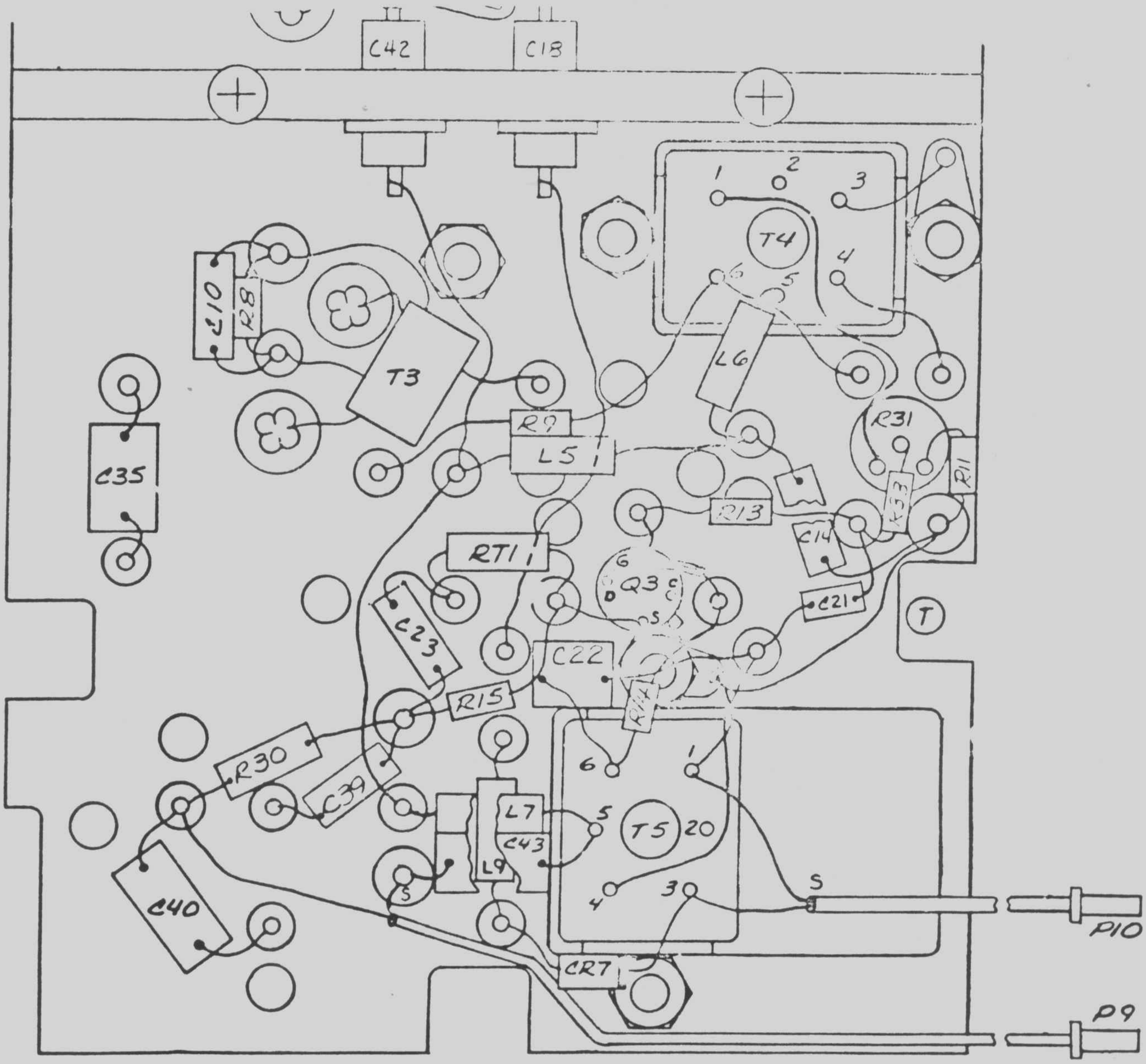
*Order if needed.



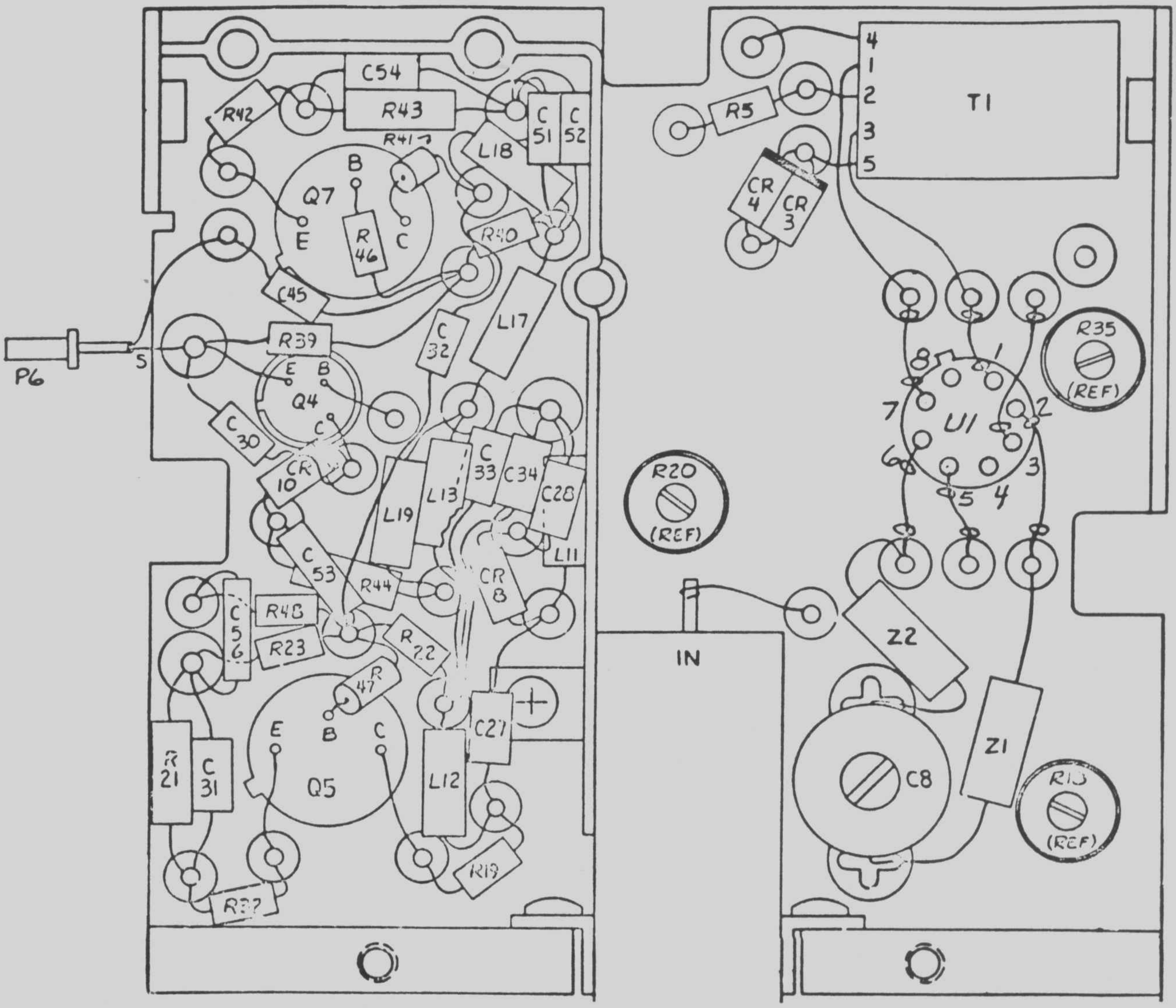
P/O RF Mixer (606-9877-002)
Figure 1



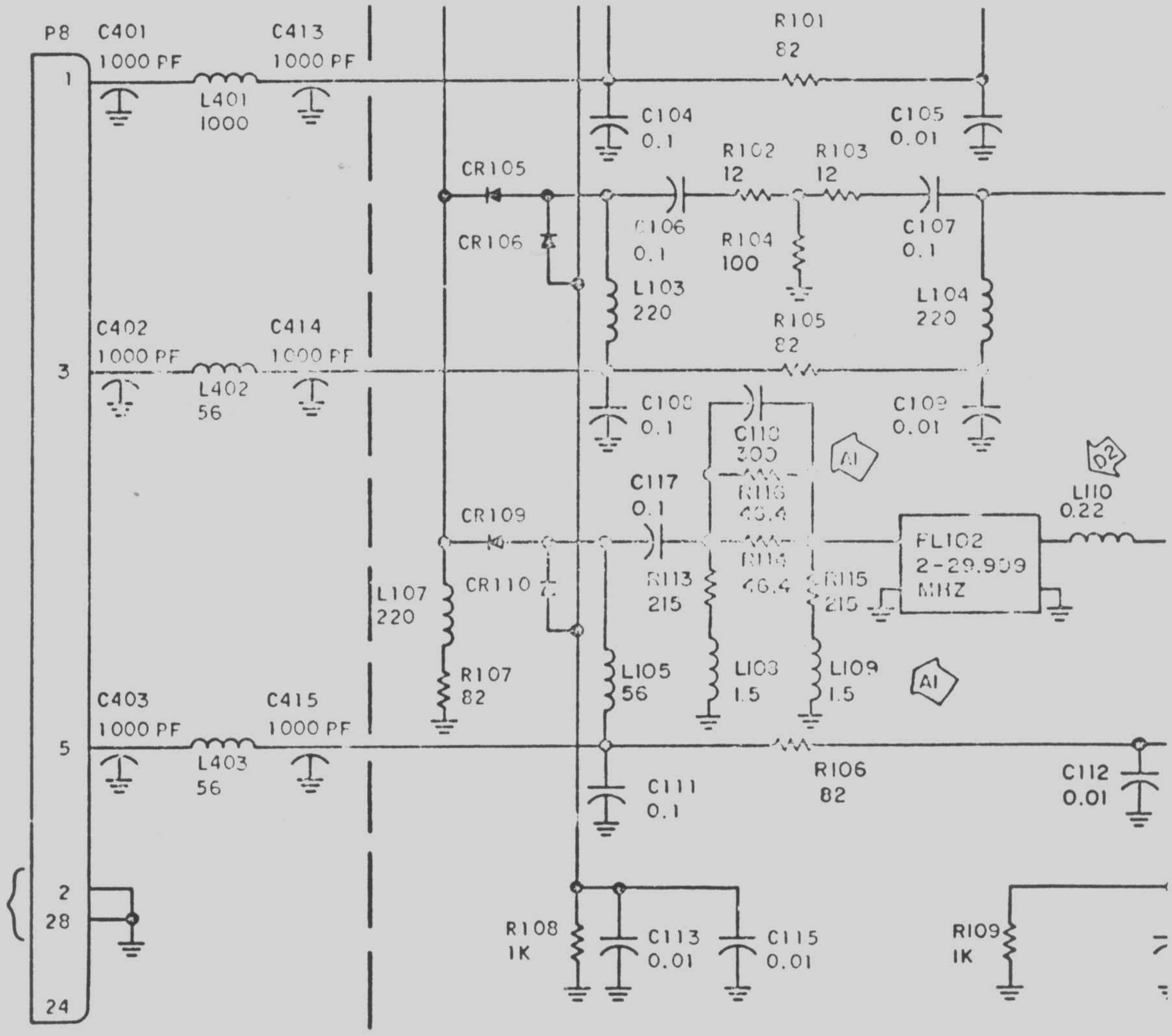
P/O RF Mixer (618-3258-002)
Figure 2 (Sheet 1 of 2)



P/O RF Mixer (618-3258-002)
Figure 2 (Sheet 2)



P/O RF Mixer (618-3258-002)
Figure 3



NOTES:

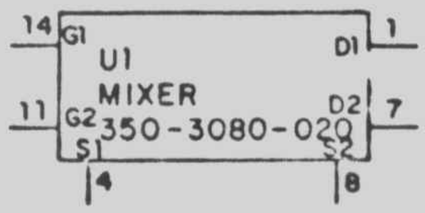
(1) UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS, AND ALL DIODES ARE TYPE 1N4001. D1 D2

(2) TEST SELECT COMPONENTS, SEE TABLE OF VALUES IN PARTS LIST.

(3) A6A1 CPN 618-3258-001—C49 AND C50 ARE 12 PF. C44 AND C46 ARE 24 PF.
A6A1 CPN 618-3258-002—C49 AND C50 ARE NOT USED. C44 AND C46 ARE 0.01 UF.

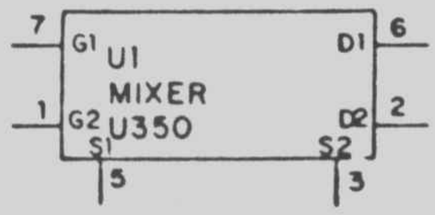
(4) A6A1 CPN 618-3258-001:

MICROCIRCUIT CONNECTIONS

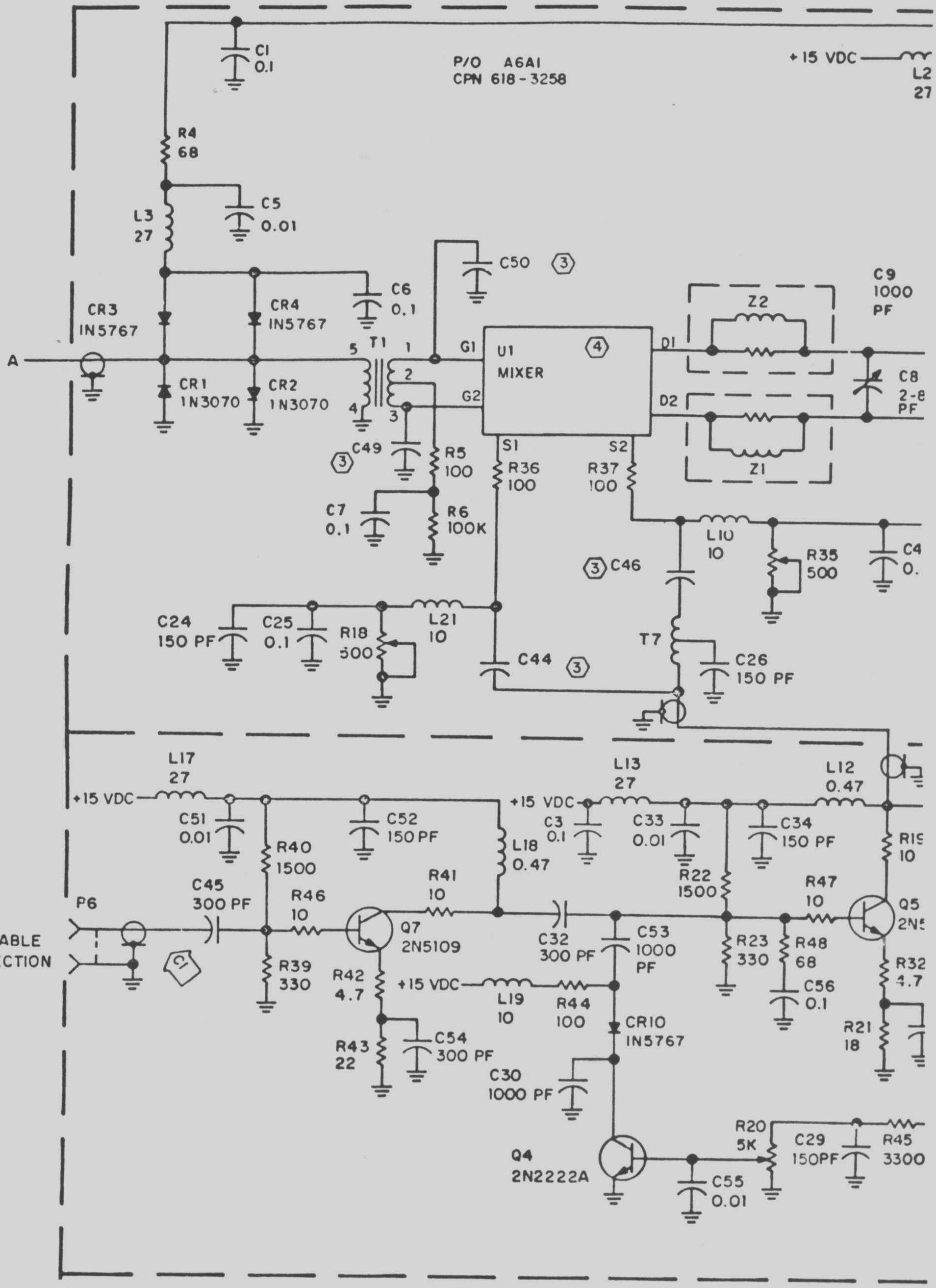


A6A1 CPN 618-3258-002:

MICROCIRCUIT CONNECTIONS



P/O RF Module A6 (790-1048-020), Schematic Diagram
Figure 4 (Sheet 1 of 2)



P/O RF Module A6 (790-1048-020),
Schematic Diagram
Figure 4 (Sheet 2)

Rockwell-Collins | **SERVICE BULLETIN**

Collins Telecommunications Products Division/Rockwell International

.350314

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-XXX)
651S-1A GENERAL PURPOSE HF RECEIVER (622-1062-001)
651S-1B GENERAL PURPOSE HF RECEIVER (622-1165-001)
SYNTHESIZER REFERENCE CARD A11 (608-9442-001)

SERVICE BULLETIN NO 14

REDUCE 100 kHz SIDEBANDS

This service bulletin applies to 651S-1 (522-4836-XXX), 651S-1A (622-1062-001), and 651S-1B (622-1165-001) units that contain synthesizer reference card A11 (608-9442-001) with REV H and below.

Production cut-in for reference card A11 is REV J.

This modification reduces the external standard sidebands on the phase-locked 9.9-MHz injection and is needed when operating the 651S-1 with a 100-kHz external standard and using the vlf up-converter for vlf reception. It prevents 100-kHz "birdies" from interfering with reception when the vlf converter is enabled.

This modification consists of removing three capacitors, replacing one coil, and adding one crystal and one jumper wire.

Estimated time required is 1.5 man-hour.

The modification parts are itemized in the material information paragraph. For parts information, contact Collins Telecommunications Products Division/Rockwell International, Service Parts Department, Cedar Rapids, Iowa 52406. Reference 651S-1/1A/1B Service Bulletin No 14 in all correspondence.

No special tools or equipment are required.

This service bulletin references the 651S-1/1A instruction book, part 2, Collins part number 523-0764052.

MODIFICATION PROCEDURE

A. Turn off all power to the receiver.

NOTE: Refer to the 651S-1/1A instruction book, part 2, parts list, CPN 523-0764057, for location of subassemblies and components. Figure and item numbers are in parentheses.

B. Remove the dust cover (1-1) by removing two screws on the rear of the unit. Slide the unit out of the dust cover.

C. Remove card cage cover (1-8) by removing the screws that secure it to the card cage.

D. Remove synthesizer reference card A11 (1-13) from the card cage.

E. Remove and discard coil L5 (6-31), and capacitors C17 (6-32), C18 (6-33), and C19 (6-30).

NOTE: Refer to figure 1 of this bulletin while performing steps F through I. Refer to figure 2 for before and after modification schematic diagrams.

F. Unsolder and move the square pin and coax cable shield from hole 1055 to hole 258. Solder the pin in hole 258.

G. Install 9.9-MHz crystal Y1 (289-7140-010) with insulator (352-9552-550) into holes 453, 454, and 1055 on top of board as shown in figure 1.

H. Install new 82 μH coil L5 (240-2715-360) flat onto top of card with leads connected to hole 511 and the square pin in hole 1050. Use insulation sleeving (152-2493-000) on the L5 lead to hole 1050. The coax cable center conductor should remain on the square pin in hole 1050.

I. Install and solder a #26 AWG bus wire from hole 512 to hole 507 on top of board.

J. Stamp RWK REV J near the existing REV letter.

K. Reassemble the receiver in the reverse order of disassembly.

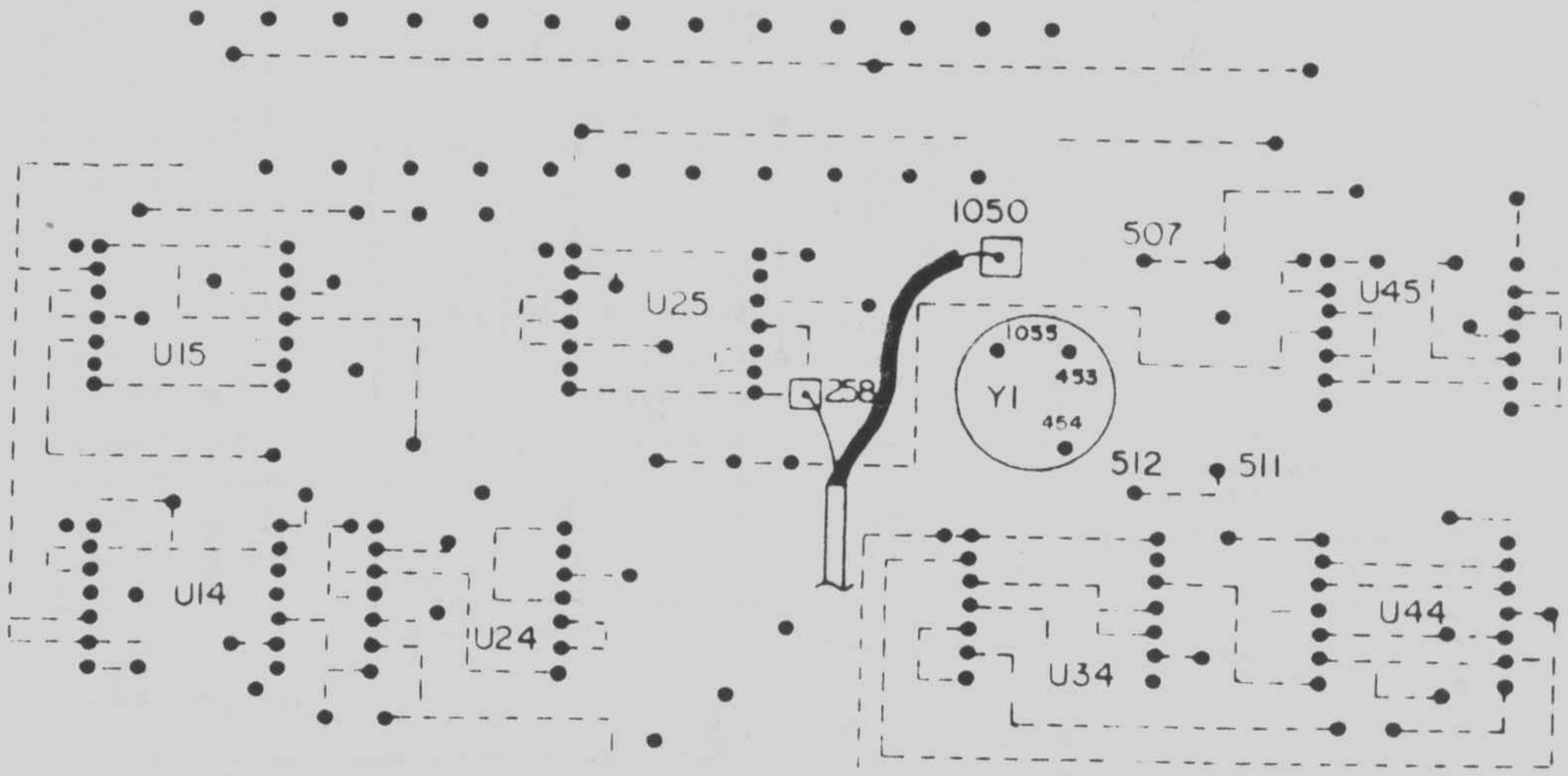
L. Mark SB 14 on the service bulletin information chart. If the receiver does not have an information chart, install a chart (280-3778-010) near the nameplate.

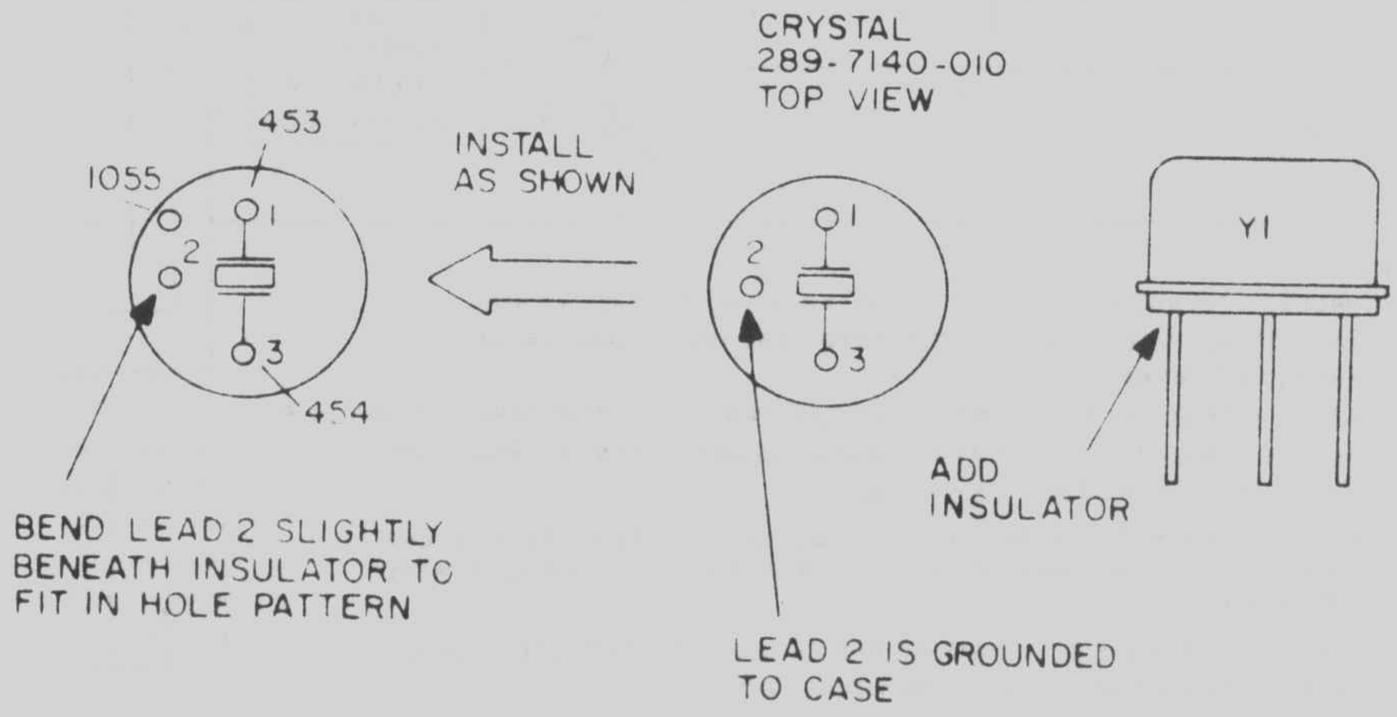
MATERIAL INFORMATION

The parts listed below are required to modify one 651S-1, 651S-1A, or 651S-1B.

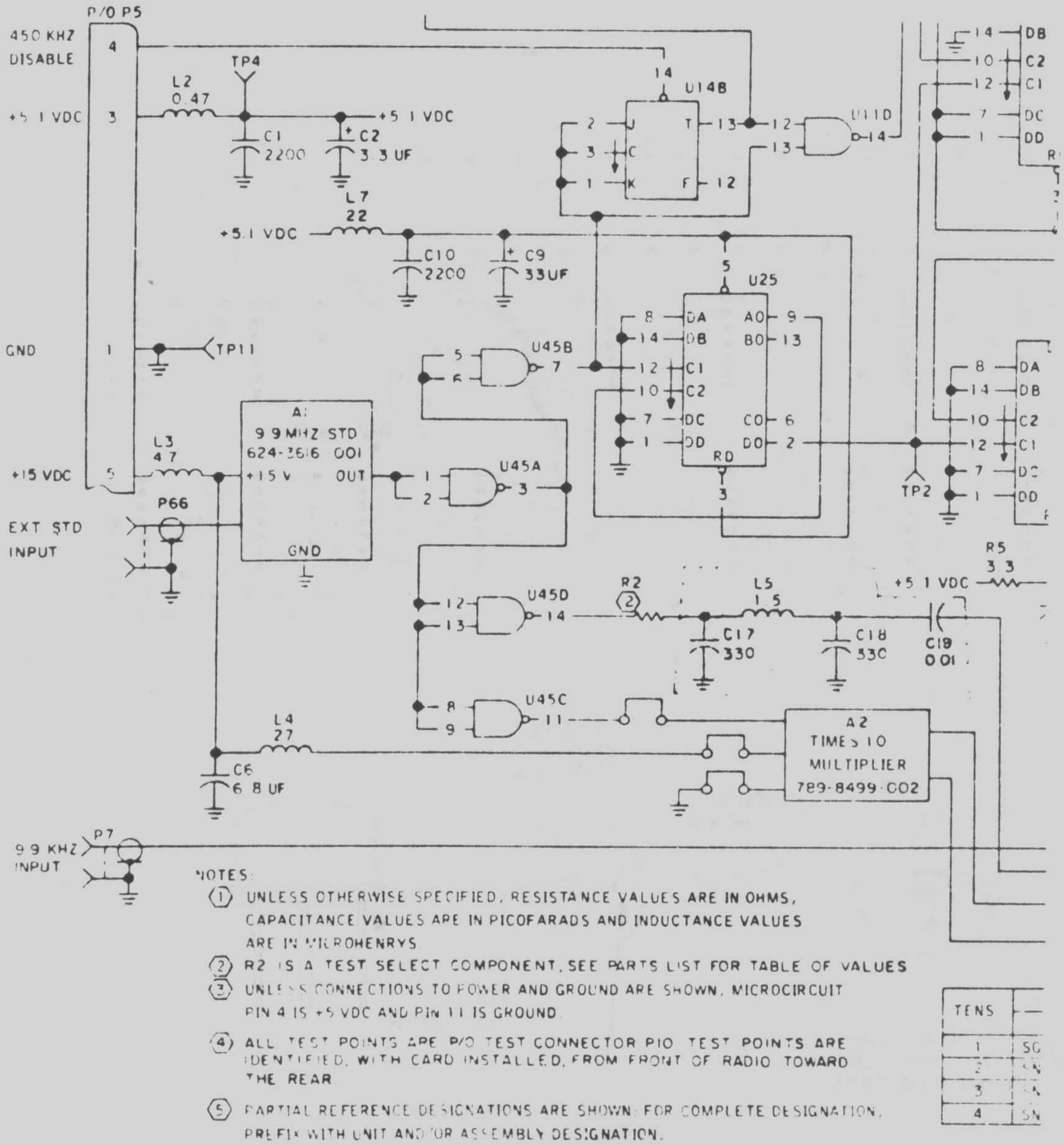
COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
289-7140-010	1		Crystal, 9.9 MHz, Y1
352-9552-550	1		Insulator
240-2715-360	1		Choke, 82 μH, L5
428-0282-030	25 mm (1 in)		Wire, #26 AWG
152-2493-000	25 mm (1 in)		Sleeving, insulation
*280-3778-010	1		Chart, information

*Order if needed.





Crystal Filter Y1 Installation Diagram
Figure 1



NOTES:

(1) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN PICOFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS

(2) R2 IS A TEST SELECT COMPONENT, SEE PARTS LIST FOR TABLE OF VALUES

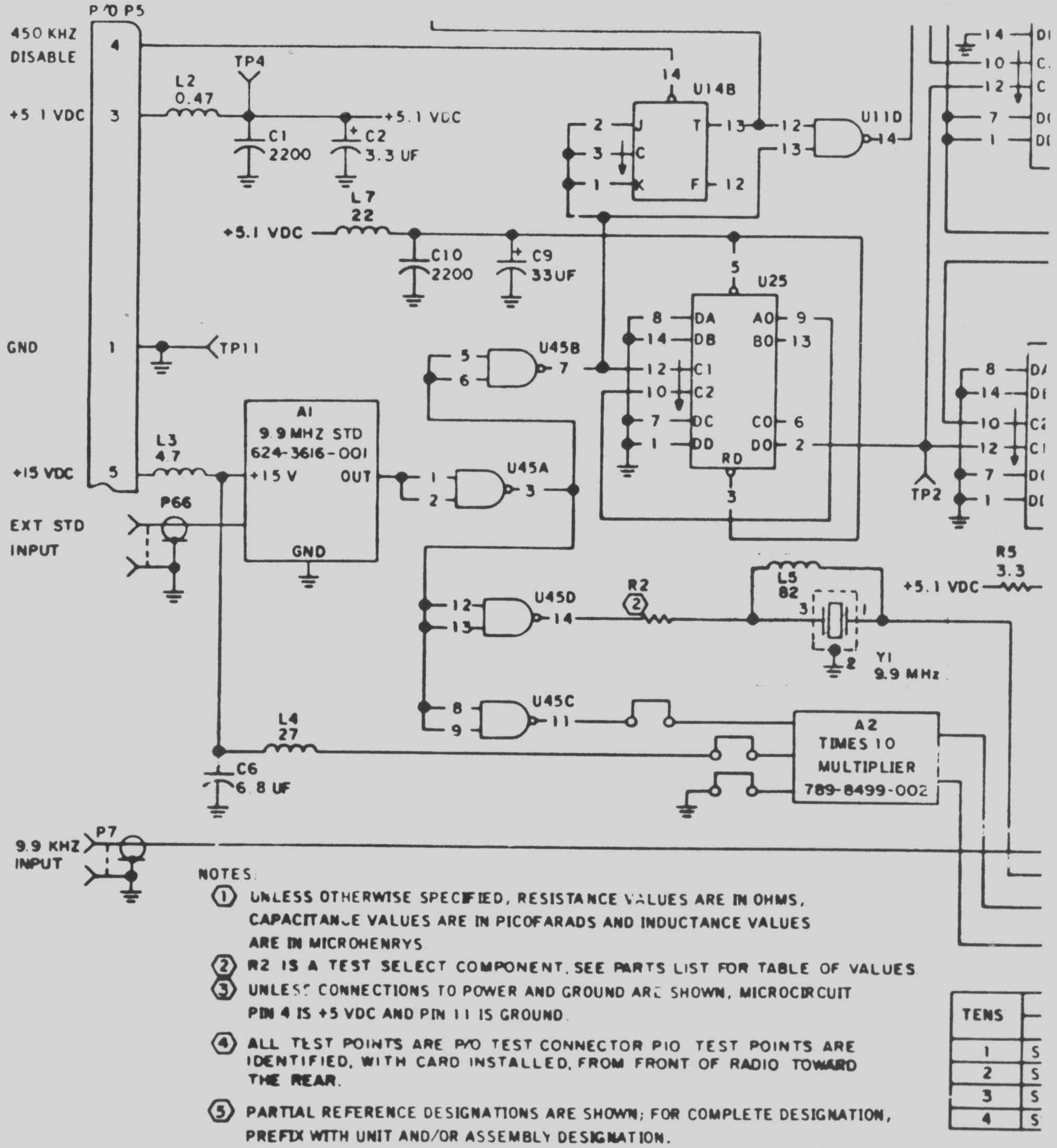
(3) UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN 4 IS +5 VDC AND PIN 11 IS GROUND.

(4) ALL TEST POINTS ARE P/O TEST CONNECTOR P10. TEST POINTS ARE IDENTIFIED, WITH CARD INSTALLED, FROM FRONT OF RADIO TOWARD THE REAR.

(5) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

TENS	—
1	SG
2	SN
3	SN
4	SN

P/O Synthesizer Reference Card A11, Before Modification, Schematic Diagram
Figure 2 (Sheet 1 of 2)



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN PICOFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. R2 IS A TEST SELECT COMPONENT. SEE PARTS LIST FOR TABLE OF VALUES.
3. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN 4 IS +5 VDC AND PIN 11 IS GROUND.
4. ALL TEST POINTS ARE P/O TEST CONNECTOR P10. TEST POINTS ARE IDENTIFIED, WITH CARD INSTALLED, FROM FRONT OF RADIO TOWARD THE REAR.
5. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

TENS	
1	S
2	S
3	S
4	S

Rockwell-Collins | **SERVICE BULLETIN**

Collins Telecommunications Products Division/Rockwell International

.350363

651S-1 GENERAL PURPOSE HF RECEIVER (522-4836-XXX)
651S-1B GENERAL PURPOSE HF RECEIVER (622-1165-XXX)
DCFE CIRCUIT CARD ASSEMBLY A8 (624-5744-XXX)
DCFE CIRCUIT CARD ASSEMBLY A8 (608-9322-001)

SERVICE BULLETIN NO 15

PREVENT INVALID MONITOR RESPONSES FROM THE HF RECEIVER

This service bulletin applies as follows:

EQUIPMENT	APPLIES TO SERIAL NUMBERS	PRODUCTION CUT-IN SERIAL NUMBER
651S-1 522-4836-XXX	6266 and below	6267
651S-1B 622-1165-XXX	134 and below	135
Production cut-in for circuit card A8 (624-5744-XXX) is REV Y, and circuit card A8 (608-9322-001) is REV G.		

When using the DCFE card with the RS-232 control option, DCFE shift register strobe logic level transitions may be coincident with the shift register mode control line transitions. Coincidence of these signals may cause logic upset in some integrated circuits (SC5047F or RL301J), resulting in an invalid monitor response from the receiver.

In the 651S-1, if integrated circuits U9, U17, U21, U25, U29, U33, or U37 on A8 (624-5744-XXX) are replaced or if symptoms described above appear, this service bulletin should be implemented.

In the 651S-1B, if integrated circuits U7, U14, U21, U25, U30, U35, or U40 on A8 (608-9322-001) are replaced of if the symptoms described above appear, this service bulletin should be implemented.

This modification consists of adding a capacitor on the DCFE circuit card to delay the parallel input strobe to the DCFE shift registers.

Estimated time required is 1.0 man-hour.

The modification parts are listed in the material information paragraph. For additional information concerning parts, contact Collins Telecommunications Products Division/

Rockwell International, Service Parts Department, Cedar Rapids, Iowa, 52406. Reference 651S-1/1B Service Bulletin No 15 in all correspondence.

No special tools or equipment are required.

This service bulletin references the 651S-1/1A General Purpose HF Receiver Instruction Book, CPN 523-0764052, and the 651S-1B General Purpose HF Receiver Instruction Book, CPN 523-0765619.

MODIFICATION PROCEDURE

A. Disconnect the receiver from the power source.

NOTE: Refer to the 651S-1/1A instruction book, part 2, parts list section, CPN 523-0764057, and to the 651S-1B instruction book parts list section, CPN 523-0765625, for location of subassemblies and components. Figure and item numbers are in parentheses.

B. Remove dust cover (1-1, 651S-1 or 1-2, 651S-1B) by removing two screws on the rear of the unit. Slide the unit out of the dust cover.

C. Remove left hand card cage cover (1-8) by removing the screws that secure the cover to the card cage.

D. Remove DCFE circuit card A8 (1-16, 651S-1 or 1-32, 651S-1B) from the card cage.

NOTE: Refer to the parts list section, figure 14 (651S-1) or figure 16 (651S-1B) for orientation while installing the new capacitors. Steps E and F apply to circuit card A8, CPN 624-5744-XXX.

E. Install a 1500-pF capacitor C20 (913-3279-040) between U29-3 and C4 bottom lead as shown in figure 1. Use sleeving (152-2463-000) on the capacitor leads.

F. Stamp RWK REV Y near the existing REV letter.

NOTE: Steps G, H and I apply to circuit card A8, CPN 608-9322-001.

G. Install a post (372-2601-010) at U14-3 on the top of the circuit card as shown in figure 2.

H. Install a 1500-pF capacitor C12 (913-3279-040) between the new post and the ground lead of C9 as shown in figure 2. Use sleeving (152-2463-000) on the capacitor leads.

I. Stamp RWK REV G near the existing REV letter.

J. Reassemble the receiver in the reverse order of disassembly.

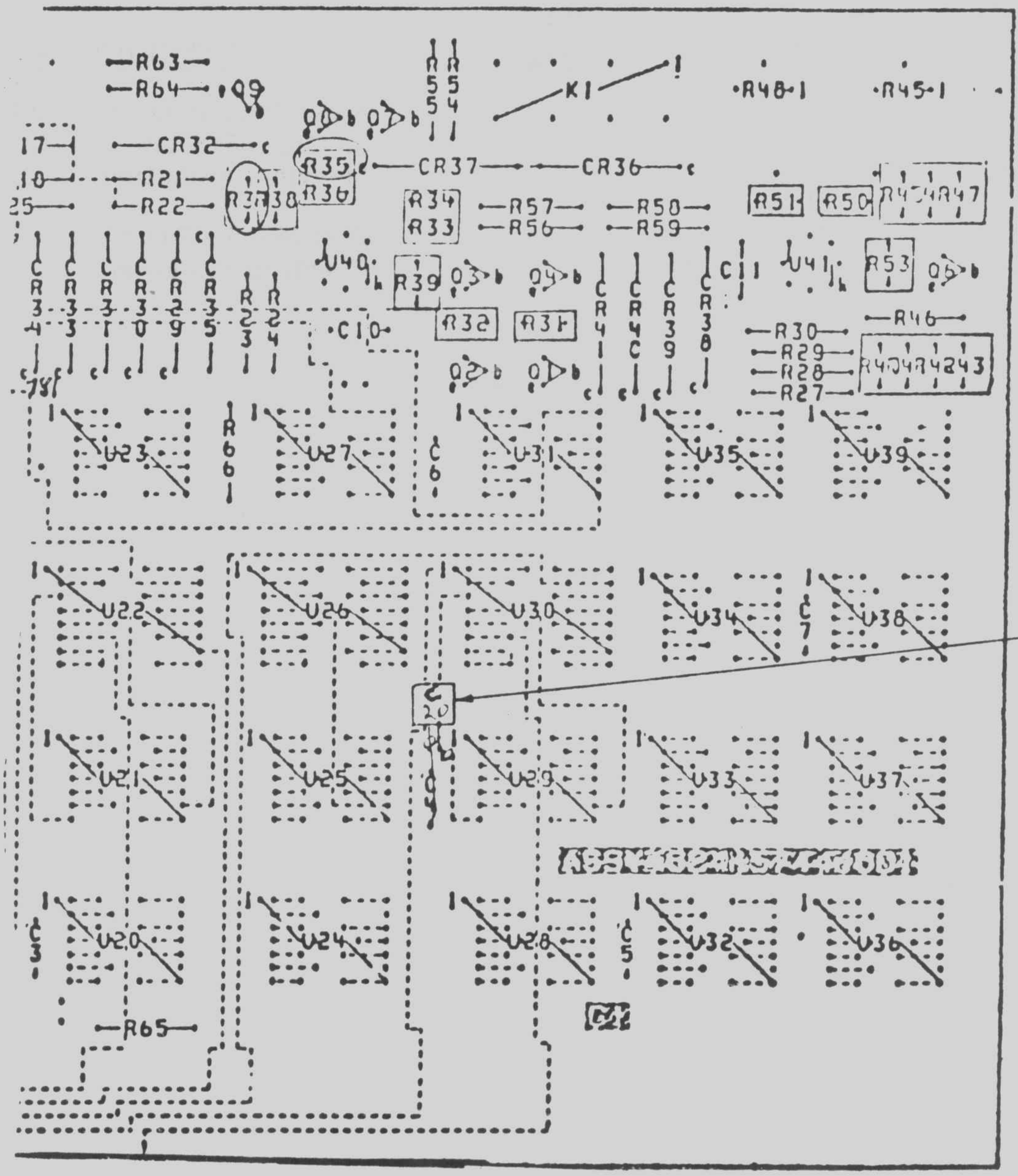
K. Mark SB 15 on the service bulletin information chart. If the radio does not have an information chart, order a chart (280-3778-010) and attach it near the nameplate.

MATERIAL INFORMATION

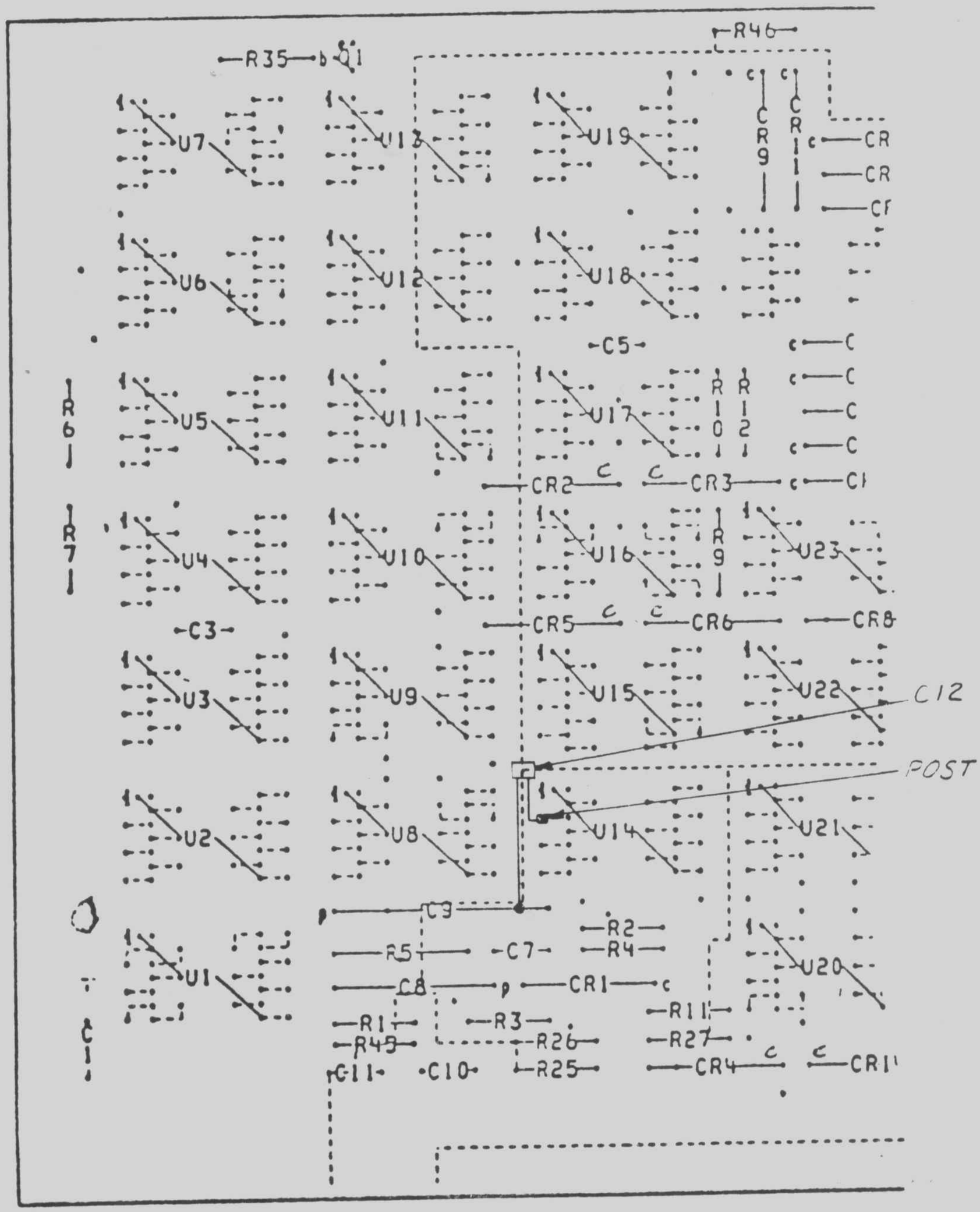
The parts listed below are required to modify one 651S-1 or one 651S-1B.

COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
913-3279-040	1		Capacitor, 1500 pF, C20 (651S-1) or C12 (651S-1B)
152-2463-000	50 mm (2 in)		Sleeving, insulation
372-2601-010	1		Post (651S-1B only)
*280-3778-010	1		Chart, information

*Order if needed.



P/O DCFE Circuit Card Assembly A8 (624-5744-001)
Figure 1



P/O DCFE Circuit Card Assembly A8 (608-9322-001)
Figure 2

Collins
Collins Radio Group
Rockwell International

SERVICE BULLETIN

651S-1 GENERAL PURPOSE HF RECEIVER (522-[illegible]36-XXX)
651S-1A GENERAL PURPOSE HF RECEIVER (622-1062-001)
INDICATOR HOUSING ASSEMBLY (606-9707-002)

SERVICE BULLETIN NO 9

INCREASE LIFE OF DISPLAY TUBES

This modification is applicable to all 651S-1/1A receivers containing indicator housing assembly (606-9707-002) that is marked with Rev F and below.

Production cut-in for the indicator housing assembly: Rev G and above.

The purpose of this modification is to increase the life of display tubes by decreasing the filament voltage. This condition has little effect on the initial brightness of the display tubes.

The modification consists of moving a wire and installing a resistor. This accomplishes the same result as the production revision, which changes the values of R132, R140, R148, R156, R164, and R172 from 82 to 100 ohms.

Estimated time to perform this modification is 1 man-hour.

The modification parts (as listed in the material information paragraph) are available for shipment within 30 days after receipt of order at a price of $0.55 (price is subject to change without notice; minimum order price is $25.00). Parts may be ordered from Collins Radio Group/Rockwell International, Service Parts Department, Cedar Rapids, Iowa 52406. All orders should specify part numbers and reference 651S-1/1A Service Bulletin No 9.

No special tools or equipment required.

Revision 1 of the 4th edition of the diagrams section (523-0764058) of the 651S-1/1A General Purpose HF Receiver Instruction Book, Part 1 (523-0764052), and revision 2 of the 4th edition of the parts list section (523-0764057) of the 651S-1/1A General Purpose HF Receiver Instruction Book, Part 2, will cover the changes included in this bulletin.

MODIFICATION PROCEDURE

A. Disconnect all external cables and wiring. Remove two screws from rear of unit and slide dust cover from the unit.

B. Mount standoff terminal (306-1018-000) on TB103 (refer to figure 1).

C. Mount 3.3-ohm resistor between the standoff terminal and TB103-10 and solder.

D. Unsolder blue wire from J56-4. See figure 1. Pull this wire through the cable ties and connect and solder to the standoff terminal mounted in step B.

E. Mark information chart (280-3778-010) with SB 9 and apply to chassis near nameplate.

F. Slide cover back on unit and replace two screws on rear of unit.

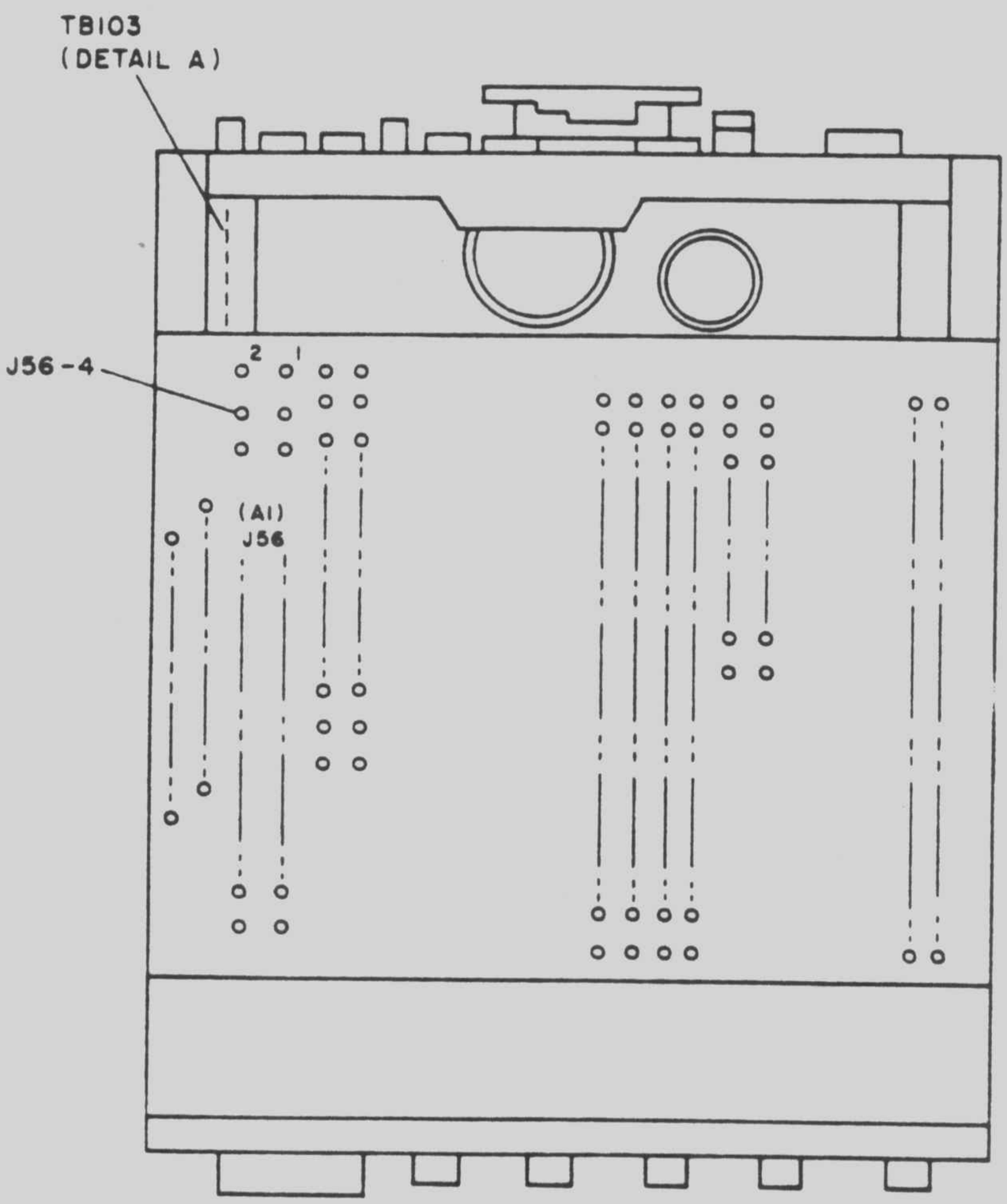
G. Reconnect external cables and wires and check that the display tubes light properly.

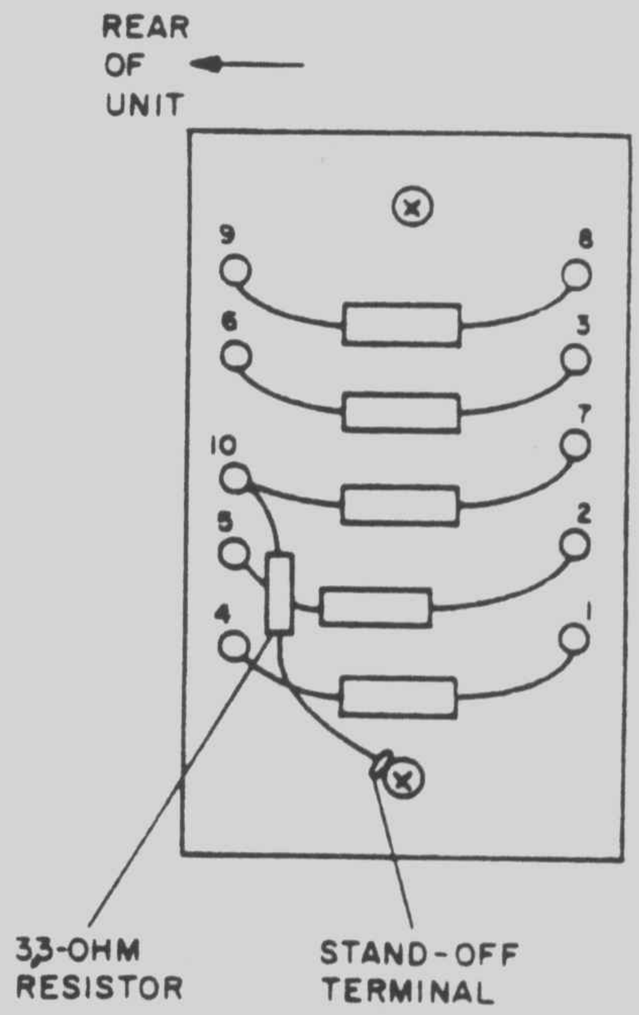
NOTE: Refer to figure 2 for the schematic modifications.

MATERIAL INFORMATION

The following parts are required to modify one 651S-1/1A.

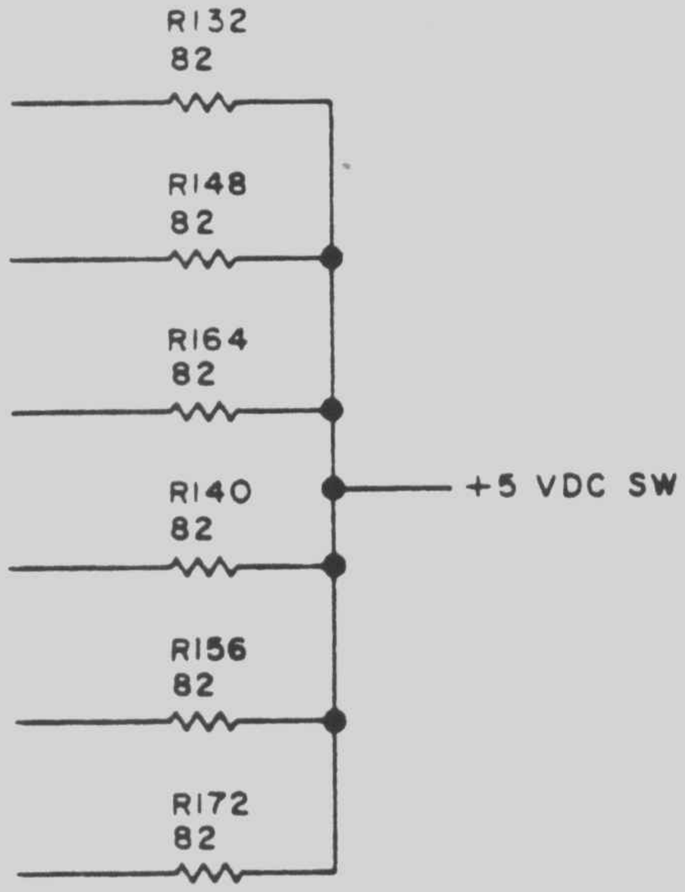
COLLINS PART NUMBER	QTY	UNIT PRICE	DESCRIPTION
280-3778-010	1	$0.30	Chart, information
306-1018-000	1	0.09	Terminal, standoff
745-4376-000	1	0.16	Resistor, 3.3-ohm, 1/4-watt, RCR07G3R3JS



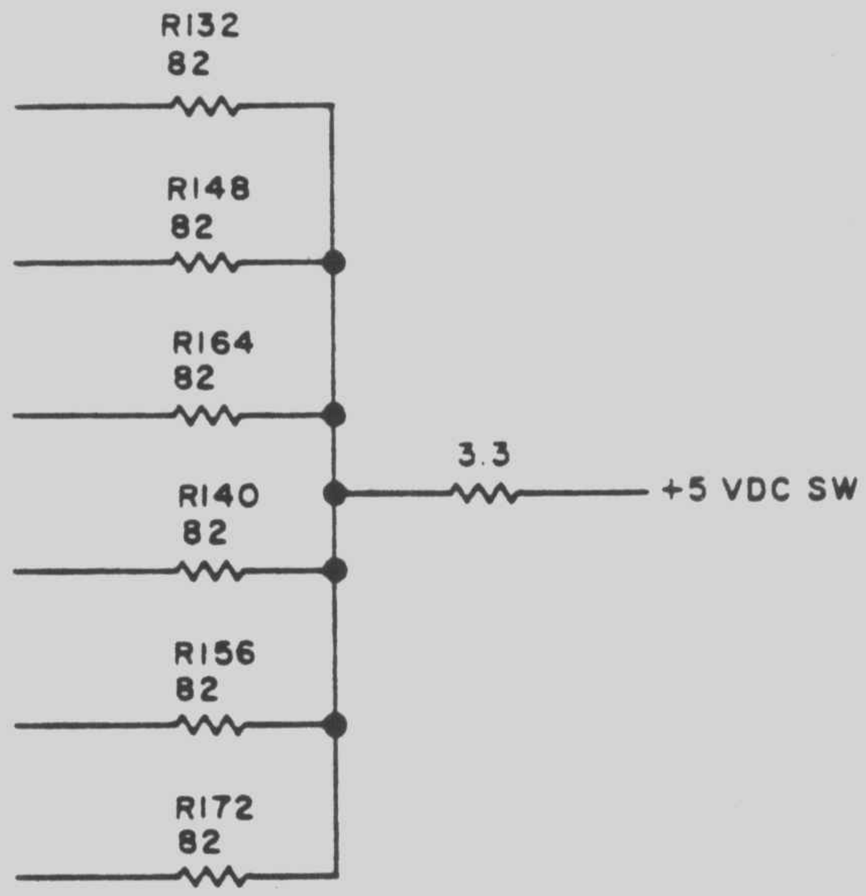


DETAIL A (TB103)

651S-1/1A Chassis, Bottom View
Figure 1



BEFORE



AFTER

NOTE:
INSTEAD OF ADDING 3.3 OHM RESISTOR ON PRODUCTION UNITS WITH REVISION G, THE SIX RESISTORS ARE CHANGED FROM 82 TO 100 OHMS.

651S-1/1A Chassis, Partial Schematic Diagram
Figure 2